

**ANALYSIS, DESIGN AND DEVELOPMENT OF ROBUST
DIGITAL CONTROLLERS FOR
FOURTH-ORDER BOOST DC-DC CONVERTERS**

by

ANMOL RATNA SAXENA

Department of Electrical Engineering

**Submitted in fulfillment of the requirements of the degree of
DOCTOR OF PHILOSOPHY
to the**



INDIAN INSTITUTE OF TECHNOLOGY DELHI

SEPTEMBER 2013

CERTIFICATE

This is to certify that the thesis entitled “**ANALYSIS, DESIGN AND DEVELOPMENT OF ROBUST DIGITAL CONTROLLERS FOR FOURTH-ORDER BOOST DC-DC CONVERTERS**” being submitted by **Mr. Anmol Ratna Saxena** for the award of degree of **Doctor of Philosophy** is a record of a bonafide research work carried out by him in the Department of Electrical Engineering of Indian Institute of Technology, New Delhi.

Mr. Anmol Ratna Saxena worked under my guidance and supervision and has fulfilled the requirement for the submission of the thesis, which to my knowledge has reached the requisite standards. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any Degree or Diploma.

Date: September 2013

(Prof. M. Veerachary)
Department of Electrical Engineering
Indian Institute of Technology Delhi
New Delhi-110016

ACKNOWLEDGEMENTS

It is a proud privilege of mine to extend my heartfelt gratitude to my esteemed supervisor Dr. M. Veerachary, Professor, Department of Electrical Engineering, IIT Delhi. His untiring zeal, commitment towards excellence in work, extensive vision and towering scholarship has been the source of inspiration for me throughout the research period. In spite of all important engagements, he always spared his precious time for me and gave his valuable and enlightening suggestions. His vast knowledge, wide experience, innovative ideas, constructive criticism and continuous encouragement consistently improved the quality of this work and helped me to think innovatively on my research work. Without his support and guidance it would have been truly impossible for me to carryout this research work. It is difficult for me to find appropriate words for salutation towards his all time endeavors. I am very much thankful to Prof. (Drs.) Gert-Helge Geitner, Technische Universitat Dresden, Prof. Mahesh Kumar, IIT Madras for their valuable comments.

My most cordial gratitude is also due to my SRC members: Prof. J. K. Chatterjee, Prof. P.R. Bijwe and Prof. T.S. Bhatti for their valuable suggestions, comments, motivation and encouragement during the tenure of this work. I would like to take this opportunity to express my deep sense of indebtedness to Prof. (Mrs.) B. Bhaumik, Head of department and all faculty members of the department specially PEEMD group for their constant motivation throughout my study at IIT Delhi.

I would also like to extend my gratitude to Mr. Gurcharan Singh and Mr. S.S. Negi for their outmost cooperation rendered in providing lab equipment and components at all times. My heartfelt thanks to my colleagues in Power Electronics Lab T. Chandrasekhar, B. Amarendra Reddy, Vargil Kumar, Sudhakar, Priyesh, Frieahun, Ankit, Shikha and Swati. I would also like to thanks M. Tech students Suresh, Kamlesh, B. Krishna Mohan, Satish, Sachin, Anand, V. Krishna Mohan, Mukesh, Vijay for helpful discussions, great supports and precious friendship.

I am also grateful to Dr. Sanjeev Jain, Director MITS Gwalior and Dr. M. Pandit, HOD, Dept. of Electrical Engg. and other colleagues at MITS, Gwalior for constant support and cooperation extended by them at the time of writing of this thesis.

Now emotions are flowing like an endless river to acknowledge them who gave actual shape to my whole life. All the words could not sum up the pain and hardship that my adorable parents faced in bringing me till this stage, I remember the sacrifices made by them in shaping my career. Their motivation, positive attitude, love unlimited faith and confidence has been the guiding principles of my life. I would also like to express my sense of gratitude to my parents-in-law for showing confidence in me and for their inspiration, support, motivation and love in my life. I seek their blessing and the blessings of God and dedicate this dissertation work to my parents and parents-in-law.

As truly said, "Behind every success, there is a woman" but for me two women are constant source of inspiration, one is my lovely wife 'Priyanka' and other my cute daughter 'Aadya'. I am thankful to both of them from the depth of my heart for their love, inspiration, constant encouragement & support in my life. I am indebted to the sacrifice made by them during this research work, especially during the writing of thesis. It is the cute face of Aadya which made me to stand back on my feet after every setback. This research work is dedicated to them too.

At this juncture, I am feeling immense pleasure to convey my heartiest thanks to my younger brothers Asheesh and Abhishek along with their wife Rajani and Kanika for their constant support, motivation & love. I would also like to mention the name of Aryashree, on seeing her face I forget all my tensions. A special thanks to Kamal and Neha for their motivation and support and of course good time we spent together.

I would also like to thank Manish for his motivation, encouraging thoughts and being with me whenever I needed.

While writing this page of my thesis, I derive immense pleasure in acknowledging all those who directly and indirectly helped me in accomplishing the task of completing the work successfully. Truly said success depend in a large amount upon individual initiative, exertion and hard work, but it won't be an exaggeration to say that nothing can never be achieved without the guidance, support, love and care of those in whom you place your trust.

Date: September 2013

Anmol Ratna Saxena

ABSTRACT

In this thesis, non-isolated fourth-order boost dc-dc converter topologies that are obtained by structural rearrangement of boost converter with output filter are analyzed with the aim of evolving a fourth-order boost topology, exhibiting low source current ripple together with low overall inductance requirement, improved dynamic response and satisfying other steady-state requirements. Discrete-time models that are considered to be more accurate than averaged model are formulated for fourth-order boost converters and used to derive small-signal discrete-time transfer functions, which characterize the dynamical behavior of these converters. Discrete-time models formulated in this thesis takes into account the effect of sampling instant, PWM modulation and delay in control loop and used to facilitate the controller design and analyze the converter stability with voltage-mode and current-mode control. Non-linear sampled data models have also been derived from the exact discrete-time model for continuous conduction mode of operation.

It is shown through discrete-time analysis that the presence of additional energy storage elements as compared to conventional boost converter increases the complexity in control loop design. Particularly, dynamic response improvement becomes a challenging task which is on account of successive multiple complex-conjugate pole-zero pattern, which forms an up-down glitch in the small-signal characterizing transfer functions of fourth-order boost converters. The implications this up-down glitch on dynamic performance of the converters is addressed and factors affecting the shape of the up-down glitch are brought out. Safety margin is proposed as an additional design specification which along with gain margin and phase margin must be used to judge the stability of fourth-order converters. A generalized optimization procedure, using particle swarm optimization, with a possibility to extend for other higher-order topologies is proposed to

resolve the contradictory issues of steady-state and dynamic performance requirements in fourth-order dc-dc converters.

Controllers for point of load converters, either for voltage-mode control or current-mode control are designed to regulate the load voltage against small disturbances around their steady-state operating points. However, there are certain factors which are classified as structured and unstructured uncertainties, that not only degrade the converter performance over due course of time but even tend to make them unstable in some cases. Therefore, robust digital voltage-mode and current-mode controllers are designed for fourth-order boost converters using Quantitative Feedback Theory (*QFT*) which takes into account the effect of these uncertainties. A modified loop shaping approach is proposed for controller design, wherein controller designed using pole-placement approach is used to initiate loop-shaping in *QFT GUI* environment. A robust digital deadbeat controller is proposed for fourth-order boost converters, where inductance estimation is done online by taking only one sample in one switching period and then control law is updated in every switching cycle based on the estimated value of inductance. The dynamic performance and robustness range of the converters against structured and unstructured uncertainties is verified experimentally on 12-to-28 V, 30 W laboratory prototypes of the converters and shows that experimental results are inline with the simulation and analytical design studies made in the thesis.

CONTENTS

CERTIFICATE	i
ACKNOWLEDGEMENTS	iii
ABSTRACT	v
CONTENTS	vii
LIST OF FIGURES	xv
LIST OF TABLES	xxvii
LIST OF SYMBOLS AND ABBREVIATIONS	xxix
1 INTRODUCTION	1
1.1 Introduction	1
1.2 Scopes and Objectives	9
1.3 Main Contributions of Thesis	10
1.4 Organization of Thesis	11
1.5 Publications	13
2 NON-ISOLATED FOURTH-ORDER BOOST CONVERTER TOPOLOGIES	15
2.1 Introduction	15
2.2 Fourth-Order Boost Dc-Dc Converters	20
2.2.1 Fourth-Order Boost Dc-Dc Converter	20
2.2.1.1 State-Space Analysis	23
2.2.2 Two-Inductor Boost Dc-Dc Converter	24
2.2.2.1 State-Space Analysis	25
2.2.2.2 Hidden Issues in Two-Inductor Boost Dc-Dc Converter	26
2.2.3 High Ripple Fourth-Order Boost Converter	30
2.2.3.1 State-Space Analysis	31
2.2.4 Low Source Current Ripple Fourth-Order Boost Converter	33
2.2.4.1 State-Space Analysis	35
2.3 Steady-State and Time-Domain Analysis of Fourth-Order Boost Converters	35
2.4 Results and Discussions	36
2.5 Conclusion	51

3	MODELING OF FOURTH-ORDER BOOST DC-DC CONVERTERS	53
3.1	Introduction	53
3.2	State-Space Averaging Modeling Method	54
3.3	Sampled-Data Model	56
3.3.1	Exact Discrete-Time Model	57
3.3.2	Approximate Discrete-Time Model	59
3.3.3	Improved Discrete-Time Model	60
3.4	Non-Linear Sampled-Data Model	64
3.4.1	Continuous Conduction Mode	64
3.5	Small-Signal Discrete-Time Model	65
3.6	Results and Discussion	67
3.7	Conclusion	75
4	DESIGN AND DYNAMICAL CHARACTERIZATION OF FOURTH-ORDER BOOST DC-DC CONVERTERS	77
4.1	Introduction	77
4.2	General Dynamic Representation	78
4.2.1	Small-Signal Characterizing Transfer Functions in Discrete-Time Domain	78
4.3	General Dynamical Characterization of Fourth-Order Boost Dc-Dc Converters	82
4.4	Origin of Up-Down Glitch in Frequency Response of Characterizing Transfer Functions	86
4.4.1	Factors Affecting the Up-Down Glitch	88
4.5	Design of Fourth-Order Boost Dc-Dc Converters	91
4.6	Small-Signal Characterization of Fourth-Order Boost Converters	92
4.6.1	Dynamical Characterization of Fourth-Order Boost Dc-Dc Converter	92
4.6.1.1	Analysis at Nominal Converter Parameters	92
4.6.1.2	Effect of Parameter Variations on Transfer-Function Poles and Zeros	94
4.6.2	Dynamical Characterization of Two-Inductor Boost Dc-Dc Converter	101
4.6.2.1	Analysis at Nominal Converter Parameters	101
4.6.2.2	Effect of Parameter Variations on Transfer-Function Pole-Zero location	102
4.6.2.3	Minimizing The Effect of Up-Down Glitch: Possible Solutions	103

4.6.3	Dynamical Characterization of Low Source Current Ripple Fourth-Order Boost Dc-Dc Converter	111
4.6.3.1	Analysis at Nominal Converter Parameters	111
4.6.3.2	Effect of Parameter Variations on Transfer-Function Pole-Zero location	112
4.7	Conclusion	116
5	OPTIMIZED POWER STAGE DESIGN OF FOURTH-ORDER BOOST DC-DC CONVERTERS	117
5.1	Introduction	117
5.2	Minimizing the Severity of Up-Down Glitch	119
5.3	Formulation of Optimization Problem	120
5.3.1	Optimization Constraints and Their Significance	121
5.4	Particle Swarm Optimization	123
5.5	Power Stage Design of Fourth-Order Boost Converters Using Particle Swarm Optimization	124
5.6	Direct-Digital Voltage-Mode Controller Design Using Pole-Placement Technique	134
5.6.1	Pole-Placement Technique	134
5.6.2	Controller Design for Fourth-Order Boost Converters	136
5.7	Conclusion	139
6	ROBUST DIGITAL VOLTAGE-MODE CONTROLLER DESIGN FOR FOURTH-ORDER BOOST DC-DC CONVERTERS	141
6.1	Introduction	141
6.2	Robust Control System	144
6.2.1	Representation of System Uncertainties	144
6.2.2	Robustness Quantification Indices	146
6.2.2.1	Stability Margins	146
6.3	Formulation of Sensitivity Functions for Voltage-Mode Controlled Dc-Dc Converters	148
6.3.1	Impact of Sensitivity Functions on Converter Robustness	150
6.3.1.1	Output Sensitivity and Complementary Sensitivity Function	151
6.3.1.2	Control Sensitivity Function	152
6.4	Quantitative Feedback Theory	161
6.4.1	Design Procedure For Quantitative Feedback Theory Based Robust	162

Digital Controllers For Higher-Order Dc-Dc Converters	
6.4.1.1 Selection of Frequency Array	162
6.4.1.2 Uncertainty Template Generation	162
6.4.1.3 Design Specification	163
6.4.1.4 Formulation of Bounds	163
6.4.1.5 Start-up Response	167
6.4.1.6 Formulation of Composite Bounds	167
6.4.1.7 Controller Design by Loop-Shaping	167
6.4.1.8 Pre-Filter Design	168
6.5 Quantitative Feedback Theory Based Robust Digital Voltage-Mode Controller Design For Fourth-Order Boost Dc-Dc Converter	169
6.5.1 Digital Controller Selection	171
6.5.2 Robust Controller Design	173
6.6 QFT Based Robust Digital Voltage-Mode Controller Design For FOBC TIBDC and LSCRFBC Designed Using Conventional Design Approach	180
6.6.1 Performance Specifications For Converter Design	180
6.6.2 Robust Controller Design	180
6.6.3 Performance Validation and Simulation Results	186
6.6.4 Pre-Filter Design	194
6.7 QFT Based Robust Digital Voltage-Mode Controller Design For Fourth-Order Boost Dc-Dc Converters Designed Using PSO Based Parameters	196
6.7.1 Robust Controller Design	196
6.7.2 Performance Validation and Simulation Results	201
6.7.3 Pre-Filter Design	208
6.8 Experimental Verification of Dynamic Performance And Robustness Range of Voltage-Mode Controlled Fourth-Order Boost Converters	210
6.8.1 Fourth-Order Boost Converter	213
6.8.2 Results For Fourth-Order Boost Converter Designed Using Conventional Design and Particle Swarm Optimization Based Design	219
6.8.3 Experimental Results For Two-Inductor Boost Dc-Dc Converter	225
6.8.4 Experimental Results For Low Source Current Ripple Fourth-Order Boost Dc-Dc Converter	231
6.9 Conclusion	238

7 ROBUST DIGITAL TWO-LOOP CURRENT-MODE CONTROLLER DESIGN FOR FOURTH-ORDER BOOST CONVERTERS	239
7.1 Introduction	239
7.2 Formulation of Sensitivity Functions for Current-Mode Controlled Dc-Dc Converters	241
7.2.1 Impact of Control Sensitivity Function in Robust Controller Design for Current-Mode Controlled Converters	243
7.3 Quantitative Feedback Theory Based Robust Digital Average Current-Mode Controller Design For Fourth-Order Boost Converters	247
7.4 QFT Based Robust Digital Average Current-Mode Controller Design For Two-Inductor Boost Dc-Dc Converter Designed Using Conventional Design Approach	248
7.4.1 Inner-Loop Controller Design	249
7.4.2 Outer-Loop Controller Design	250
7.4.3 Simulation Results And Discussions	255
7.5 QFT Based Robust Digital Average Current-Mode Controller Design For FOBC and LSCRFBC Designed Using Conventional Design Parameters	260
7.5.1 QFT Based Inner-Loop Controller Design	260
7.5.1.1 Performance Validation and Simulation Results for Inner Loop Design	261
7.5.2 Controller Design for Outer-Loop	263
7.5.2.1 Performance Validation and Simulation Results for Outer-Loop Design	265
7.5.3 Pre-Filter Design	269
7.6 QFT Based Robust Average Current-Mode Controller Design For Fourth-Order Boost Dc-Dc Converters with PSO Based Design Parameters	269
7.6.1 Controller Design for Inner-Loop	269
7.6.1.1 Performance Validation and Simulation Results for Inner Loop Design	271
7.6.2 Outer-Loop Controller Design	274
7.6.2.1 Performance Validation and Simulation Results for Outer-Loop Design	278
7.6.3 Pre-Filter Design	283
7.7 Experimental Verification of Dynamic Performance And Robustness Range Current-Mode Controlled Fourth-Order Boost Converters	283
7.7.1 Two Inductor Boost Converter	285
7.7.2 Fourth-Order Boost Converter	298

7.7.3	Low Source Current Ripple Fourth-Order Boost Converter	306
7.8	Conclusions	309
8	DIGITAL DEADBEAT CONTROLLER FOR FOURTH-ORDER BOOST CONVERTER	311
8.1	Introduction	311
8.2	Small-Signal Discrete-Time Model For Control-to-Inductor Current Based On Sampled Data Model	313
8.3	Design of Digital Deadbeat Controller	317
8.3.1	Theory of Digital Deadbeat Control	317
8.3.2	Design of Deadbeat Controller For Inductor-1 Current of Fourth-Order Boost Dc-Dc Converters	318
8.4	Online Estimation of Inductance	319
8.5	Results and Discussions	321
8.6	Conclusions	329
9	CONCLUSION AND FUTURE WORK	331
9.1	Conclusions	331
9.2	Future Scope of Work	333
	REFERENCES	335
	APPENDICES	359
A	STATE-SPACE AND TIME-DOMAIN ANALYSIS OF FOURTH-ORDER BOOST CONVERTERS	359
A.1	Fourth-Order Boost Dc-Dc Converter	359
A.1.1	State-Space Analysis	359
A.1.2	Time-Domain Analysis	360
A.2	Two-Inductor Boost Dc-Dc Converter	362
A.2.1	State-Space Analysis	362
A.2.2	Time-Domain Analysis	363
A.3	High Ripple Fourth-Order Boost Dc-Dc Converter	364
A.3.1	State-Space Analysis	364
A.3.2	Time-Domain Analysis	365
A.4	Low Source Current Ripple Fourth-Order Boost Dc-Dc Converter	366
A.4.1	State-Space Analysis	366

B	SMALL-SIGNAL DISCRETE-TIME MODELS FOR FOURTH-ORDER BOOST CONVERTERS	369
B.1	Small-Signal Discrete-Time Model For Triangular Edge Modulation With On-Time Sampling	369
C	GENERALIZED EXPRESSION FOR SHIFTING RHP ZERO OF TIBDC TO LHP	373
D	GENERALIZED EXPRESSION OF CONTROL-TO-INDUCTOR CURRENT OF FOBC IN PRESENCE OF PARASITICS AND CONDITION FOR ZERO STEADY-STATE ERROR IN FINITE TIME	374
D.1	Generalized Expression of Control-to-Inductor Current of FOBC	374
D.2	Condition for Zero Steady-State Error in Finite Time	375

PUBLICATIONS

BIO-DATA