ANALYSIS, DESIGN AND DEVELOPMENT OF ROBUST DIGITAL CONTROLLERS FOR FOURTH-ORDER BOOST DC-DC CONVERTERS

by

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CERTIFICATE

This is to certify that the thesis entitled "**ANALYSIS, DESIGN AND DEVELOPMENT OF ROBUST DIGITAL CONTROLLERS FOR FOURTH-ORDER BOOST DC-DC CONVERTERS**" being submitted by **Mr. Anmol Ratna Saxena** for the award of degree of **Doctor of Philosophy** is a record of a bonafide research work carried out by him in the Department of Electrical Engineering of Indian Institute of Technology, New Delhi.

Mr. Anmol Ratna Saxena worked under my guidance and supervision and has fulfilled the requirement for the submission of the thesis, which to my knowledge has reached the requisite standards. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any Degree or Diploma.

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Date: September 2013 **Anmol Ratna Saxena**

ABSTRACT

In this thesis, non-isolated fourth-order boost dc-dc converter topologies that are obtained by structural rearrangement of boost converter with output filter are analyzed with the aim of evolving a fourth-order boost topology, exhibiting low source current ripple together with low overall inductance requirement, improved dynamic response and satisfying other steady-state requirements. Discrete-time models that are considered to be more accurate than averaged model are formulated for fourth-order boost converters and used to derive small-signal discrete-time transfer functions, which characterize the dynamical behavior of these converters. Discrete-time models formulated in this thesis takes into account the effect of sampling instant, PWM modulation and delay in control loop and used to facilitate the controller design and analyze the converter stability with voltage-mode and current-mode control. Non-linear sampled data models have also been derived from the exact discrete-time model for continuous conduction mode of operation.

It is shown through discrete-time analysis that the presence of additional energy storage elements as compared to conventional boost converter increases the complexity in control loop design. Particularly, dynamic response improvement becomes a challenging task which is on account of successive multiple complex-conjugate pole-zero pattern, which forms an up-down glitch in the small-signal characterizing transfer functions of fourth-order boost converters. The implications this up-down glitch on dynamic performance of the converters is addressed and factors affecting the shape of the up-down glitch are brought out. Safety margin is proposed as an additional design specification which along with gain margin and phase margin must be used to judge the stability of fourth-order converters. A generalized optimization procedure, using particle swarm optimization, with a possibility to extend for other higher-order topologies is proposed to

resolve the contradictory issues of steady-state and dynamic performance requirements in fourth-order dc-dc converters.

Controllers for point of load converters, either for voltage-mode control or current-mode control are designed to regulate the load voltage against small disturbances around their steady-state operating points. However, there are certain factors which are classified as structured and unstructured uncertainties, that not only degrade the converter performance over due course of time but even tend to make them unstable in some cases. Therefore, robust digital voltage-mode and current-mode controllers are designed for fourth-order boost converters using Quantitative Feedback Theory (*QFT*) which takes into account the effect of these uncertainties. A modified loop shaping approach is proposed for controller design, wherein controller designed using pole-placement approach is used to initiate loop-shaping in *QFT GUI* environment. A robust digital deadbeat controller is proposed for fourth-order boost converters, where inductance estimation is done online by taking only one sample in one switching period and then control law is updated in every switching cycle based on the estimated value of inductance. The dynamic performance and robustness range of the converters against structured and unstructured uncertainties is verified experimentally on 12-to-28 *V*, 30 *W* laboratory prototypes of the converters and shows that experimental results are inline with the simulation and analytical design studies made in the thesis.

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