DESIGN OF WIRELINE COMMUNICATION RECEIVERS FOR MULTI-GIGABIT DATA RATES

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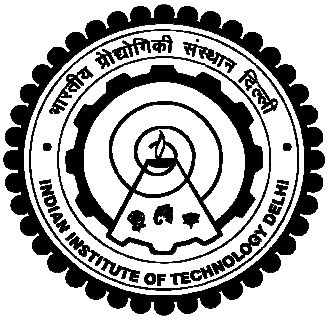

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DESIGN OF WIRELINE COMMUNICATION RECEIVERS FOR MULTI-GIGABIT DATA RATES.

by

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Department of Electrical Engineering

Submitted

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Certificate

This is to certify that the thesis entitled ***"Design of wireline communication receivers for multi-gigabit data rates."***, being submitted by **Mr. Sushrant Monga** to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of **Doctor of Philosophy** and is a record of the original bonafide research work carried out by him under my guidance and supervision. The results contained in the thesis have not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

I certify that he has pursued the prescribed course of research.

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– Sushrant Monga

Abstract

Contributions to the architecture and modeling of high speed serial link transceivers are presented in this thesis. Basically three contributions are described that address the issues of jitter and intersymbol interference in the receiver at gigabit data rates. Design proposals (modeling and CMOS implementation) specifically for termination impedance at the transmitter and the receiver, equalizer and clock and data recovery circuits for gigabit receiver are presented.

The thesis presents an adaptive transmitter designed in 40 nm CMOS that calibrates its termination impedance to the characteristic impedance of the channel that ensures a low Bit Error Rate (BER) across external variables independent of operating conditions (process, voltage and temperature). The design presents digital calibration of the termination over an impedance range of $30\ \Omega$ - $120\ \Omega$ with an accuracy of ($\leq\ 8\ \%$). These digital calibration codes are also distributed to the receiver for the calibration of receiver's termination assuming the common architecture for the impedance design. The calibration scheme enables the transmitter to function as a plug-n-play device across multiple environments. Mathematical formulation for the problem of impedance matching in practical scenarios is presented thereby developing the proposed solution for dynamic impedance calibration. Simulation results for the implemented system are presented showing the respective waveforms with a total power consumption for the receiver to be 20 mW @2.5 V in contrast to other reported results.

A single tap CMOS continuous-time feedback equalization is proposed as a solution to

solve the latency issues in decision feedback equalization (DFE). The architecture avoids the use of synchronous blocks having a continuous feedback loop with controlled transconductance in the feedback path that gives the required delay for the desired operation of the loop. The equalizer is designed in 130 nm CMOS and is scalable across technologies. The measurement results show effective equalization with little area and power overhead. Post-simulation and measurement results indicate a minimum equalization gain (for the default setting of the digital calibration in the equalizer) of 5 dB(min.) at a frequency of 2.98 Ghz (almost 3 Ghz) for data rates approaching 6 Gb/s.

In this thesis a clock and data recovery (CDR) architecture is presented to enhance the jitter tolerance to the input data thus ensuring a lower BER for multiple data rates. A hybrid architecture with open-loop and closed-loop clock recovery schemes is presented. The results for the behavioral model for the CDR show high jitter tolerance for the input with random jitter (RJ= 2.264 ps) in addition to the deterministic jitter (DJ= 30 ps pk-pk) superimposed with the sinusoidal jitter components such that the total data jitter reaches 64% of the data-eye. The clock trajectory (in time) for the behavioral model of the proposed CDR is shown respect to the state-of-art CDR's (open-loop and closed loop recovery architectures). The simulation results for CMOS 65nm design are presented for the input data having RJ=0.01 UI_{rms} and DJ = $0.2UI_{pp}$. Simulation results are also presented for the input data (to the CDR) having only the residual ISI (output of the cascade of the channel and CTFE) and no other source of jitter to show the functioning of the respective blocks.

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