MODELING AND SIMULATION OF SELF-HEATING EFFECTS IN SUB-14NM CMOS DEVICES

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MARCH 2019

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by

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Submitted

in fulfilment of the requirements of the degree of Doctor of Philosophy

to the

INDIAN INSTITUTE OF TECHNOLOGY DELHI

MARCH 2019

Certificate

This is to certify that the thesis entitled ***"Modeling and simulation of self-heating effects in advanced silicon multiple-gate field-effect transistors"***, being submitted by **Ishita Jain** to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of **Doctor of Philosophy** and is a record of the original bonafide research work carried out by him under my guidance and supervision. The results contained in the thesis have not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

I certify that she has pursued the prescribed course of research.

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Declaration of Authorship

I, Ishita Jain, declare that this thesis entitled ***"Modeling and Simulation of Self-Heating Effects in Advanced Silicon Multiple-Gate Field-Effect Transistors"*** and the work presented in it is my own. I confirm that

- This degree has been done completely while in candidature for a research degree in this University.
- If any part of this thesis has perviously been submitted for a degree or any other qualification in this University or any other institution, this has been clearly stated.
- Whatever the published work of others have consulted, I have mentioned it clearly.
- The quotation of other's work has been referenced. With the exception of those quotes, this thesis is entirely my own work.
- I have acknowledged all the main sources of help.
- This thesis is based on work done by myself and with other's support as well, which I have mentioned it clearly.

Signed:

Date:

Acknowledgments

"The journey is what brings us happiness not the destination: Dan Millman". The Ph.D. journey for me will always remain a cherish experience for a lifetime.

Without the support of these people, this thesis would not have been possible. Firstly, I express my deepest gratitude to my supervisor Prof. Abhisek Dixit for the continuous support through my PhD studies. His motivation and immense knowledge always enhanced my research abilities throughout the course of learning. His guidance helped me in all the time of research and the writing of this thesis.

Besides my advisor, I would like to thank the committee members Prof. Bhaskar Mitra, Prof. Manan Suri and Prof. Smuriti Sarangi for their useful inputs. A special thanks to Prof. Mamidala Jagadesh Kumar for free ranging discussions on various topics.

I would like to thank the Department of Science and Technology, Govt. of India, for the instrumentation setup for the Device and Wafer Level Characterization Laboratory (DWLCL), through Science and Engineering Research Board (SERB), under grant SB/S3/EECE/037/2014 and through TSG, under grant DST/TSG/AMT/2015/339 (General).

I would also like to thank our industry collaborator Terence Hook in IBM Research Group from Albany, USA, for his valuable and expert comments.

I thank the past and the present graduate students of VDTT, VLSI, and laboratories of the department of electrical engineering; Anil, Ramendra, Anshul, Charu, Kritika, Chandan, Manoj, Shivendra and Pritam. I would like to acknowledge Anil and Ramendra for their technical inputs during the measurement of chips. I would like to acknowledge Anil, Ramendra and Anshul for their help during the characterization and simulation of these devices. I am thankful to them for long technical discussions which made me learn the subject comprehensively.

Apart part from my colleagues, I am thankful to my seniors Dr. Gajendranath Chowdhary, and Dr. Hitesh Shirmali who motivated me for the focused research by sharing their research-experiences.

I want to thank my M. Tech. friends, Arpit, Arathy, Neelima, Shruti, Kranthi, Surya, Ravi for motivating me to opt for higher studies.

To Siddharth, Ketan, Amit for their concerns, encouragement, and unconditional support. I am thankful to God for those moments with them and hope to have their presence for always and always in my life. *"Hope is a good thing, maybe the best of things, and no good thing ever dies.....:The Shawshank Redemption"*.

Last, but not the least, I express my deep heartfelt gratitude to my Acharya guruvar 108 Shree Vidyasagarji maharaj ji and my respected parents, Smt.Meenal Jain and Shri.Sanjay Jain for their blessings and supporting me spiritually throughout writing this thesis. Special thanks to my sisters Shuchita and Deeksha for their support and understanding.

I tried to express my gratitude, however, *The most important things are the hardest to say, because words diminish them: Stephen King"*.

Abstract

Multiple-gate transistors (MuGFETs) are perceived as the feasible solution to extreme downscaling of CMOS technology in comparison to planar bulk and other contemporary CMOS technologies. Compared to a planar MOSFET, MuGFETs can achieve better electrostatic control and higher drive capability for a given layout area at a given power consumption. As we go beyond 14nm technology node, several challenges such as lithography, variability, electromigration margins, parasitics, and electrostatic discharge (ESD) come in picture for ultra-large integration of these devices. These devices also suffer from self-heating effects (SHE) due to low thermal conductivity of materials, high conduction current densities, and the physical confinement of device geometries.

In this thesis, a series resistance based issue for stacked-nanowire FETs has been discussed. This thesis also presents 3-D device simulations to analyze thermal effects in FinFETs and stacked-nanowire FETs. Based on empirically extracted equations, a new model for the thermal resistance estimation is proposed, which takes into account the aggregate impact of various device parameters such as number of fins, number of gate fingers, number and dimensions of stacked nanowires. The results show that the model may be useful for estimation of thermal resistance in FinFETs and nanowire FETs with large layouts.

Heating effects are undesirable for CMOS integrated circuits due to change in electrical behaviour of devices with temperature. MOSFET channel mobility degrades as local temperature increases, which leads to slowing down in switching circuits. Such a rise in temperature can be due to SHE or even from other neighbouring devices, such as resistors or other MOSFETs. In order for the generated heat to flow out to the contact pads, it has to pass through length and width of various materials and interfaces. Only an accurate determination of all the thermal resistivities can make calculation of contact thermal resistance. Thermal resistivity of a given layer of material differs more and more from its bulk value as the layer is thinned down. Due to continuous front and back-end technology scaling, estimation of thermal resistivities

of thin material layers and their interfaces has become even more challenging. In a switching circuit involving MOSFETs, heat is continuously generated and dissipated, thus giving rise to a thermal capacitance related to heat transfer inertia of the device under test (DUT). Like the thermal resistance (Rth), thermal capacitance (Cth) is also layout and process technology dependent. Together Rth and Cth determine a thermal time constant (τth) of the DUT. If the switching frequency falls in the range of τth, undesired heating effects will be present. Thus in order to ascertain operability of a DUT in sub-14nm CMOS technology, accurate layout and process dependent models of Rth and Cth are critically required.

Goal of this work is to enable accurate simulation of thermal effects for circuit designers so that layouts can be optimized. This requires inclusion of thermal effects in process design kit (PDK) through SPICE based compact models. However, electro thermal measurements required for model parameter extraction is a complex task. Lack of sufficient number of specific test structures is a limitation for sub-14nm advanced technology nodes. This problem could be solved by the use of TCAD, which requires limited calibration of TCAD models to measurement data and then use of TCAD to simulate both SHE and heat dissipation for various layouts and processes.

सार

आज कल प्लानर बल्क सिमोस की तुलना में मल्टीप्ल-गेट ट्रांसिस्टर्स एक नया विकल्प बनता जा रहा है जैसे- जैसे सिमोस स्केलिंग बढ़ती जा रही है |प्लानर मॉसफेट्स की तुलना में, किसी दिए हुए लेआउट के एरिये के लिए एवं कांस्टेंट पावर सेवन के लिए मग्फेट्स का इलेक्ट्रोस्टेटिक कण्ट्रोल अधिक अच्छा है | १४ नैनोमीटर के आगे, बहुत-सी चुनौतियां सामने आने लगती है जैसे - लिथोग्राफी, वरिएबिलिटी, इलेक्ट्रोस्टेटिक डिस्चार्ज, एलेक्ट्रोमीग्रैशन मार्जिन्स, परसिटिक्स आदि- आदि| इन उपकरण में सेल्फ-हीटिंग इफ़ेक्ट भी हुआ करता है जिसका कारन कम ऊष्मीय चालकता वाले मैटेरियल्स का प्रयोग, ज्यादा चालन वर्तमान घनत्व, उपकरण क्षेत्र का कम होना |

इस थीसिस में सबसे पहले सीरीज रेजिस्टेंस पर आधारित एक प्रॉब्लम पर प्रकाश डाला गया है | इस थीसिस में 3-डी सिम्युलेशन्स का प्रयोग करके फिनफिट्स और नैनोवायर फेट्स पर विश्लेषण किया गया है| एम्पिरिकल एक्सट्रेक्टेड एक्वेशन्स के आधार पर, एक नया मॉडल थर्मल रेजिस्टेंस के अनुमान के लिए दिया जा रहा है, जिसमें विभिन्न उपकरण के पैरामीटर्स जैसे - फिन्स की संख्या, फिंगर्स की संख्या, नैनोवायर की संख्या एवं उसका व्यास आदि का प्रभाव कैसे होता है और क्यों होता है, इस पर ध्यान व् प्रकाश डाला गया है | इसके परिणाम के फलस्वरूप, ये मॉडल बड़े- बड़े लेआउट्स के थर्मल रेजिस्टेंस के अनुमान के लिए काफी उपयोगी सिद्ध होता प्रतीत होता है|

सिमोस उपकरण में हीटिंग इफेक्ट्स के कारन इलेक्ट्रिकल इफेक्ट्स पर अवांछनीय परिणाम सामने आते है| इलेक्ट्रिकल बिहेवियर तापमान के बढ़ने से बदल जाता जाता है जिससे उस उपकरण का सही उपयोग संभव नहीं हो पाता| मॉस्फेट की चैनल मोबिलिटी कम हो जाने से, सर्किट्स की गति धीमी पढ़ जाती है| ये तापमान बढ़ने का कारन सेल्फ-हीटिंग इफ़ेक्ट या दूसरे अन्य आस-पास के उपकरण होते है, जिनके कारन हीट बाहर निकल नहीं पाती| इसलिए, हीट को संतुलित तरीके से बाहर निकलने के लिए बहुत से मैटेरियल्स और उनके इंटरफेसेस के बीच होकर गुज़ारना पड़ता है| जो सीधे कॉन्टेक्ट्स पैड्स के माध्यम से बाहर निकलती है | एक स्विचन सर्किट में हीट निरंतर उत्पन्न और नष्ट होती रहती है, जिससे थर्मल कपसिटंस की उत्पत्ति होती है|

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$\#\mathbf{NW}$	Number of nanowires in the stack
$\mathbf{D_{fin}}$	Fin width
$\mathbf{D_{NW}}$	Nanowire diameter
$\mathbf{H_{fin}}$	Fin height
$\mathbf{N_{finger}}$	Number of gate fingers
$\mathbf{N_{fin}}$	Number of fins
$\mathbf{R_{th}}$	Effective thermal resistance

List of Abbreviations

BEOL	Back End Of Line
CMOS	Complementary Metal Oxide Semiconductor
FEOL	Front End Of Line
MOL	Mid Of Line
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NWFET	Nanowire Field Effect Transistor
PPA	Power Performance Area
SDE	Sentaurus Structure Editor
SHE	Self Heating Effect
SOI	Silicon On Insulator
TCAD	Technology Computer Aided Design