POWER MANAGEMENT CIRCUITS FOR ENERGY-HARVESTING SYSTEMS

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by

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Submitted

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to the



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To my beloved family members
Shri Rajesh Bansal, Shri Shubham Bansal, and Shrimati Manju Bansal

DECLARATION

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Raghav Bansal

Abstract

The thesis showcases power management circuits for energy-harvesting systems. The contributions of the thesis are as follows:
AC-DC power conversion techniques for energy harvesting from piezoelectric transducer: Phase-locked loop (PLL)-based rectifier-less power switching converter, multi-step charge transfer interface circuit, and CMOS-only undervoltage lockout circuit with dual mode operation.
Ultra-low-power reference circuits: Dual loop self-regulated CMOS-only voltage reference and a single BJT-based voltage and current references.
Nanoampere-level quiescent current low dropout regulators: A gm-boosted flipped-voltage-follower (FVF) based output-capacitor-less LDO with fast transient response and a multi-feedback-loop LDO.
A sub-1V LDO with built-in single BJT-based bandgap reference.
A multi-loop LDO with integrated single-BJT voltage and current references.

A PLL-based rectifier-less interface circuit is proposed to control the power switches for harvesting energy from a low-voltage piezoelectric transducer, with input power levels ranging from 100 nW to 40 μW. In this method, the charge-pump PLL is first locked to the piezoelectric energy harvester (PEH) input frequency to detect the PEH's peak output voltage, thereby maximizing power extraction. Once locked, power transfer occurs with the PLL operated in open loop (only the voltage-controlled oscillator (VCO) is functional) to minimize power loss. In 180 nm CMOS technology, the power switching converter was designed to extract power with a minimum piezoelectric open-circuit voltage of 0.17 V. At an input power of 10 μW and a vibration frequency of 88 Hz, it achieves a maximum power efficiency of 84$\%$. To extract the maximum available input power from a piezoelectric energy harvester, a highly power-efficient interface circuit based on a multi-step charge transfer (MSCT) technique is proposed. The MSCT approach pre-charges the piezoelectric capacitance, flips the piezoelectric output voltage, and extracts the stored charge in multiple stages. This technique enhances the end-to-end power efficiency of the rectifier by reducing conduction losses in the power converter stage while extracting the maximum possible stored energy from the piezoelectric intrinsic capacitance for a given CMOS process. The proposed rectifier is designed and simulated in a 0.18-μm CMOS process. Under the same input power conditions, the rectifier extracts 14.39 μW and 16.34 μW of output power with one-step and four-step charge transfer, respectively. The MSCT achieves maximum power efficiencies of 68.5% with a 47 μH inductor and 83% with a 220 μH inductor. Simulation results demonstrate that the MSCT

technique with four steps yields a 13.85% enhancement in power efficiency relative to single-step charge transfer. For reliable operation of the interface circuit, a charge-monitor circuit, also known as under-voltage lockout, is required. An ultra-low-power, CMOS-only undervoltage lockout (UVLO) circuit is proposed for energy-harvesting applications. The proposed UVLO operates in a dual-mode configuration, which is essential for energy-autonomous power-switching converters, while consuming significantly less area and power than conventional bandgap-based UVLOs that require multiple resistors and BJTs. The design is fabricated in a 0.18 μm CMOS technology and occupies an active area of 0.0066 mm^2. The measured low-to-high trip voltage ($LHTV_1$) and high-to-low trip voltage ($HLTV_1$) for the first mode are 1.362 V and 1.018 V, respectively, while the $LHTV_2$ and $HLTV_2$ for the second mode are 1.608 V and 1.492 V, respectively. The circuit consumes a quiescent current (I_Q) of 300 pA at room temperature under a 1.8 V supply.

To achieve ultra-low-power operation and occupy a small area, energy-efficient and area-efficient reference circuits are proposed. A picowatt CMOS-only voltage reference (VR) that improves the line sensitivity (LS) using a dual self-regulation circuit while consuming a small area and power. The proposed design has been implemented in a 65 nm CMOS low power (LP) process and occupies an active area of 1373 μm^2. The post-layout Monte Carlo simulation shows that the circuit gives an average reference voltage of 287 mV and a standard deviation of 10.32 mV. The line sensitivity is 0.59%/V across the supply voltage range from 0.5 V to 1.2 V, and it drops to 0.036%/V when the power supply sweeps from 0.8 V to 1.2 V. The circuit consumes 70 pA of quiescent current from a 0.5 V supply at room temperature. To generate a reference voltage and current that are insensitive to process variations, a single bipolar junction transistor (BJT)-based voltage-current reference (VCR) is proposed, combining both in a single circuit. In the proposed design, a β-multiplier produces a proportional-to-absolute-temperature (PTAT) voltage, which is summed with a fractional BJT emitter-base voltage (V_{EB}) having complementary-to-absolute-temperature characteristics, to obtain a temperature-compensated reference voltage (V_{REF}). The reference current (I_{REF}) is obtained from the ratio of V_{REF} to a temperature-compensated resistor (TCR), implemented as a series connection of a CTAT unsilicided P+ poly resistor and a PTAT N-well resistor. The proposed circuit is implemented in a 65-nm CMOS technology and occupies an area of 0.1 mm^2. Results from post-layout Monte Carlo simulations demonstrate that V_{REF} and I_{REF} achieve average temperature coefficients of 13.9 ppm/°C and 83.85 ppm/°C, respectively, over the temperature range of -40 °C to 120 °C. The average V_{REF} and I_{REF} values are 243.34 mV and 9.97 nA, with standard deviations of 2.49 mV and 454 pA, respectively. The circuit operates from a 0.85 V supply and consumes 113 nW power at 120 °C.

Furthermore, the power management unit (PMU) is designed for energy-efficient applications that demand an ultra-low I_Q low dropout regulator (LDO) to provide a clean and regulated supply for a wide range of load currents. In this thesis, an ultra-low quiescent output-capacitor-less low-dropout regulator (OCL-LDO) with enhanced load regulation is proposed. The LDO architecture is based on a FVF topology, where the Gm stage with a current-mirror load replaces the constant-current source of the folded-cascode common-gate amplifier to improve DC load regulation and transient performance. A super-source follower (SSF), which acts as a voltage buffer, is inserted

to drive the high-power transistor. Furthermore, a dynamic sensing unit is utilized to achieve a fast settling time during a low-to-high load step. In a 65 nm low-power CMOS process, the proposed LDO was designed. The LDO consumes 95 nA of quiescent current and can deliver up to 50 mA of load current with a 1.2 V supply and a 1 V regulated output. It achieves a DC load regulation of 14.8 mV/A by varying the load current from 500 nA to 50 mA. With a 100 pF load capacitor, the output voltage undershoot is 626 mV with a 100 ns rise time and reduces to 530 mV with a 200 ns rise time for a full-load-step current, settling within 350 ns. To achieve the best trade-off among quiescent current, area, and other LDO parameters, especially line/load regulation, settling time, and maximum load current, an ultra-low-power, output-capacitor-less low-dropout regulator (OCL-LDO) with a multiple-feedback loop (MFL) is proposed. The proposed LDO comprises five feedback loops that deliver excellent steady-state and transient performance. A tri-loop FVF stage enhances both line and load regulation. The slew-rate enhancement loop based on a source cross-coupled error amplifier (SXCEA) provides a fast transient response. Moreover, the proposed LDO utilizes a dynamic feedback loop that significantly improves undershoot recovery time during the full-load step current. The proposed LDO was fabricated in a 65-nm CMOS node with an active area of 0.025 mm^2. The LDO can deliver a maximum of 50 mA load current at a 1 V output voltage and consume only 22 nA measured quiescent current. The measurement results show that the proposed LDO achieves a load regulation of $0.004\ mV/mA$ and a low-frequency power supply rejection (PSR) at full load of -63.5 dB. For a load current step from 200 nA to 50 mA with a 10 ns edge time, the measured voltage undershoot is 574 mV and settles within 200 ns.

To further reduce overall area and power consumption, a fully integrated, low-power, low-voltage, low-dropout regulator is proposed that shares the feedback resistors of the LDO with a single BJT-based voltage reference. The proposed architecture uses only one BJT and two resistors to generate a temperature-compensated, regulated output voltage, unlike conventional reference-integrated voltage regulators, which require multiple BJTs and resistors. Additionally, by reducing the V_{EB} of the BJT to half its value using a voltage divider circuit, the design achieves sub-1V operation. Hence, the proposed LDO offers both area and power efficiency. The proposed architecture was fabricated in a 65-nm low-power CMOS node and occupies a die area of 0.017 mm^2. The LDO delivers a maximum load current of 10 mA at a nominal output voltage of 0.608 V. Measurement results show that the LDO achieves a temperature coefficient (TC) of 26.2 ppm/°C from $-40\,^{\circ}C$ to $120\,^{\circ}C$, and a voltage precision of $0.499\,\%$. The measured line regulation and load regulation are 3.925 mV/V and 0.12 mV/mA, respectively. The LDO consumes 241 nW of power with a minimum supply voltage of 0.8 V.

To achieve an optimal trade-off among small silicon area, low power consumption, and excellent LDO performance metrics, a fully integrated output-capacitor-less (OCL) multi-feedback-loop low-dropout regulator (LDO) with an in-built single bipolar junction transistor (BJT)-based voltage and current reference is proposed for energy-harvesting applications. The proposed architecture comprises four loops, which significantly enhance the DC regulation and transient performance of the LDO. A tri-loop regulation core based on a flipped-voltage-follower (FVF) structure offers high DC loop gain, resulting in enhanced line and load regulation. A replica-based slew-

rate enhancement (RSRE) loop improves the undershoot and overshoot recovery times during load transient response. Furthermore, the proposed LDO consumes less area and power, and exhibits reduced output noise by integrating a single BJT branch bandgap reference (BGR) with an FVF power stage, unlike conventional LDOs that use externally connected BGRs, which require multiple resistors and BJTs. The bias current is generated internally by a proposed current reference based on a shared single BJT and is powered by the LDO output voltage to improve current line sensitivity. The proposed design is fabricated in a 65-nm low-power CMOS technology and occupies an area of 0.041 mm^2. Measurement results show that the proposed LDO achieves line and load regulation of 0.66 mV/V and 0.195 mV/mA, respectively. The measured power supply rejection (PSR) at 10 Hz is 67.5 dB at maximum load current. The proposed LDO consumes a 268 nA quiescent current at room temperature with a minimum supply voltage of 1.3 V.

सारांश

यह थीसिस एनर्जी-हार्वेस्टिंग सिस्टम के लिए पावर मैनेजमेंट सर्किट के बारे में है। इस थीसिस में किए गए काम इस प्रकार हैं:
पीज़ोइलेक्ट्रिक ट्रांसड्यूसर से एनर्जी हार्वेस्टिंग के लिए AC-DC पावर कन्वर्ज़न तकनीकें: फेज़-लॉक्ड लूप (PLL) पर आधारित रेक्टिफायर-लेस पावर स्विचिंग कन्वर्टर, मल्टी-स्टेप चार्ज ट्रांसफर इंटरफेस सर्किट, और डुअल मोड ऑपरेशन वाला CMOS-ओनली अंडरवोल्टेज लॉकआउट सर्किट।
अल्ट्रा-लो-पावर रेफरेंस सर्किट: डुअल लूप सेल्फ-रेगुलेटेड CMOS-ओनली वोल्टेज रेफरेंस और सिंगल BJT-आधारित वोल्टेज और करंट रेफरेंस।
नैनोएम्पीयर-लेवल क्विसेंट करंट वाले लो ड्रॉपआउट रेगुलेटर: तेज़ ट्रांजिएंट रिस्पॉन्स वाला g_m-बूस्टेड फ्लिप-वोल्टेज-फॉलोअर (FVF) आधारित आउटपुट-कैपेसिटर-लेस LDO और मल्टी-फीडबैक-लूप LDO।
इन-बिल्ट सिंगल BJT-आधारित बैंडगैप रेफरेंस वाला सब-1V LDO।
इंटीग्रेटेड सिंगल-BJT वोल्टेज और करंट रेफरेंस वाला मल्टी-लूप LDO।

कम-वोल्टेज वाले पीज़ोइलेक्ट्रिक ट्रांसड्यूसर से एनर्जी हार्वेस्ट करने के लिए पावर स्विच को कंट्रोल करने हेतु एक PLL-आधारित रेक्टिफायर-लेस इंटरफेस सर्किट का प्रस्ताव दिया गया है, जिसमें इनपुट पावर लेवल 100 nW से 40 µW तक होता है। इस तरीके में, चार्ज-पंप PLL को पहले पीज़ोइलेक्ट्रिक एनर्जी हार्वेस्टर (PEH) की इनपुट फ्रीक्वेंसी के साथ लॉक किया जाता है ताकि PEH के पीक आउटपुट वोल्टेज का पता लगाया जा सके और इस तरह ज़्यादा से ज़्यादा पावर निकाली जा सके। एक बार लॉक हो जाने पर, पावर लॉस को कम करने के लिए PLL को ओपन लूप (केवल वोल्टेज-कंट्रोल्ड ऑसिलेटर (VCO) काम करता है) में चलाकर पावर ट्रांसफर किया जाता है। 180 nm CMOS टेक्नोलॉजी में, पावर स्विचिंग कन्वर्टर को कम से कम 0.17 V के पीज़ोइलेक्ट्रिक ओपन-सर्किट वोल्टेज के साथ पावर निकालने के लिए डिज़ाइन किया गया था। 10 µW की इनपुट पावर और 88 Hz की वाइब्रेशन फ्रीक्वेंसी पर, यह 84% की अधिकतम पावर दक्षता हासिल करता है। पीज़ोइलेक्ट्रिक एनर्जी हार्वेस्टर से उपलब्ध अधिकतम इनपुट पावर निकालने के लिए, मल्टी-स्टेप चार्ज ट्रांसफर (MSCT) तकनीक पर आधारित एक अत्यधिक पावर-एफिशिएंट इंटरफेस सर्किट का प्रस्ताव दिया गया है। MSCT तरीका पीज़ोइलेक्ट्रिक कैपेसिटेंस को प्री-चार्ज करता है, पीज़ोइलेक्ट्रिक आउटपुट वोल्टेज को फ्लिप करता है, और कई चरणों में जमा चार्ज को निकालता है। यह तकनीक पावर कन्वर्टर स्टेज में कंडक्शन लॉस को कम करके रेक्टिफायर की एंड-टू-एंड पावर एफिशिएंसी को बढ़ाती है, साथ ही किसी खास CMOS प्रोसेस के लिए पीज़ोइलेक्ट्रिक इंट्रिन्सिक कैपेसिटेंस से ज़्यादा से ज़्यादा स्टोर्ड एनर्जी निकालती है। प्रस्तावित रेक्टिफायर को 0.18-µm CMOS प्रोसेस में डिज़ाइन और सिम्युलेट किया गया है। एक ही इनपुट पावर कंडीशन में, रेक्टिफायर क्रमशः वन-स्टेप और फोर-स्टेप चार्ज ट्रांसफर के साथ 14.39 µW और 16.34 µW आउटपुट पावर निकालता है। MSCT, 47 µH इंडक्टर के साथ 68.5% और 220 µH इंडक्टर के साथ 83% की अधिकतम पावर एफिशिएंसी हासिल करता है। सिमुलेशन के नतीजे बताते हैं कि सिंगल-स्टेप चार्ज ट्रांसफर की तुलना में चार-स्टेप वाली MSCT तकनीक से पावर एफिशिएंसी में 13.85% की बढ़ोतरी होती है। इंटरफ़ेस सर्किट के भरोसेमंद ऑपरेशन के लिए, एक चार्ज-मॉनिटर सर्किट की ज़रूरत होती है, जिसे अंडर-वोल्टेज लॉकआउट भी कहा जाता है। एनर्जी-हार्वेस्टिंग एप्लीकेशन के लिए एक अल्ट्रा-लो-पावर, सिर्फ़ CMOS वाले अंडरवोल्टेज लॉकआउट (UVLO) सर्किट का सुझाव दिया गया है। सुझाया गया UVLO डुअल-मोड कॉन्फ़िगरेशन में काम करता है, जो एनर्जी-ऑटोनॉमस पावर-स्विचिंग कन्वर्टर्स के लिए ज़रूरी है, जबकि यह पारंपरिक बैंडगैप-आधारित UVLOs (जिनमें कई रेसिस्टर्स और BJTs की ज़रूरत होती है) की तुलना में बहुत कम जगह और पावर लेता है। इस डिज़ाइन को 0.18 µm CMOS टेक्नोलॉजी में बनाया गया है और यह 0.0066 mm^2 का एक्टिव एरिया लेता है। पहले मोड के लिए मापा गया लो-टू-हाई ट्रिप वोल्टेज ($LHTV_1$) और हाई-टू-लो ट्रिप वोल्टेज ($HLTV_1$) क्रमशः 1.362 V और 1.018 V है, जबकि दूसरे मोड के लिए $LHTV_2$ और $HLTV_2$ क्रमशः 1.608 V और 1.492 V हैं। यह सर्किट कमरे के तापमान पर 1.8 V सप्लाई के तहत 300 pA का क्विसेंट करंट (I_Q) लेता है।

अल्ट्रा-लो-पावर ऑपरेशन पाने और कम जगह घेरने के लिए, एनर्जी-एफिशिएंट और एरिया-एफिशिएंट रेफरेंस सर्किट का सुझाव दिया गया है। एक पिकोवाट CMOS-ओनली वोल्टेज रेफरेंस (VR) जो डुअल सेल्फ-रेगुलेशन सर्किट का इस्तेमाल करके लाइन सेंसिटिविटी (LS) को बेहतर बनाता है, साथ ही कम जगह और पावर लेता है। सुझाए गए डिज़ाइन को 65 nm CMOS लो पावर (LP) प्रोसेस में लागू किया गया है और यह 1373 μm^2 का एक्टिव एरिया लेता है। पोस्ट-लेआउट मोंटे कार्लो सिमुलेशन से पता चलता है कि सर्किट 287 mV का औसत रेफरेंस वोल्टेज और 10.32 mV का स्टैंडर्ड डेविएशन देता है। 0.5 V से 1.2 V की सप्लाई वोल्टेज रेंज में लाइन सेंसिटिविटी 0.59%/V है, और जब पावर सप्लाई 0.8 V से 1.2 V तक बदलती है, तो यह घटकर 0.036%/V हो जाती है। यह सर्किट कमरे के तापमान पर 0.5 V की सप्लाई से 70 pA का क्वीसेंट करंट (quiescent current) लेता है। प्रोसेस वेरिएशन से प्रभावित न होने वाले रेफरेंस वोल्टेज और करंट को बनाने के लिए, एक सिंगल बाइपोलर जंक्शन ट्रांजिस्टर (BJT)-बेस्ड वोल्टेज-करंट रेफरेंस (VCR) का सुझाव दिया गया है, जो दोनों को एक ही सर्किट में मिलाता है। सुझाए गए डिज़ाइन में, एक β-मल्टीप्लायर एक प्रोपोर्शनल-टू-एब्सोल्यूट-टेम्परेचर (PTAT) वोल्टेज बनाता है, जिसे एक फ्रैक्शनल BJT एमिटर-बेस वोल्टेज (V_{EB}) के साथ जोड़ा जाता है, जिसमें कॉम्प्लिमेंट्री-टू-एब्सोल्यूट-टेम्परेचर विशेषताएँ होती हैं, ताकि टेम्परेचर-कंपनसेटेड रेफरेंस वोल्टेज (V_{REF}) प्राप्त किया जा सके। रेफरेंस करंट (I_{REF}) को V_{REF} और टेम्परेचर-कंपनसेटेड रेसिस्टर (TCR) के अनुपात से प्राप्त किया जाता है, जिसे CTAT अनसिलिसाइड P+ पॉली रेसिस्टर और PTAT N-वेल रेसिस्टर के सीरीज़ कनेक्शन के रूप में लागू किया जाता है। सुझाए गए सर्किट को 65-nm CMOS टेक्नोलॉजी में लागू किया गया है और यह 0.1 mm^2 का एरिया लेता है। पोस्ट-लेआउट मोंटे कार्लो सिमुलेशन के नतीजे बताते हैं कि V_{REF} और I_{REF}, -40°C से 120°C की टेम्परेचर रेंज में क्रमशः 13.9 ppm/°C और 83.85 ppm/°C का औसत टेम्परेचर कोएफिशिएंट प्राप्त करते हैं। औसत V_{REF} और I_{REF} वैल्यू क्रमशः 243.34 mV और 9.97 nA हैं, जिनका स्टैंडर्ड डेविएशन क्रमशः 2.49 mV और 454 pA है। यह सर्किट 0.85 V सप्लाई पर काम करता है और 120°C पर 113 nW पावर इस्तेमाल करता है।

इसके अलावा, पावर मैनेजमेंट यूनिट (PMU) को ऐसे एनर्जी-एफिशिएंट एप्लीकेशन के लिए डिज़ाइन किया गया है, जिन्हें अलग-अलग तरह के लोड करंट के लिए साफ़ और रेगुलेटेड सप्लाई देने के लिए अल्ट्रा-लो I_Q लो ड्रॉपआउट रेगुलेटर (LDO) की ज़रूरत होती है। इस थीसिस में, बेहतर लोड रेगुलेशन वाला एक अल्ट्रा-लो क्वीसेंट, आउटपुट-कैपेसिटर-लेस लो-ड्रॉपआउट रेगुलेटर (OCL-LDO) प्रस्तावित किया गया है। LDO आर्किटेक्चर FVF टोपोलॉजी पर आधारित है, जहाँ DC लोड रेगुलेशन और ट्रांजिएंट परफॉर्मेंस को बेहतर बनाने के लिए फोल्डेड-कैसकोड कॉमन-गेट एम्पलीफायर के कॉन्स्टेंट-करंट सोर्स की जगह करंट-मिरर लोड वाला Gm स्टेज लगाया गया है। हाई-पावर ट्रांजिस्टर को चलाने के लिए एक सुपर-सोर्स फॉलोअर (SSF) लगाया गया है, जो वोल्टेज बफ़र का काम करता है। साथ ही, लो-टू-हाई लोड स्टेप के दौरान तेज़ी से सेटल होने का समय पाने के लिए एक डायनामिक सेंसिंग यूनिट का इस्तेमाल किया गया है। प्रस्तावित LDO को 65 nm लो-पावर CMOS प्रोसेस में डिज़ाइन किया गया था। LDO 95 nA क्वीसेंट करंट इस्तेमाल करता है और 1.2 V सप्लाई और 1 V रेगुलेटेड आउटपुट के साथ 50 mA तक लोड करंट दे सकता है। यह लोड करंट को 500 nA से 50 mA तक बदलकर 14.8 mV/A का DC लोड रेगुलेशन हासिल करता है। 100 pF लोड कैपेसिटर के साथ, फुल-लोड-स्टेप करंट के लिए 100 ns राइज़ टाइम पर आउटपुट वोल्टेज अंडरशूट 626 mV होता है और 200 ns राइज़ टाइम पर घटकर 530 mV हो जाता है, जो 350 ns के अंदर सेटल हो जाता है। क्वीसेंट करंट, एरिया और दूसरे LDO पैरामीटर - खासकर लाइन/लोड रेगुलेशन, सेटलिंग टाइम और मैक्सिमम लोड करंट - के बीच सबसे अच्छा तालमेल बिठाने के लिए, मल्टीपल-फीडबैक लूप (MFL) वाला एक अल्ट्रा-लो-पावर, आउटपुट-कैपेसिटर-लेस लो-ड्रॉपआउट रेगुलेटर (OCL-LDO) प्रस्तावित किया गया है। प्रस्तावित LDO में पाँच फीडबैक लूप हैं जो बेहतरीन स्टेडी-स्टेट और ट्रांजिएंट परफॉर्मेंस देते हैं। एक ट्राई-लूप FVF स्टेज लाइन और लोड रेगुलेशन, दोनों को बेहतर बनाता है। सोर्स क्रॉस-कपल्ड एरर एम्प्लीफायर (SXCEA) पर आधारित स्लू-रेट एन्हांसमेंट लूप तेज़ ट्रांज़िएंट रिस्पॉन्स देता है। इसके अलावा, प्रस्तावित LDO एक डायनामिक फीडबैक लूप का इस्तेमाल करता है जो फुल-लोड स्टेप करंट के दौरान अंडरशूट रिकवरी टाइम को काफी बेहतर बनाता है। प्रस्तावित LDO को 65-nm CMOS नोड में 0.025 mm^2 के एक्टिव एरिया के साथ बनाया गया था। LDO 1 V आउटपुट वोल्टेज पर अधिकतम 50 mA लोड करंट दे सकता है और केवल 22 nA का क्विसेंट करंट (quiescent current) इस्तेमाल करता है। माप के नतीजे बताते हैं कि प्रस्तावित LDO 0.004 mV/mA का लोड रेगुलेशन

और फुल लोड पर -63.5 dB का लो-फ़्रीक्वेंसी पावर सप्लाई रिजेक्शन (PSR) हासिल करता है। 10 ns एज टाइम के साथ 200 nA से 50 mA तक के लोड करंट स्टेप के लिए, मापा गया वोल्टेज अंडरशूट 574 mV है और यह 200 ns के भीतर स्थिर हो जाता है।

कुल एरिया और बिजली की खपत को और कम करने के लिए, एक पूरी तरह से इंटीग्रेटेड, कम-पावर, कम-वोल्टेज, लो-ड्रॉपआउट रेगुलेटर का प्रस्ताव दिया गया है जो LDO के फीडबैक रेसिस्टर्स को एक सिंगल BJT-आधारित वोल्टेज रेफरेंस के साथ शेयर करता है। प्रस्तावित आर्किटेक्चर तापमान-कंपेंसेटेड, रेगुलेटेड आउटपुट वोल्टेज बनाने के लिए केवल एक BJT और दो रेसिस्टर्स का इस्तेमाल करता है, जबकि पारंपरिक रेफरेंस-इंटीग्रेटेड वोल्टेज रेगुलेटर में कई BJTs और रेसिस्टर्स की ज़रूरत होती है। इसके अलावा, वोल्टेज डिवाइडर सर्किट का इस्तेमाल करके BJT के V_{EB} को उसके आधे मान तक कम करके, डिज़ाइन सब-1V ऑपरेशन हासिल करता है। इसलिए, प्रस्तावित LDO एरिया और बिजली दोनों के मामले में कुशल है। प्रस्तावित आर्किटेक्चर को 65-nm लो-पावर CMOS नोड में बनाया गया था और यह 0.017 mm^2 का डाई एरिया लेता है। LDO 0.608 V के नॉमिनल आउटपुट वोल्टेज पर अधिकतम 10 mA का लोड करंट देता है। माप के नतीजे बताते हैं कि LDO -40°C से 120°C तक 26.2 ppm/°C का तापमान गुणांक (TC) और 0.499% की वोल्टेज सटीकता हासिल करता है। मापी गई लाइन रेगुलेशन और लोड रेगुलेशन क्रमशः 3.925 mV/V और 0.12 mV/mA हैं। LDO, 0.8 V के मिनिमम सप्लाई वोल्टेज पर 241 nW पावर का इस्तेमाल करता है।

छोटे सिलिकॉन एरिया, कम पावर खपत और बेहतरीन LDO परफॉर्मेंस मेट्रिक्स के बीच सही संतुलन बनाने के लिए, एनर्जी-हार्वेस्टिंग एप्लीकेशन के लिए एक पूरी तरह से इंटीग्रेटेड आउटपुट-कैपेसिटर-लेस (OCL) मल्टी-फीडबैक-लूप लो-ड्रॉपआउट रेगुलेटर (LDO) का प्रस्ताव है, जिसमें इन-बिल्ट सिंगल बाइपोलर जंक्शन ट्रांजिस्टर (BJT)-बेस्ड वोल्टेज और करंट रेफरेंस होता है। प्रस्तावित आर्किटेक्चर में चार लूप होते हैं, जो LDO के DC रेगुलेशन और ट्रांजिएंट परफॉर्मेंस को काफी बेहतर बनाते हैं। फ्लिप्ड-वोल्टेज-फॉलोअर (FVF) स्ट्रक्चर पर आधारित ट्राई-लूप रेगुलेशन कोर हाई DC लूप गेन देता है, जिससे लाइन और लोड रेगुलेशन बेहतर होता है। एक रेप्लिका-बेस्ड स्ल्यू-रेट एन्हांसमेंट (RSRE) लूप लोड ट्रांजिएंट रिस्पॉन्स के दौरान अंडरशूट और ओवरशूट रिकवरी टाइम को बेहतर बनाता है। इसके अलावा, प्रस्तावित LDO कम एरिया और पावर का इस्तेमाल करता है, और FVF पावर स्टेज के साथ सिंगल BJT ब्रांच बैंडगैप रेफरेंस (BGR) को इंटीग्रेट करके कम आउटपुट नॉइज़ दिखाता है, जबकि पारंपरिक LDO बाहरी रूप से जुड़े BGR का इस्तेमाल करते हैं, जिनमें कई रेसिस्टर और BJT की ज़रूरत होती है। बायस करंट को एक साझा सिंगल BJT पर आधारित प्रस्तावित करंट रेफरेंस द्वारा आंतरिक रूप से उत्पन्न किया जाता है और करंट लाइन सेंसिटिविटी को बेहतर बनाने के लिए इसे LDO आउटपुट वोल्टेज से पावर मिलती है। प्रस्तावित डिज़ाइन 65-nm लो-पावर CMOS टेक्नोलॉजी में बनाया गया है और 0.041 mm^2 का एरिया लेता है। माप के नतीजे बताते हैं कि प्रस्तावित LDO क्रमशः 0.66 mV/V और 0.195 mV/mA का लाइन और लोड रेगुलेशन हासिल करता है। अधिकतम लोड करंट पर 10 Hz पर मापा गया पावर सप्लाई रिजेक्शन (PSR) 67.5 dB है। प्रस्तावित LDO कमरे के तापमान पर 1.3 V के मिनिमम सप्लाई वोल्टेज के साथ 268 nA का क्वीसेंट करंट इस्तेमाल करता है।

Contents

Certificate i

Acknowledgments ii

Abstract iii

List of Figures xi

List of Tables xvi

Abbreviations xvii

1 Introduction 1
- 1.1 Piezoelectric energy harvesting interface circuit . . . 2
  - 1.1.1 Applications of piezoelectric energy transducer . . . 2
  - 1.1.2 Overview of piezoelectric energy harvesting interface circuit . . . 4
- 1.2 Reference circuits . . . 4
  - 1.2.1 Bandgap voltage reference . . . 5
  - 1.2.2 CMOS-only voltage reference . . . 6
  - 1.2.3 Hybrid voltage reference . . . 7
  - 1.2.4 Current reference . . . 9
- 1.3 Low dropout regulator . . . 10
- 1.4 Our work and thesis organization . . . 11

2 AC-DC power management unit for energy harvesting from piezoelectric transducer 14
- 2.1 PLL-based rectifier-less power switching converter . . . 16
  - 2.1.1 Operating principle . . . 17
  - 2.1.2 Circuit implementation . . . 17
  - 2.1.3 Harvester efficiency . . . 20
  - 2.1.4 Simulation results . . . 20
- 2.2 Multi-step charge transfer interface circuit . . . 22
  - 2.2.1 Operating principle . . . 23
  - 2.2.2 Circuit implementation . . . 26
  - 2.2.3 Harvested power analysis . . . 26
  - 2.2.4 Simulation results . . . 27
- 2.3 CMOS-only undervoltage lockout circuit . . . 28
  - 2.3.1 Dual-mode UVLO . . . 30
  - 2.3.2 Low-voltage and high-voltage UVLO implementation . . . 33
  - 2.3.3 Simulation and measurement results . . . 33

2.4 Conclusions . . . 35

3 Ultra-low-power reference circuits 37
3.1 Introduction . . . 37
3.2 Dual self-regulated CMOS VR . . . 38
3.2.1 Architecture implementation . . . 38
3.2.2 Line sensitivity . . . 39
3.2.3 Post-layout simulation results . . . 40
3.3 Single BJT-based VCR . . . 41
3.3.1 Voltage reference . . . 41
3.3.2 Current Reference . . . 43
3.3.3 Supply Voltage . . . 44
3.3.4 Post-layout simulation results . . . 45
3.4 Conclusion . . . 46

4 Ultra low quiescent current low dropout regulator 49
4.1 Introduction . . . 49
4.2 Gm-boosted OCL-LDO with fast transient response . . . 50
4.2.1 Circuit design and implementation . . . 51
4.2.2 Stability analysis . . . 52
4.2.3 DC load regulation . . . 54
4.2.4 Simulation results . . . 54
4.3 A multiple-feedback loop LDO . . . 56
4.3.1 MFL-LDO architecture . . . 57
4.3.2 Circuit implementation and LDO performance analysis . . . 58
4.3.3 Measurement results . . . 63
4.4 Conclusion . . . 65

5 A sub-1 V LDO with integrated single-BJT VR 66
5.1 Introduction . . . 66
5.2 Proposed reference-integrated LDO . . . 67
5.2.1 Architectural considerations . . . 67
5.2.2 Operating principle and circuit implementation . . . 67
5.2.3 LDO performance analysis . . . 70
5.3 Measurement results . . . 73
5.4 Conclusion . . . 77

6 A multi-loop LDO with integrated single-BJT VR and CR 80
6.1 Introduction . . . 80
6.2 Proposed VCR-Integrated MFL Regulator . . . 82
6.2.1 Architectural considerations . . . 82
6.2.2 Regulation Core . . . 84
6.2.3 Replica-Based Slew-Rate Enhancement . . . 89
6.2.4 Constant Bias Current Generator . . . 90
6.3 Full Circuit Implementation and Performance Analysis . . . 94
6.3.1 Efficiency Analysis . . . 95
6.3.2 Stability Analysis . . . 96
6.3.3 DC PSR Analysis . . . 99
6.3.4 Device Noise Analysis . . . 101

6.4 Measurement Results 103
6.5 Conclusion 110

7 Conclusion and Future Scope **111**
7.1 Energy harvesting interface circuits 111
7.2 Reference circuits 112
7.3 OCL-LDO 112
7.4 A fully-integrated sub-1V LDO 113
7.5 A fully-integrated multi-loop LDO 113
7.6 Future scope 113

Bibliography **114**

List of Publications **124**

List of Figures

1.1 Block diagram of an energy autonomous WSN. 2
1.2 Hierarchical block diagram of bucks, bandgap reference, and LDOs in the WSN PMIC 3
1.3 Piezoelectric cantilever structure 3
1.5 Vibration energy harvester applications 3
1.4 Typical piezoelectric energy harvesting system 4
1.6 (a) Voltage-mode BGR and (b) current-mode BGR 5
1.7 Schematic of the (a) 2T VR and (b) 3T VR 6
1.8 Schematic of the single BJT branch HVR (a) without resistors and (b) with resistors. 8
1.9 Simplified schematic of the (a) current-sum-based I_{REF} generation and (b) division-based V-to-I current reference. 9
1.10 Simplified structure of the (a) conventional LDO with single feedback loop and (b) FVF-LDO with dual loop. 10

2.1 Piezoelectric output voltage waveform of (a) MS-SECE (b) MCEBF (c) MCE-MPE (d) RPCA. 15
2.2 System-level architecture of the proposed piezoelectric energy harvesting IC including off-chip components and external control signals. The PLL locks to the input vibration frequency and controls the power switches to harvest power from the piezoelectric transducer optimally. 16
2.3 Simplified representation of the Integer-N charge-pump phase-locked loop (PLL) where N is 2. 18
2.4 Schematic of the digital switch control logic unit. 19
2.5 Simulated transient waveforms of the piezoelectric output voltage and the PLL output signal. The zoom-in views show that the PLL is locked, and harvesting begins. 20
2.6 Simulation of piezoelectric output voltage V_{PEH}, inductor current, and switch driving signals during the energize and dump phase. 21
2.7 (a) Simulated output power varies with load voltage at three different input power values. (b) Simulated harvester efficiency and output power across piezoelectric open-circuit voltage with $V_{DD} = 1.5\,V$. 22
2.8 Simulated power dissipation of various circuit blocks along with percentage ratio is shown. The graph depicts a resistive conduction loss of 149 nW and 59.5 nW control unit loss. 23
2.9 Top-level architecture of the proposed multi-step charge transfer interface circuit with external digital signals and off-chip components. 24

2.10 Piezoelectric output voltage waveforms with different V_{PC} when (a) V_{PEZ} flips two times (b) V_{PEZ} flips once (c) no flipping per harvesting time period T_{HAR}. 25
2.11 Schematic diagram of the tunable pulse generator for energize pulse with width (a) t_E (b) t_C 26
2.12 Simulation of (a) V_{PEZ} and inductor current waveforms for the case where piezoelectric voltage flips once per harvesting cycle, with zoomed waveforms during the multi-step (b) charge extraction and precharge phase, and (c) bias-flip phase. In this simulation, N is 4, $V_{PEZ,OC}$ is 508 mV, and L is 47 μH. 27
2.13 (a) Simulated average output power as a function of number of steps N with different precharge voltages when (a) $V_{PEZ,OC}$ = 508 mV (b) $V_{PEZ,OC}$ = 471 mV. In this simulation, L is 47 μH. 28
2.14 (a) Simulated power conduction loss and (b) harvesting efficiency as a function of N with two different inductor values. In this simulation, $V_{PEZ,OC}$ is 508 mV, V_{PC} is 4.5$V_{PEZ,OC}$ and V_{OUT} is 1.5 V 29
2.15 Block diagram of the energy-harvesting power management unit. 30
2.16 Schematic of the proposed UVLO, where the body terminals of all pMOS transistors are tied to their respective source terminals to eliminate threshold voltage mismatch caused by the body-effect. 31
2.17 Graphical representation of operating modes. 32
2.18 Variants of the proposed UVLO configured for (a) low-voltage and (b) high voltage CMOS processes. The minimum supply voltage (V_D) required to obtain stable reference voltage for the low-voltage and high-voltage configurations is $V_R + 4V_T$ and N$V_R + 4V_T$, respectively. 33
2.19 (a) Chip micrograph highlighting the UVLO circuit and (b) its corresponding layout view. 34
2.20 Simulated temperature variation of LHTV and HLTV for both modes of operation. 34
2.21 Histogram plot of trip voltages obtained from 1000-run Monte-Carlo simulations. 35
2.22 Measured transient waveforms of the UVLO select signals during supply power-up and power-down. 36

3.1 Schematic of the (a) 3T VR with single self-regulation loop reported in [1], (b) proposed VR with dual self-regulation. 39
3.2 Proposed VR Layout in 65 nm CMOS. 40
3.3 (a) Simulated V_{REF} as a function of V_{DD} for 3T and proposed VR (b) V_{REF} distribution obtained from 500 Monte-Carlo simulation runs at 0.5 V V_{DD}. 40
3.4 (a) Simulated V_{REF} variation with temperature under different V_{DD} (b) Statistically distribution of TC with 0.5 V supply. 41
3.5 Schematic of the proposed single BJT-based VCR. 42
3.6 Schematic of the operational amplifier (a) OP_1 and (b) OP_2. In both amplifiers, the first stage is a five-transistor operational transconductance amplifier (OTA), while the second stage is a common source amplifier with an active load. 43
3.7 Proposed VCR layout. 45
3.8 Post-layout simulations of (a) V_{REF} and (b) I_{REF} versus temperature in all process corners, at $V_{DD} = 0.85$ V. 45
3.9 Post-layout Monte-Carlo simulation of (a) V_{REF}, (b) TC of V_{REF}, (c) I_{REF}, and (d) TC of I_{REF} for 500 runs. In this simulation, both process and mismatch are included. 46

3.10 Post-layout simulations of (a) V_{REF} and (b) I_{REF} with temperature at different V_{DD} levels. 47
3.11 Post-layout simulated (a) V_{REF} and (b) I_{REF} as a function of V_{DD} at T= 27 °C. . 47
3.12 The total power consumption of the proposed VCR versus temperature at V_{DD} = 0.85 V. 48

4.1 Proposed LDO architecture. The M_{A1} operates as an amplifying transistor. M_{A2} and M_{A3} serve as the current mirror load. 50
4.2 Full schematic of the proposed LDO. 50
4.3 Small signal model of the LDO core with Miller compensation scheme. 52
4.4 Layout view of the LDO. 53
4.5 Simulated open-loop frequency response of the proposed LDO under different I_{LOAD} and C_L = 100 pF. 54
4.6 Simulated load transient responses under various C_L for a step load current with the rise (T_R) and fall time (T_F) of (a) 100 ns, (b) 200 ns, respectively. 55
4.7 (a) Simulated load regulation by varying load current for (1) conventional CAFVF, (2) pre-layout, and (3) post-layout proposed LDO (b) Histogram plot of LR from 500-runs Monte-Carlo simulation. 56
4.8 Proposed architecture of the multiple-feedback loop LDO. 57
4.9 Full schematic of the proposed LDO. 58
4.10 Monte-Carlo simulation for (a) V_{OUT} and (b) I_Q. In this simulation, V_{IN} is 1.2 V, and I_{LOAD} is 200 nA. 59
4.11 Small-signal model of the proposed LDO. 60
4.12 Simulated frequency response of the global loop with different I_{LOAD} at $C_L = 150$ pF. 61
4.13 (a) Four major supply ripple coupling paths exist in the LDO. (b) Simulated overall PSR at $I_{LOAD} = 50$ mA, where the red and black curves represent EA being supplied by V_{IN} and V_{OUT}, respectively. 62
4.14 (a) Chip micrograph. (b) Measured V_{OUT} by varying off-chip and on-chip R_L over a range of 20 Ω–5 MΩ and 20 Ω–1 kΩ, respectively, with $V_{IN} = 1.2$ V. 62
4.15 (a) Measured PSR at different load currents. (b) Measured transient waveforms of v_{in} and v_{out} at 200 Hz with $I_{LOAD} = 50$ mA. 63
4.16 Measured load transient responses for a load current step of (a) 1–100 μA and (b) 1–10 mA, respectively. In this measurement, V_{IN} is 1.2 V, V_{OUT} is 1 V, off-chip C_L is 100 pF, and edge time (T_E) is 10 ns. 64
4.17 Measured load transient response for a 200 nA to 50 mA load step with $V_{IN} = 1.2$ V, $V_{OUT} = 1$ V, $C_L = 100$ pF, and $T_E = 10$ ns. 64

5.1 (a) Conventional voltage regulator with external BGR. (b) Single BJT BGR with load driving capability. 67
5.2 Schematic of the proposed LDO structure. 68
5.3 Schematic of the two-stage error amplifier (a) EA_1 and (b) EA_2. 69
5.4 (a) Small-signal model. (b) Simulated Bode plot of the regulation loop across different process corners and at two temperatures (−40 °C and 120 °C). The simulation is carried out under the worst-case stability condition for the OCL-LDO, i.e., $I_{LOAD} = 5\,\mu$A and load capacitance $C_L = 100$ pF. 70
5.5 Simplified circuit representation for analyzing (a) DC power supply rejection (PSR) and (b) the effect of non-idealities in a proposed LDO. 71
5.6 (a) Chip micrograph. (b) Measured I_Q vs. temperature at various V_{IN}. 73

5.7 Measured temperature variation of V_{OUT} across ten chips under (a) 0.8 V supply and (b) 1.2 V supply. 74
5.8 Measurement setup for line and load regulation. 74
5.9 (a) Measured line and load regulation. (b) Measured PSR. 75
5.10 (a) Measured load transient response. (b) Measured output voltage noise spectral density. In both cases, $V_{IN} = 0.8$ V and off-chip $C_L = 100$ pF. 76
5.11 Power line ground loop. 77
5.12 Measurement setup for eliminating ground loop. 77

6.1 Schematic of a conventional regulator with an external VR, implemented as either (a) a CMOS-only VR or (b) a double BJT branch voltage-mode BGR. 82
6.2 (a) Single-BJT branch BGR with load-driving capability. (b) FVF pass stage. . . 83
6.3 Proposed circuit diagram of the tri-loop regulation core. The flat V_{OUT} response (shown in gray) indicates that the regulation stage maintains a nearly constant output voltage across variations in process (P), temperature (T), supply voltage (V_{IN}), and DC load current (I_{LOAD}). 84
6.4 (a) Schematic of the PTAT-embedded amplifier. (b) Simulated V_{OUT} versus temperature across different process corners at $V_{IN} = 1.3$ V. 85
6.5 (a) Implementation of binary trimming for R_{F1}. (b) Simulated V_{OUT} versus temperature with trimming applied individually for each process corner at $V_{IN} = 1.3$ V. 86
6.6 Simulated 500-run Monte Carlo distributions of (a) V_{OUT} at 27 °C and (b) its TC over −40 °C to 85 °C with a fixed trimming code. 86
6.7 (a) Small signal model of the regulation core at DC. Unless otherwise specified, it is assumed that the small-signal resistance at the emitter node of Q_1 is much lower than at v_{out} and v_{fb}, allowing v_{eb} to be treated as an ac ground. (b) Simulated gain plots of the regulation core and the FVF loop at minimum load current. 87
6.8 Proposed RSRE. 89
6.9 Simulated load transient response with and without the NF_{L4} loop during load (a) step-up from 500 nA to 50 mA and (b) step-down from 50 mA to 500 nA. In this simulation, $V_{IN} = 1.3$ V and the edge time $T_E = 10$ ns. 90
6.10 Schematic of the shared single BJT branch nanoampere CR. 91
6.11 Simulated 500-run Monte Carlo distributions of the TC of (a) R and (b) V_{REF}, showing their mean (μ) and standard deviation (σ) under global and local variations. In this simulation, the temperature range is −40 °C to 85 °C. 93
6.12 Full schematic of the proposed LDO. 94
6.13 (a) Simulated leakage current of M_{S1} at different supply voltages under extreme process and temperature corners. (b) Simulated $I_{L,MS1}$ as a percentage of I_Q at different V_{IN} under FF process corner and 85 °C. 94
6.14 Simulated (a) current efficiency and (b) power efficiency of the proposed LDO at $V_{IN} = 1.3$ V, $V_{OUT} = 1.2$ V, and $T = 27$ °C. 95
6.15 Small-signal model for stability analysis of the MFL-LDO. 96
6.16 Conceptual gain plot of the global loop and the combined FVF and RSRE loops. 98
6.17 (a) Simulated frequency responses of the global loop under different process and temperature conditions. (b) Simulated 500-run Monte Carlo distribution of PM at the FF corner and −40 °C, including local mismatch. Both simulations are performed under the worst-case stability condition for the OCL-LDO, i.e., $I_{LOAD} =$ 500 nA and $C_L = 100$ pF. 99

6.18 Simulated frequency responses of the global loop under (a) different load currents and (b) different supply voltages at the TT corner and 27 °C. 100
6.19 (a) Simulated frequency responses of the local loops. (b) Simulated loop stability plot of the positive feedback loop across different process and temperature corners. 101
6.20 Simplified small-signal model for DC PSR analysis. 102
6.21 Simplified circuit representation for analyzing the contribution of the major noise sources in (a) the proposed LDO and (b) a conventional LDO. 102
6.22 (a) Simulated breakdown of noise contributions. (b) Simulated output noise spectral density. 103
6.23 (a) Chip micrograph. (b) Measured I_Q versus temperature at different V_{IN}. 103
6.24 Measurement setup for I_Q ($I_{IN} - I_{LOAD}$) characterization. 104
6.25 Measured temperature dependence of V_{OUT} under (a) $V_{IN} = 1.4$ V (10 samples) and (b) different V_{IN} (1 sample), for $I_{LOAD} = 10$ μA. 105
6.26 Measured (a) line and (b) load regulation characteristics of the LDO. 105
6.27 Measurement setup for PSR characterization. 106
6.28 (a) PSR measured under different load conditions and simulated PSR (black curve) without PF_{L3} loop. (b) Measured transient waveforms at full load with input ripple at 2 kHz. 106
6.29 Measured load transient response for different load current steps at $V_{IN} = 1.4$ V and $C_L = 100$ pF. 107
6.30 (a) Measured load transient response for a full load step without C_L at $V_{IN} = 1.4$ V. (b) Measured load transient response for a 1–10 mA load step at $V_{IN} = 1.3$ V and $C_L = 100$ pF. 107
6.31 Measured output noise spectral density of the proposed LDO at $V_{IN} = 1.3$ V, $C_L = 100$ pF, and $I_{LOAD} = 500$ nA. 108
6.32 Measured (a) temperature dependence and (b) line sensitivity of $I_{REF,PAD}$. . . . 108

List of Tables

2.1 Performance Comparison With State-of-the-Art Rectifier 28
2.2 Performance Summary and Comparison With State-of-the-Art 36

3.1 Performance Comparison With State-of-the-Art CMOS VR 41
3.2 Performance Summary and Comparison 48

4.1 LDO Core Device Dimensions 51
4.2 Performance Comparison With State-of-the-Art OCL-LDO 56
4.3 Performance Comparison With State-of-the-Art OCL-LDOs 65

5.1 Performance Summary and Comparison With State-of-the-Art 79

6.1 Performance Summary and Comparison With the State-of-the-Art Reference-Integrated OCL-LDOs 109

Abbreviations

AC	Alternating Current
DC	Direct Current
WSN	Wireless Sensor Nodes
PEH	Piezoelectric Energy Harvester
MPPT	Maximum Power Point Tracking
SECE	Synchronous Electric Charge Extraction
MSEE	Multistage Energy Extraction
MSCT	Multi-Step Charge Transfer
PLL	Phase Locked Loop
CP	Charge Pump
PFD	Phase/Frequency Detector
DCM	Discontinuous Conduction Mode
VCO	Voltage-Controlled Oscillator
RCD	Reverse Current Detector
ZCD	Zero Crossing Detector
UVLO	Under Voltage Lockout
LHTV	Low-to-High Trip Voltage
HLTV	High-to-Low Trip Voltage
TG	Transmission Gate
CG	Common-Gate
TC	Temperature Coefficient
BGR	Bandgap Reference
CMOS	Complementary Metal Oxide Semiconductor
IoT	Internet-of-Things
BJT	Bipolar Junction Transistor
CTAT	Complementary To Absolute Temperature
PTAT	Proportional To Absolute Temperature
VR	Voltage Reference
PVT	Process-Voltage-Temperature
NMOS	N-Channel Metal Oxide Semiconductor
LS	Line Sensitivity
VCR	Voltage-Current Reference
UGB	Unity-Gain Bandwidth
TCR	Temperature-Compensated Resistor
PMU	Power Management Unit
PMIC	Power Management Integrated Circuit
PPA	Power, Performance, and Area
OCL	Output-Capacitor-Less

LDO	Low Drop Out
SoC	System-on-Chip
CAFVF	Cascoded Flipped Voltage Follower
SR	Slew Rate
SSF	Super Source Follower
DSU	Dynamic Sensing Unit
CVG	Control Voltage Generation
OTA	Operational Transconductance Amplifier
EA	Error Amplifier
PM	Phase Margin
GM	Gain Margin
LR	Load Regulation
LP	Low Power
FOM	Figure of Merit
MFL	Multiple Feedback Loop
NFL	Negative Feedback Loop
PFL	Positive Feedback Loop
PSR	Power Supply Rejection
SXCEA	Source Cross-Coupled Error Amplifier
UDB	Undershoot Detection Block
LHP	Left Half Plane
RHP	Right Half Plane
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
RF	Radio Frequency