

**EFFICIENT TECHNIQUES FOR  
FAULT DIAGNOSIS OF ANALOG CIRCUITS  
USING DICTIONARY APPROACH**

by  
**N. SARAT CHANDRA BABU**

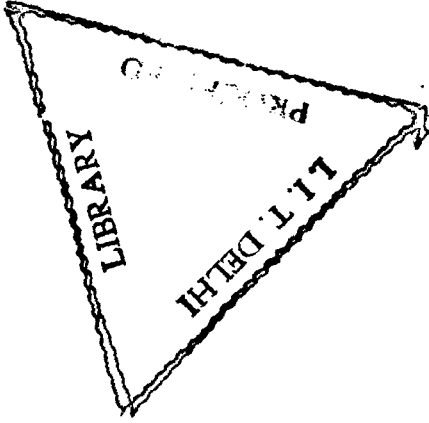
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## CERTIFICATE

This is to certify that the thesis entitled “**EFFICIENT TECHNIQUES FOR FAULT DIAGNOSIS OF ANALOG CIRCUITS USING DICTIONARY APPROACH**”, which is being submitted by N. Sarat Chandra Babu, to the Department of Electrical Engineering, Indian Institute of Technology, Delhi, India. for the award of degree of Doctor of Philosophy, is a record of bonafide research work carried out under my guidance and supervision.

This dissertation has reached the standard of fulfilling the requirements of the regulations to the degree. The results contained in this thesis have not been submitted to any other University or Institute for award of any degree or diploma.



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**THIS THESIS  
IS DEDICATED  
TO  
MY PARENTS**

**Late Sri. N.Venkatachary and Smt. Meenakshi Sundaram**

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## ABSTRACT

The proliferation of large analog networks and systems, growing usage of mixed mode analog/digital integrated circuits, and the need for diagnosing analog faults in the digital circuits, has made the problem of analog fault diagnosis very important. However the inherent problems associated with analog circuits such as continuum of failures, component tolerances etc. makes their fault diagnosis more complex and slow. Thus there is a need for devising special methods to tackle this problem. Fault dictionary, which is one of the three approaches of analog fault diagnosis, is popular, as it requires less test measurements to isolate a given set of faults. This method consists of three phases viz., fault dictionary construction, selection of test nodes, and fault isolation. This thesis is concerned with the study of last two phases.

Chapter 2 deals with improvements in diagnosability. A systematic analysis is carried out to study the effectiveness of multiple excitations. They are shown to be useful in situations where single excitation fails. It is demonstrated that varying amplitude of single excitation will not help, whereas changing amplitude of one of multiple excitations help in separating faults. In the present work it has been found that the capability of fault dictionary enhances greatly by loading accessible nodes. i.e., by connecting external impedances across accessible nodes. This technique exploits the behaviour of the Thevenin's equivalent circuit. It is shown that external impedance can be connected in many ways. It is possible even to use input node as a test node for diagnosing some faults. This approach is novel and results are promising. In general component tolerances affect the diagnosability of analog circuit faults. An efficient technique is devised to account for component tolerances. This approximates the fault bands under the assumption that deviation of circuit parameters under different faults is more or less same as deviations under nominal conditions.

In Chapter 3, selection of test nodes has been studied in-depth to explore efficient techniques to generate valid sets and minimal sets, falling under inclusion methods and exclusion methods respectively. The main objective of this phase is to reduce number of nodes with out affecting the diagnosis capability. A new method is presented to generate the test node set using sorting. Fault-wise integer coded table entries are sorted, whenever a node is included. This sorting is repeated till there is no repetition of the numbers in the sorted list. This method is shown to have time complexity of  $O(fp \log f)$ . There is hardly any method in the literature, which gives a minimal set of test nodes. One important contribution of the thesis is development of efficient methods to solve this problem. A method is proposed to generate minimal sets directly from initial set of test nodes employing sort technique in polynomial time compared to the Boolean technique that requires exponential time. Techniques are proposed to obtain a minimal set by suitably modifying a non-minimal set generation algorithm. Parallel methods are suggested which adopt existing parallel sort algorithms to speed-up this phase. The work required to generate a minimal set is proportional to  $(p+m)$ . An attempt has been made, to generate test node sets in a novel way using hardware. A Boolean circuit is developed to select test nodes. Using this circuit as the basic building block, hardware schemes are proposed to generate (i) all valid sets (ii) all minimal sets and (iii) one minimal set. Generation of one minimal set using hardware is very fast.

Most methods use fault-wise information from ambiguity sets. Deviating from this philosophy, a new method using pairs of faults is proposed in Chapter IV. This is shown to have many advantages. In this method, a fault pair table is constructed with one row per fault pair. Methods are presented to generate valid sets and minimal sets. Binary nature of this table is exploited to present efficient techniques to generate these sets. A Boolean method is proposed to get all minimal sets of test nodes. A Boolean circuit is constructed, which is functionally similar to the Boolean circuit developed for fault-wise organisation. It is demonstrated that fault pair methods are well suited to hardware solutions. Therefore hardware schemes can be used gainfully to develop test equipment for test node selection.

A technique is proposed in chapter 5 to eliminate redundant frequencies generated by Seshu and Waxman's method using the methods developed for test node selection. A procedure is developed to select more frequencies when the set of frequencies suggested by their method is not sufficient to isolate faults. It is shown that fault dictionary can be constructed from the measurements of bandwidth and mid-band gain.

Chapter six delves in presenting efficient techniques for fault isolation phase using hardware, parallel and neural net approaches. All these methods separate faults in constant time. Hardware method employs binary coding of the fault-wise integer table. This results in multi input - multi output truth table. A Boolean circuit is realised using this truth table that can separate faults in constant time. Two hardware schemes are suggested to suit test equipment for fault isolation. They can accept field measurements and generate the corresponding binary codes. These codes are given as input to the Boolean circuit that can diagnose the faulty condition of the circuit. Parallel methods are also suggested using fixed or variable number of processors to isolate faults in constant time. Neural network approach is studied for fault isolation phase of analog circuits. Backpropagation (BP) and Radial basis function (RBF) networks are studied for doing this. A new method is proposed for fault isolation using RBF networks. A method to determine the width and centre of RBF units to account component tolerances is suggested. Data representation problems are addressed. A modification is suggested to the RBF network to accommodate novel faults. Performance of the BP and RBF network is compared in terms of learning speed, classification accuracy, data representation problems and response to novel faults in the context of fault isolation.

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