EFFICIENT TECHNIQUES FOR FAULT DIAGNOSIS OF ANALOG CIRCUITS USING DICTIONARY APPROACH

by
N. SARAT CHANDRA BABU

Thesis submitted
in fulfilment of the requirements
for the degree of
DOCTOR OF PHILOSOPHY

Department of Electrical Engineering
INDIAN INSTITUTE OF TECHNOLOGY, DELHI
HAUZ KHAS, NEW DELHI - 110016, INDIA
JUNE, 1997

CERTIFICATE

This is to certify that the thesis entitled **"EFFICIENT TECHNIQUES FOR FAULT DIAGNOSIS OF ANALOG CIRCUITS USING DICTIONARY APPROACH"**, which is being submitted by N. Sarat Chandra Babu, to the Department of Electrical Engineering, Indian Institute of Technology, Delhi, India, for the award of degree of Doctor of Philosophy, is a record of bonafide research work carried out under my guidance and supervision.

This dissertation has reached the standard of fulfilling the requirements of the regulations to the degree. The results contained in this thesis have not been submitted to any other University or Institute for award of any degree or diploma.

V. C. Prasad

(V. C. PRASAD)
Professor
Department of Electrical Engineering
Indian Institute of Technology, Delhi
Hauz Khas, New Delhi - 110 016
INDIA.

THIS THESIS

IS DEDICATED

TO

MY PARENTS

Late Sri. N.Venkatachary and Smt. Meenakshi Sundaram

ACKNOWLEDGEMENTS

I express my deep sense of gratitude to my supervisor Prof. V.C.Prasad for his constant guidance, untiring help and for sparing his valuable time throughout my research work. The discussions we had have enriched my understanding of research and helped me in achieving my educational goal.

My thanks are due to the authorities of IIT Delhi and staff of the Department of Electrical Engineering for providing the necessary facilities to carryout the work.

I am indebted to Late Prof. K.S.P. Rao for his elderly advice and moral support.

I am grateful to Shri S.Mukhopadhyay, Advisor, Shri N. Das Sharma, Senior Director, Dr. Krishna Kant, Director of Department of Electronics (DOE) for their encouragement throughout the period of research work. I am thankful also to the authorities of DOE for giving me permission to carryout research work at IIT, Delhi.

I thank all my colleagues R.S.Mani, R.Ravichandran, D.V.L. Narayana Rao, Mrs.Sangita Arora, Mrs.Uma Chauhan, Dr.(Mrs.) Hema Khurana, Dr.P.S.Nageswara Rao, Mr.Tara Shankar, and Mr.B.B.Tiwari for sharing my work load at office and helping me at various stages of my research work and preparation of the thesis.

My special thanks are due to my colleague Mr.D.V.L.Narayana Rao for his constant encouragement and especially for his excellent DTP support. I also thank Arvind, Sanjay and Sangita for their support in the preparation of drawings.

My heartfelt appreciation is due to Mr. A. Durga Prasad, Manager, Silicon Graphics India for his enjoyable company and my thanks are especially due for sparing his computer and printer during the entire period of thesis writing.

I thank the families of Prof.V.C.Prasad, Lt. Cdr. T.B.Rangachary, Mr.Srinivasa Sastry, Dr.G.V.Sarath Babu, Mr. Muniram, Dr.G.V.Rama Raju, Dr.B.K.Murthy, Mr.S.A.Kumar, Mr.Rajendra Babu Reddy, Sri G. Padmanabha Rao, Mr.Venkata Reddy and Mr.Pitchiah for their ready help and warmth extended to me during crucial phases of my work.

My sincere thanks are to D.V.L.N.Somayajulu and K. Chandrasekhar for their support and company at IIT campus.

I thank Prof.S.B.K.Murthy for his advise and support in proof reading the thesis. I also thank Shri S.P.Dixit for his encouragement and help. I thank Sridhar, Sukhanya and Rama Devi for their help during my thesis work.

My heart felt thanks are due to Dr.N.D.R.Sarma who extended all possible help with his abundant enthusiasm and his constant encouragement to achieve this objective.

I thank my uncles Shri N.Souri Rajan, Shri B.V.Chalam and Shri B.Padmanabham for their advice and encouragement.

I express my gratitude to all my brothers and sisters, Mr. Raghu Ram, Mr. Nanda Kishore, Mr. Ananda Swaroop, Mr. Niranjan, Mrs. Ramadevi, Mrs.Nirmala and Mrs. Padmaja for their constant encouragement and for their support.

I express my deep sense of gratitude to my parents for their constant encouragement and support. It is unfortunate that I miss my father at the time of submission of this thesis. I am sure that his blessings from heaven have helped me to reach this stage of submission.

I express my thanks to my brothers-in-law and sisters-in-law for their moral support.

I express my appreciation and thank my two little daughters Sindhu and Neeharika for their understanding and co-operation.

Finally, I offer my warmest and heartfelt thanks to my wife Radhika for among many other things, her understanding and patience throughout the thesis period.

(N Sarat Chandra Babu)

ABSTRACT

The proliferation of large analog networks and systems, growing usage of mixed mode analog/digital integrated circuits, and the need for diagnosing analog faults in the digital circuits, has made the problem of analog fault diagnosis very important. However the inherent problems associated with analog circuits such as continuum of failures, component tolerances etc. makes their fault diagnosis more complex and slow. Thus there is a need for devising special methods to tackle this problem. Fault dictionary, which is one of the three approaches of analog fault diagnosis, is popular, as it requires less test measurements to isolate a given set of faults. This method consists of three phases viz., fault dictionary construction, selection of test nodes, and fault isolation. This thesis is concerned with the study of last two phases.

Chapter 2 deals with improvements in diagnosability. A systematic analysis is carried out to study the effectiveness of multiple excitations. They are shown to be useful in situations where single excitation fails. It is demonstrated that varying amplitude of single excitation will not help, where as changing amplitude of one of multiple excitations help in separating faults. In the present work it has been found that the capability of fault dictionary enhances greatly by loading accessible nodes. i.e., by connecting external impedances across accessible nodes. This technique exploits the behaviour of the Thevenin's equivalent circuit. It is shown that external impedance can be connected in many ways. It is possible even to use input node as a test node for diagnosing some faults. This approach is novel and results are promising. In general component tolerances affect the diagnosability of analog circuit faults. An efficient technique is devised to account for component tolerances. This approximates the fault bands under the assumption that deviation of circuit parameters under different faults is more or less same as deviations under nominal conditions.

In Chapter 3, selection of test nodes has been studied in-depth to explore efficient techniques to generate valid sets and minimal sets, falling under inclusion methods and exclusion methods respectively. The main objective of this phase is to reduce number of nodes with out affecting the diagnosis capability. A new method is presented to generate the test node set using sorting. Fault-wise integer coded table entries are sorted, whenever a node is included. This sorting is repeated till there is no repetition of the numbers in the sorted list. This method is shown to have time complexity of O(fplogf). There is hardly any method in the literature, which gives a minimal set of test nodes. One important contribution of the thesis is development of efficient methods to solve this problem. A method is proposed to generate minimal sets directly from initial set of test nodes employing sort technique in polynomial time compared to the Boolean technique that requires exponential time. Techniques are proposed to obtain a minimal set by suitably modifying a non-minimal set generation algorithm. Parallel methods are suggested which adopt existing parallel sort algorithms to speed-up this phase. The work required to generate a minimal set is proportional to (p+m). An attempt has been made, to generate test node sets in a novel way using hardware. A Boolean circuit is developed to select test nodes. Using this circuit as the basic building block, hardware schemes are proposed to generate (i) all valid sets (ii) all minimal sets and (iii) one minimal set. Generation of one minimal set using hardware is very fast.

Most methods use fault-wise information from ambiguity sets. Deviating from this philosophy, a new method using pairs of faults is proposed in Chapter IV. This is shown to have many advantages. In this method, a fault pair table is constructed with one row per fault pair. Methods are presented to generate valid sets and minimal sets. Binary nature of this table is exploited to present efficient techniques to generate these sets. A Boolean method is proposed to get all minimal sets of test nodes. A Boolean circuit is constructed, which is functionally similar to the Boolean circuit developed for fault-wise organisation. It is demonstrated that fault pair methods are well suited to hardware solutions. Therefore hardware schemes can be used gainfully to develop test equipment for test node selection.

A technique is proposed in chapter 5 to eliminate redundant frequencies generated by Seshu and Waxman's method using the methods developed for test node selection. A procedure is developed to select more frequencies when the set of frequencies suggested by their method is not sufficient to isolate faults. It is shown that fault dictionary can be constructed from the measurements of bandwidth and mid-band gain.

Chapter six delves in presenting efficient techniques for fault isolation phase using hardware, parallel and neural net approaches. All these methods separate faults in constant time. Hardware method employs binary coding of the fault-wise integer table. This results in multi input - multi output truth table. A Boolean circuit is realised using this truth table that can separate faults in constant time. Two hardware schemes are suggested to suit test equipment for fault isolation. They can accept field measurements and generate the corresponding binary codes. These codes are given as input to the Boolean circuit that can diagnose the faulty condition of the circuit. Parallel methods are also suggested using fixed or variable number of processors to isolate faults in constant time. Neural network approach is studied for fault isolation phase of analog circuits. Backpropagation (BP) and Radial basis function (RBF) networks are studied for doing this. A new method is proposed for fault isolation using RBF networks. A method to determine the width and centre of RBF units to account component tolerances is suggested. Data representation problems are addressed. A modification is suggested to the RBF network to accommodate novel faults. Performance of the BP and RBF network is compared in terms of learning speed, classification accuracy, data representation problems and response to novel faults in the context of fault isolation.

This page is intentionally left blank

CONTENTS

Title	Page
LIST OF FIGURES	**xi**
CHAPTER I: INTRODUCTION	**1**
1.1 Introduction	1
1.2 Methods of Analog Fault Diagnosis	3
1.2.1 SAT Methods	3
1.2.2 SBT Methods	7
1.3 Importance of Fault Dictionary	8
1.4 Review of SAT Methods	13
1.4.1 Parameter Identification Methods	13
1.4.2 Fault Verification Methods	16
1.4.3 Optimisation Methods	19
1.4.4 Fault Prediction	19
1.5 Review of SBT Methods	20
1.5.1 Fault Dictionary	20
1.5.1.1 Types of Stimuli and Measurements	20
1.5.1.2 Network Analysis	22
1.5.1.3 Selection of Test Measurements	23
1.5.1.4 Fault Isolation	25
1.5.2 Probabilistic Techniques	27
1.6 Definitions / Nomenclature	27
1.7 Scope of the Thesis	30
CHAPTER II: FAULT DICTIONARY-DIAGNOSABILITY CONSIDERATIONS	**35**
2.1 Introduction	35
2.2 Multiple excitations	36
2.2.1 Single excitation	37
2.2.2 Multiple excitations help	38
2.2.3 Single excitation with variable amplitudes	41
2.2.4 Multiple excitations with variable amplitudes	43
2.3 Impedance effects	47
2.3.1 Loading	47
2.3.2 Source Impedance	56

Title	Page
2.4 Tolerance Effects on Fault Dictionary	59
2.4.1 Computation of Tolerance Effects	60
2.4.2 Proposed Method	63
2.5 Conclusions	70
CHAPTER III: SELECTION OF TEST NODES USING FAULT-WISE TABLE	**71**
3.1 Introduction	71
3.2 Inclusion Method	72
3.2.1 Strategies for Inclusion	73
3.2.2 Inclusion Algorithm	76
3.3 Exclusion Method	78
3.3.1 Strategies for Exclusion	78
3.3.2 Exclusion Algorithm	79
3.4 Inclusion Method by Sort	80
3.5 Selection of Minimal Sets	90
3.5.1 Exclusion by Sort	90
3.5.2 Minimal Set from a Non-Minimal Set	94
3.5.2.1 Sorting Method	95
3.5.2.2 Intersection Method	97
3.6 Parallel Implementation	102
3.7 Test Equipment	106
3.7.1 Boolean Circuit for Test Node Selection	107
3.7.2 Generation of All Valid Sets	111
3.7.3 Generation of All Minimal Sets	113
3.7.4 Generation of One Minimal Set	117
3.8 Conclusions	119
CHAPTER IV: SELECTION OF TEST NODES USING FAULT PAIR TABLE	**123**
4.1 Introduction	123
4.2 Fault Pair Table and Its Importance	124
4.2.1 Construction of Fault Pair Table	125
4.2.2 Fault Pair Table and Ambiguity Sets	127
4.3 Inclusion Method	129
4.3.1 Strategy for Inclusion	129
4.3.2 Inclusion Algorithm	129

Title	Page

4.4 Exclusion Method 138
4.4.1 Strategy for Exclusion 139
4.4.2 Minimal Set Generation 140
4.4.3 Minimal Set from Non-Minimal Set 151

4.5 Faster Implementations 153
4.5.1 Generation of a Valid Set 154
4.5.2 Generation of a Minimal Set 157
4.6 Parallel Implementation 159
4.7 Generation of All Minimal Sets 161
4.8 Hardware Technique 164
4.8.1 Boolean Circuit for Test Node Selection 164
4.8.2 PLD Realisation from the Fault Pair Table 166
4.9 Conclusions 169

CHAPTER V: MULTI-FREQUENCY APPROACH TO FAULT DICTIONARY 173

5.1 Introduction 173
5.2 Selection of Test Frequencies 174
5.2.1 Redundant Frequencies 178
5.2.2 Generalised Procedure for Selection of Test Frequencies 181
5.3 Frequency Response Characteristics for Fault Dictionary 187
5.4 Conclusions 193

CHAPTER VI: ANALOG CIRCUIT FAULT ISOLATION 195

6.1 Introduction 195
6.2 Hardware Technique for Fault Isolation 196
6.2.1 Boolean Circuit for Fault Isolation 196
6.2.2 Hardware Schemes 201
6.3 Parallel Methods 205
6.4 Neural Networks for Fault Isolation 206
6.4.1 Backpropagation Neural Networks for Fault Isolation 215
6.4.2 Radial Basis Funcions Networks for Fault Isolation 226
6.4.3 Comparison of Neural Network approaches 242
6.5 Conclusions 244

Title	Page
CHAPTER VII: CONCLUSIONS	**247**
7.1 Contributions of the present work	247
7.2 Scope for further work	251
REFERENCES	**254**
APPENDIX	**273**
LIST OF PUBLICATIONS PERTAINING TO THE THESIS	**279**
BIO-DATA OF THE AUTHOR	**281**