CIRCULATING CURRENT AND LINE CURRENT RIPPLE REDUCTION FOR PARALLEL INTERLEAVED TWO-LEVEL VSIs

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by

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CERTIFICATE

It is certified that the thesis entitled "**Circulating Current and Line Current Ripple Reduction for Parallel Interleaved Two-Level VSIs**," being submitted by **Mr. Kapil Shukla** for award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of the student work carried out by him under my supervision and guidance. The matter embodied in this thesis has not been submitted for award of any other degree or diploma.

Dated:

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ABSTRACT

The voltage source inverters (VSIs) are conventionally connected in parallel to deliver higher amount of power. Along-with the higher power delivery, the parallel connected voltage source inverters have distinct advantages of reduced current stress on switches, modularity, better thermal management, easy maintenance, etc. The parallel connected VSIs could be modulated using the space-vector based approach or carrier based approach. In the carrier based approach, the high frequency carrier signals are compared with the low frequency reference signals to generate the gate pulses of individual VSIs. The carrier signals of individual VSIs are conventionally phase shifted by certain angles to lower the load side harmonics. This shifting of carrier signals is called as interleaving. However, this interleaving of carrier signals produces a common-mode voltage difference among the VSIs. This voltage difference between the VSIs connected with a common dc-link would provide a path for the current to flow. This current is called as circulating current. The circulating current flow could be restricted using the passive elements or active methods. The passive elements include transformers, common-mode inductors, coupling inductors, inter-phase inductors, whereas the active methods include pulse-width based modulation (PWM) techniques and current controllers.

The two parallel interleaved two-level VSIs are conventionally modulated using the two-level continuous or discontinuous PWM techniques. The impact of different two-level PWM techniques on the parallel interleaved VSIs performance indices such as circulating current, ac side line current ripple, and switching loss is already available in literature. However, the two parallel interleaved two-level VSIs could be analyzed as a single three-level VSI. Therefore, any three-level PWM technique could be implemented using the parallel interleaved two-level VSIs. The implementation of a three-level PWM technique would reduce the ac side line current ripple significantly as the three-level PWM technique utilized the three nearest vector of the equivalent space-vector diagram of the two parallel interleaved VSIs, whereas none of the conventional two-level PWM techniques utilize the three nearest vectors of the equivalent space-vector diagram of the two parallel interleaved VSIs. Different three-level continuous and discontinuous PWM techniques are implemented in this thesis using the two parallel interleaved two-level VSIs. Different methods to implement a three-level PWM technique are also explained in this

thesis. A thorough analysis on impact of different three-level PWM techniques on the system performance indices is also carried out. The practical implementation issues to implement the three-level PWM techniques using the parallel interleaved VSIs are also discussed.

The ac sides of the parallel interleaved VSIs are conventionally connected using the common-mode or differential-mode inductors to restrict the circulating current flow. Along with these inductors, line frequency inductors are also used to reduce the ac side line current ripple. Same value of inductors are normally connected in the ac sides of the VSIs. However, a mismatch could occur among the inductance values of the inductors due to factors such as ageing, tolerance, core properties, etc. This mismatch in inductor values would lead to a low frequency component in the circulating current. This low frequency circulating current could saturate the common-mode inductors. To suppress this low frequency circulating current, a modified common-mode offset based PWM technique is proposed in this thesis. A dynamic equation of circulating current is also derived during the unbalanced operating conditions.

सार

वोल्टेज स्रोत इनवर्टर (वी.एस.आई) पारंपरिक रूप से समानांतर में जुड़े होते हैं ताकि अधिक मात्रा में बिजली पहुंचाई जा सके। उच्च शक्ति वितरण के साथ-साथ, समानांतर जुड़े वोल्टेज स्रोत इनवर्टर में स्विचेस, प्रतिरूपता, बेहतर तापीय प्रबंधन, आसान रखरखाव, आदि पर कम वर्तमान तनाव के अलग-अलग फायदे हैं। समानांतर जुड़े वीएसआई को अंतरिक्ष-वेक्टर आधारित दृष्टिकोण या वाहक आधारित दृष्टिकोण का उपयोग करके संशोधित किया जा सकता है। वाहक आधारित दृष्टिकोण में, उच्च आवृत्ति वाहक संकेतों की तुलना व्यक्तिगत वीएसआई के गेट पल्स को उत्पन्न करने के लिए कम आवृत्ति संदर्भ संकेतों के साथ की जाती है। व्यक्तिगत वीएसआई के वाहक संकेतों को पारंपरिक रूप से लोड साइड हार्मोनिक्स को कम करने के लिए कुछ कोणों द्वारा स्थानांतरित किया जाता है। वाहक संकेतों के इस बदलाव को इंटरलेविंग कहा जाता है। हालांकि, वाहक संकेतों की यह इंटरलेविंग वीएसआई के बीच एक सामान्य-मोड वोल्टेज अंतर पैदा करती है। एक सामान्य डीसी-लिंक के साथ जुड़े वीएसआई के बीच यह वोल्टेज अंतर करंट प्रवाह के लिए एक मार्ग प्रदान करेगा। इस करंट को सर्कुलेटिंग करंट कहा जाता है। सर्कुलेटिंग करंट प्रवाह निष्क्रिय तत्वों या सक्रिय तरीकों का उपयोग करके प्रतिबंधित किया जा सकता है। निष्क्रिय तत्वों में ट्रांसफॉर्मर, सामान्य-मोड प्रेरक, युग्मन प्रेरक, अंतर-चरण प्रेरक शामिल हैं, जबकि सक्रिय तरीकों में पल्स-चौड़ाई आधारित मॉड्यूलेशन (पीडब्लूएम) तकनीक और करंट नियंत्रक शामिल हैं।

दो समानांतर इंटरलेव्ड दो-स्तरीय वीएसआई पारंपरिक रूप से दो-स्तरीय निरंतर या असंतुलित पीडब्लूएम तकनीकों का उपयोग करके संशोधित होते हैं। समानांतर इंटरलीव्ड वीएसआई प्रदर्शन सूचकांकों पर अलग-अलग दो-स्तरीय पीडब्लूएम तकनीकों का प्रभाव जैसे कि परिसंचारी धारा, एसी साइड लाइन करंट तरंग, और स्विचिंग नुकसान साहित्य में पहले से ही उपलब्ध है। हालांकि, दो समानांतर इंटरलेव्ड दो-स्तरीय वीएसआई का विश्लेषण एक एकल तीन-स्तरीय वीएसआई के रूप में किया जा सकता है। इसलिए, किसी भी तीन-स्तरीय पीडब्लूएम तकनीक को समानांतर इंटरलेव्ड दो-स्तरीय वीएसआई का उपयोग करके लागू किया जा सकता है। तीन-स्तरीय पीडब्लूएम तकनीक के कार्यान्वयन से एसी साइड लाइन करंट की तरंग में काफी कमी आएगी क्योंकि तीन-स्तरीय पीडब्लूएम तकनीक ने दो समानांतर इंटरलेव्ड वीएसआई के बराबर अंतरिक्ष-वेक्टर आरेख के तीन निकटतम वेक्टर का उपयोग किया, जबकि पारंपरिक दो-स्तरीय पीडब्लूएम तकनीक में से कोई भी दो समानांतर इंटरलेस्ड वीएसआई

के बराबर अंतरिक्ष-वेक्टर आरेख के तीन निकटतम वैक्टर का उपयोग नहीं करती है। इस थीसिस में दो समानांतर दो-स्तरीय वीएसआई का उपयोग करके विभिन्न तीन-स्तरीय निरंतर और असंतत पीडब्लूएम तकनीकों को लागू किया गया है। तीन-स्तरीय पीडब्लूएम तकनीक को लागू करने के विभिन्न तरीकों को भी इस थीसिस में समझाया गया है। सिस्टम प्रदर्शन सूचकांकों पर विभिन्न तीन-स्तरीय पीडब्लूएम तकनीकों के प्रभाव का गहन विश्लेषण भी किया गया है। समानांतर इंटरलीव्ड वीएसआई का उपयोग करके तीन-स्तरीय पीडब्लूएम तकनीकों को लागू करने के लिए व्यावहारिक कार्यान्वयन के मुद्दों पर भी चर्चा की गई है।

समानांतर इंटरलेव्ड वीएसआई के एसी साइड्स पारंपरिक रूप से सर्कुलेटिंग करंट प्रवाह को प्रतिबंधित करने के लिए सामान्य-मोड या अंतर-मोड प्रेरकों का उपयोग करके जुड़े हुए हैं। इन प्रेरकों के साथ, एसी साइड लाइन करंट रिपल को कम करने के लिए लाइन आवृत्ति प्रेरक का भी उपयोग किया जाता है। आमतौर पर समान मूल्य के प्रेरक वीएसआई के एसी पक्षों में जुड़े होते हैं। हालांकि, एक बेमेल उम्र बढ़ने, सहिष्णुता, कोर गुण, आदि जैसे कारकों के कारण प्रेरकों के अधिष्ठापन मूल्यों के बीच हो सकता है। यह बेमेल सर्कुलेटिंग करंट प्रवाह में कम आवृत्ति घटक को जन्म देता है। यह कम आवृत्ति वाला सर्कुलेटिंग करंट प्रवाह सामान्य-मोड प्रेरकों को संतृप्त कर सकता है। इस कम आवृत्ति सर्कुलेटिंग करंट को दबाने के लिए, इस थीसिस में एक संशोधित सामान्य-मोड ऑफसेट आधारित पीडब्लूएम तकनीक प्रस्तावित है। असंतुलित संचालन स्थितियों के दौरान सर्कुलेटिंग करंट प्रवाह का एक गतिशील समीकरण भी व्युत्पन्न किया गया है।

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2L	Two-level.
3L	Three-level.
AC	Alternating Current.
CM	Common-mode.
DC	Direct Current.
DM	Differential-mode.
DPWM	Discontinuous Pulse-width Modulation.
DSC	Digital Signal Controller.
DSO	Digital Storage Oscilloscope.
EPWM	Enhanced Pulse-width Modulation.
FFT	Fast Fourier Transform.
IGBT	Insulated-Gate Bipolar Transistor.
MDPWM	Modified Discontinuous Pulse-width Modulation.
NPC	Neutral-Point Clamped
PD	Phase Disposition.
PI	Proportional Integral.
PIR	Proportional Integral Resonant.
PWM	Pulse-width Modulation.
RMS	Root-mean Square.
SHEPWM	Selective Harmonic Elimination Pulse-width Modulation.
SPWM	Sinusoidal Pulse-width Modulation.
SVPWM	Space-vector Pulse-width Modulation.
THD	Total Harmonic Distortion.
VSI	Voltage Source Inverter.

LIST OF SYMBOLS

m_a	Modulation Index.
V_{dc}	DC-link Voltage
i_A	Phase A load current.
i_B	Phase B load current.
i_C	Phase C load current.
i_{A1}	Phase A current of VSI 1.
i_{A2}	Phase A current of VSI 2.
i_{B1}	Phase B current of VSI 1.
i_{B2}	Phase B current of VSI 2.
i_{C1}	Phase C current of VSI 1.
i_{C2}	Phase C current of VSI 2.
R_s	Internal resistance of line frequency inductor.
L_s	Inductance of line frequency inductor.
i_{CC}	Circulating current defined as the sum of three phase currents of individual VSIs.
$i_{CC,A}$	Circulating current defined as the difference of phase A currents of individual VSIs.
V_{ref}	Reference voltage vector.
T_s	Switching period.
$\mathbf{V}_1^{2L}$- $\mathbf{V}_6^{2L}$	Two-level active voltage vectors.
$\mathbf{V}_0^{2L}$- $\mathbf{V}_7^{2L}$	Two-level zero voltage vectors.
T_1	Dwell time of active voltage vector $\mathbf{V}_1^{2L}$.
T_2	Dwell time of active voltage vector $\mathbf{V}_2^{2L}$.
T_z	Dwell time of zero voltage vectors ($\mathbf{V}_0^{2L}$ and $\mathbf{V}_7^{2L}$).
$v_{A,ref}$	Phase A reference signal.
$v_{B,ref}$	Phase B reference signal.
$v_{C,ref}$	Phase C reference signal.
$v_{A1,ref}$	Updated phase A reference signal of VSI 1.
$v_{B1,ref}$	Updated phase B reference signal of VSI 1.

$v_{C1,ref}$	Updated phase C reference signal of VSI 1.
v_{max}	Maximum value of three phase reference signals.
v_{mid}	Middle value of three phase reference signals.
v_{min}	Minimum value of three phase reference signals
$v_{max1,ref}$	Maximum value of updated three phase reference signals of VSI 1.
$v_{min1,ref}$	Minimum value of updated three phase reference signals of VSI 1.
$v_{mid1,ref}$	Middle value of updated three phase reference signals of VSI 1.
$v_{mid2,ref}$	Middle value of updated three phase reference signals of VSI 2.
v_{A1O}	Phase A pole voltage of VSI 1.
v_{A2O}	Phase A pole voltage of VSI 2.
v_{AO}	Phase A equivalent pole voltage.
v_{B1O}	Phase B pole voltage of VSI 1.
v_{B2O}	Phase B pole voltage of VSI 2.
v_{BO}	Phase B equivalent pole voltage.
v_{C1O}	Phase C pole voltage of VSI 1.
v_{C2O}	Phase C pole voltage of VSI 2.
v_{CO}	Phase C equivalent pole voltage.
$v_{cm,1}$	Common-mode voltage of VSI 1.
$v_{cm,2}$	Common-mode voltage of VSI 2.
v_{off}	Common-mode offset signal.
$P_{SUB,TOT}$	Normalized total switching loss.
v_{AB}	Line-line voltage.
v_{A1N}	Generated phase A voltage of VSI 1.
v_{A2N}	Generated phase A voltage of VSI 2.
v_{AN}	Load voltage of phase A.
v_{B1N}	Generated phase B voltage of VSI 1.
v_{B2N}	Generated phase B voltage of VSI 2.
v_{BN}	Load voltage of phase B.
v_{C1N}	Generated phase C voltage of VSI 1.

v_{C2N}	Generated phase C voltage of VSI 2.
v_{CN}	Load voltage of phase C.
R_{A1}	Internal resistance of line frequency inductor of phase A of VSI 1.
R_{B1}	Internal resistance of line frequency inductor of phase B of VSI 1.
R_{C1}	Internal resistance of line frequency inductor of phase C of VSI 1.
R_{A2}	Internal resistance of line frequency inductor of phase A of VSI 2.
R_{B2}	Internal resistance of line frequency inductor of phase B of VSI 2.
R_{C2}	Internal resistance of line frequency inductor of phase C of VSI 2.
L_{A1}	Inductance of line frequency inductor of phase A of VSI 1.
L_{B1}	Inductance of line frequency inductor of phase B of VSI 1.
L_{C1}	Inductance of line frequency inductor of phase C of VSI 1.
L_{A2}	Inductance of line frequency inductor of phase A of VSI 2.
L_{B2}	Inductance of line frequency inductor of phase B of VSI 2.
L_{C2}	Inductance of line frequency inductor of phase C of VSI 2.
p_{A1}	Percentage increment value for the internal resistance of line frequency inductor of phase A of VSI 1.
p_{B1}	Percentage increment value for the internal resistance of line frequency inductor of phase B of VSI 1.
p_{C1}	Percentage increment value for the internal resistance of line frequency inductor of phase C of VSI 1.
p_{A2}	Percentage increment value for the internal resistance of line frequency inductor of phase A of VSI 2.
p_{B2}	Percentage increment value for the internal resistance of line frequency inductor of phase B of VSI 2.
p_{C2}	Percentage increment value for the internal resistance of line frequency inductor of phase C of VSI 2.
q_{A1}	Percentage increment value for the inductance of line frequency inductor of phase A of VSI 1.
q_{B1}	Percentage increment value for the inductance of line frequency inductor of phase B of VSI 1.
q_{C1}	Percentage increment value for the inductance of line frequency inductor of phase C of VSI 1.
q_{A2}	Percentage increment value for the inductance of line frequency inductor of phase A of VSI 2.
q_{B2}	Percentage increment value for the inductance of line frequency

inductor of phase B of VSI 2.

q_{C2}	Percentage increment value for the inductance of line frequency inductor of phase C of VSI 2.
i_{dref1p}	d-axis reference current for VSI 1 in positive synchronous reference frame.
i_{dref2p}	d-axis reference current for VSI 2 in positive synchronous reference frame.
i_{qref1p}	q-axis reference current for VSI 1 in positive synchronous reference frame.
i_{qref2p}	q-axis reference current for VSI 2 in positive synchronous reference frame.
i_{dref1n}	d-axis reference current for VSI 1 in negative synchronous reference frame.
i_{dref2n}	d-axis reference current for VSI 2 in negative synchronous reference frame.
i_{qref1n}	q-axis reference current for VSI 1 in negative synchronous reference frame.
i_{qref2n}	q-axis reference current for VSI 2 in negative synchronous reference frame.
v_{Ldp}	d-axis load voltage in positive synchronous reference frame.
v_{Lqp}	q-axis load voltage in positive synchronous reference frame.
v_{Ldn}	d-axis load voltage in negative synchronous reference frame.
v_{Lqn}	q-axis load voltage in negative synchronous reference frame.