REUSING DESIGN-FOR-DEBUG HARDWARE TO ENHANCE PERFORMANCE

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Certificate

This is to certify that the thesis titled **Reusing Design-For-Debug Hardware to Enhance Performance** being submitted by **Miss Neetu Jindal** for the award of **Doctor of Philosophy** in Computer Science and Engineering is a record of bona fide work carried out by her under my guidance and supervision at the Department of Computer Science and Engineering, Indian Institute of Technology Delhi. The work presented in this thesis has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma.

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To My Family

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Neetu Jindal

Abstract

Decreasing feature sizes have caused ever increasing levels of on-chip component integration. The simulation or emulation used in pre-silicon validation can take a prohibitive amount of time to check for functional errors. During post-silicon validation, applications are executed on the chip prototype at native speeds and are analyzed using dedicated design-for-debug (DFD) hardware, enabling the discovery of functional bugs that may have slipped past pre-silicon validation. Post-silicon validation represents one of the most crucial and expensive components of the systems-on-chip validation methodology. It is performed under a highly aggressive schedule to satisfy time-to-market requirements. The DFD hardware is used to record the state history of important signals in the chip that could be critical in debugging the chip. The design of the DFD structure is non-trivial because it has to maximize the visibility while operating under very stringent area constraints, since it may become vestigial once the chip is in production. The simplest DFD structure is the trace buffer which consists of memory elements and records the values of signals deemed critical by the designer. These recorded signals can be extracted outside the chip and analyzed to determine the root cause of errors. With increasing complexity and higher levels of integration of modules on a single chip, the area consumed by DFD structures increases significantly. This is a challenge for the chip manufacturers because they have to strike a balance between the visibility and the area allocated to DFD structures. The two goals are competing; increasing visibility enables faster validation, but also increases the area overhead of the DFD hardware, which may become unusable when the chip goes into production (i.e., normal operation in field).

In this thesis, we address the above problem by repurposing the Design-for-Debug hardware through reusing it in-field to enhance the underlying architecture. Our novel design essentially leads to a win-win situation that is substantially advantageous for both validation and performance. This dissertation presents and evaluates three novel reusability scenarios of the validation hardware. In the first approach, we propose to reuse the core trace buffer as a victim cache that can be dynamically partitioned among multiple threads using machine learning algorithms. In the second approach, we propose a scheme AugVC to reuse trace buffers to augment the router buffer, with the objective of improving the overall network performance.

Further, we propose an architectural framework for runtime monitoring of program assertions, called DHOOM, which exploits the combination of a reconfigurable fabric present alongside a processor core, with the on-chip Design-for-Debug hardware. This combination of hardware features allows DHOOM to minimize the overall performance overhead of runtime verification, subject to a given area constraint. We present an algorithm for dynamically selecting an effective subset of assertion monitors that can be accommodated in the available programmable fabric, while instrumenting the remaining assertions in software.

संक्षेप

ट्रांजिस्ट आकार के घटने के कारण ऑन-चिप घटक एकीकरण का स्तर बड़ा है। प्री-सिलिकॉन सत्यापन में उपयोग किए गए सिमुलेशन या अनुकरण कार्यात्मक त्रुटियों की जांच करने के लिए एक निषेधात्मक मात्रा ले सकते हैं। सिलिकॉन के बाद के सत्यापन के दौरान, अनुप्रयोगों को मूल गति पर चिप प्रोटोटाइप पर निष्पादित किया जाता है और समर्पित डिज़ाइन-फॉर-डीबग हार्डवेयर का उपयोग करके विश्लेषण किया जाता है, जो उन कार्यात्मक त्रुटियों की खोज को सक्षम करता है जो पिछले प्री-सिलिकॉन में रह गए हों । पोस्ट-सिलिकॉन सत्यापन सिस्टम-ऑन-चिप सत्यापन पद्धति के सबसे महत्वपूर्ण और महंगे घटकों में से एक का प्रतिनिधित्व करता है। यह बाजार की आवश्यकताओं को पूरा करने के लिए एक अत्यधिक आक्रामक कार्यक्रम के तहत किया जाता है।डिज़ाइन-फॉर-डीबग हार्डवेयर का उपयोग चिप में महत्वपूर्ण संकेतों के इतिहास को रिकॉर्ड करने के लिए किया जाता है जो चिप को संशोधित करने में महत्वपूर्ण हो सकते है। डिज़ाइन-फॉर-डीबग हार्डवेयर की संरचना गैर-तुच्छ है क्योंकि इसमें बहुत कड़े क्षेत्र की बाधाओं के तहत काम करते समय दृश्यता को अधिकतम करना पड़ता है, क्योंकि चिप के उत्पादन के बाद यह अवशिष्ट हो सकता है। सरलतम डिज़ाइन-फॉर-डीबग हार्डवेयर ट्रेस बफर है जिसमें मेमोरी तत्व होते हैं और डिजाइनर द्वारा बताए गये महत्वपूर्ण संकेतों के मूल्यों को रिकॉर्ड करता है। इन रिकॉर्ड किए गए संकेतों को चिप के बाहर निकाला जा सकता है और त्रुटियों के मूल कारण को निर्धारित करने के लिए विश्लेषण किया जा सकता है। बढ़ती जटिलता और एकल चिप पर मॉड्यूल के एकीकरण के उच्च स्तर के साथ डिज़ाइन-फॉर-डीबग हार्डवेयर के क्षेत्र में काफी वृद्धि होती है। चिप निर्माताओं के लिए यह एक चुनौती है क्योंकि उन्हें दृश्यता और डिज़ाइन-फॉर-डीबग हार्डवेयर की संरचनाओं को आवंटित क्षेत्र के बीच एक संतुलन बनाना है। दो लक्ष्य प्रतिस्पर्धा कर रहे हैं; बढ़ती दृश्यता तेजी से सत्यापन को सक्षम करती है, लेकिन डिज़ाइन-फॉर-डीबग हार्डवेयर के क्षेत्र को भी बढ़ाती है, जो चिप के उत्पादन (यानी, क्षेत्र में सामान्य संचालन) में जाने पर अनुपयोगी हो सकता है।

इस शोध में, हम अंतर्निहित आर्किटेक्चर को बढ़ाने के लिए डिज़ाइन-फॉर-डीबग हार्डवेयर को इन-फील्ड में पुन: उपयोग के माध्यम से उपरोक्त समस्या का समाधान करते हैं। हमारा डिजाइन अनिवार्य रूप से एक जीत-जीत की स्थिति की ओर जाता है जो सत्यापन और प्रदर्शन दोनों के लिए काफी फायदेमंद है। यह शोध प्रबंध सत्यापन हार्डवेयर के तीन पुन: प्रयोज्य परिदृश्यों को प्रस्तुत करता है और उनका मूल्यांकन करता है।पहले दृष्टिकोण में, हम कोर ट्रेस बफर का पुन: उपयोग विक्टिम कॅश के रूप में प्रस्तुत करते हैं जिसे मशीन लर्निंग एल्गोरिदम का उपयोग करके कई थ्रेड्स के बीच गतिशील रूप से विभाजित किया जा सकता है। दूसरे दृष्टिकोण में, हम ट्रेस बफ़र्स को पुन: उपयोग में लाने के लिए एक योजना औगवीसी का प्रस्ताव करते हैं जिसमे राउटर बफर दवारा समग्र नेटवर्क प्रदर्शन को बेहतर बनाते है।

इसके अलावा, हम कार्यक्रम के अभिकथन की निगरानी के लिए एक वास्तुशिल्प रूपरेखा का प्रस्ताव करते हैं, जिसे धूम कहा जाता है, जो एक साथ मौजूद पुन: प्रयोज्य चिप व डिज़ाइन-फॉर-डीबग हार्डवेयर के संयोजन का फायदा उठाता है। हार्डवेयर का यह संयोजन रनटाइम सत्यापन के समग्र प्रदर्शन के ओवरहेड को कम करने की अनुमति देता है, जो किसी दिए गए क्षेत्र की बाधा के अधीन है। हम सॉफ्टवेयर में शेष अभिक्रियाओं को लिखत करते समय उपलब्ध प्रोग्रामेबल फैब्रिक में समायोजित किए जा सकने वाले मॉनिटर के प्रभावी उपसमुच्चय का चयन करने के लिए एक एल्गोरिथम प्रस्तुत करते हैं।

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