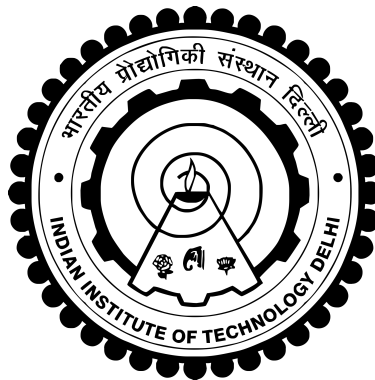


DESIGN AND ANALYSIS OF HYBRID CMOS-OXRAM NON-VOLATILE SRAM (NVSRAM)

SWATILEKHA MAJUMDAR



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY DELHI
MAY 2020

DESIGN AND ANALYSIS OF HYBRID CMOS-OXRAM NON-VOLATILE SRAM (NVSRAM)

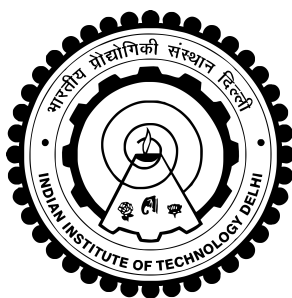
by

Swatilekha Majumdar

DEPARTMENT OF ELECTRICAL ENGINEERING

submitted

in fulfillment of the requirements of the degree of Doctor of Philosophy



INDIAN INSTITUTE OF TECHNOLOGY DELHI

MAY 2020

Dedicated to

My grandparents, whom I know will forever guide me from heaven. Maa and Baba, who are pillars of my strength and my constant inspiration. Without their love and care I would not have come so far. Anulekha, my sister who has supported me in thick and thin. All my teachers, who have inspired me to dream and get up whenever I fail. And lastly, my best friend Supriya. I thank you from the bottom of my heart.

कर्मण्येवाधिकारस्ते मा फलेषु कदा चन ।
मा कर्मफलहेतुर्भूर्मा ते सङ्गो ऽस्वकर्मणि ॥ २-४७ ॥

karmaṇy evādhikāras te mā phaleṣu kadā cana ।
mā karmaphalahetur bhūr mā te saṅgo 'stv akarmaṇi ॥2-47॥

- *Shrimad Bhagwad Gita, Chapter 2, Verse 47*

বাংলা: আপনার নির্ধারিত দায়িত্ব পালনের অধিকার আপনার রয়েছে, তবে আপনি নিজের কর্মের ফলের অধিকারি নন। নিজেকে কখনই আপনার ক্রিয়াকলাপের ফলাফলের কারণ হিসাবে বিবেচনা করবেন না এবং নিষ্ক্রিয়তা সাথে সংযুক্ত থাকবেন না।

हिंदी: आपको अपने निर्धारित कर्तव्यों को निभाने का अधिकार है, लेकिन आप अपने कार्यों के फल के हकदार नहीं हैं। कभी भी अपने आप को अपनी गतिविधियों के परिणामों का कारण न समझें, न ही निष्क्रियता से जुड़े रहें।

English: You have a right to perform your prescribed duties, but you are not entitled to the fruits of your actions. Never consider yourself to be the cause of the results of your activities, nor be attached to inaction.

CERTIFICATE

This is to certify that the thesis entitled “**Design and Analysis of Hybrid CMOS-OxRAM Non-Volatile SRAM (NVS RAM)**” being submitted by Ms. **Swatilekha Majumdar** for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by her under my supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

Place: New Delhi
Date:

Dr. Manan Suri
Assistant Professor
Department of Electrical Engineering
Indian Institute of Technology, Delhi
Hauz Khas, New Delhi- 110016, India

ACKNOWLEDGEMENTS

This thesis does not mark an end to my journey but a new beginning in the path of my thirst for knowledge. The thesis has been kept on track and has been pushed continuously towards a successful completion with the support, help and encouragement of numerous people which includes my well-wishers, colleagues and various institutions. Although I will try to name everyone, who directly or indirectly contributed to the completion of this thesis, in case I miss out on someone, I sincerely ask for your forgiveness in advance.

Official:

Firstly, I would like to express my sincere gratitude to my advisor **Prof. Manan Suri** for the continuous support of my PhD study and related research, for his patience, motivation, and immense knowledge. His guidance helped me in all the time of research and writing of this thesis. He was kind enough to take me under his supervision when I was in the midst of a professional crisis. Apart from academics, his valuable teachings on leading a pure, spiritual and disciplined life along with constant philanthropic motivations are something that I look forward to inheriting. I could not have imagined having a better advisor and mentor for my PhD study.

Besides my advisor, I would like to thank the Student Review Committee (SRC) members: Prof. Shouribrata Chatterjee, Prof. Preeti Ranjan Panda, and Prof. Bhaskar Mitra, for their insightful comments and encouragement. I am thankful to them for raising some valuable questions during every review process, which motivated me to widen my research from various perspectives. Additionally, my sincere thanks go to Prof. Tuo-Hung (Alex) Hou from NanoST Lab, National Chiao Tung University, Taiwan, who provided me with an opportunity to join his team as an intern during my visit as an exchange student. He was kind enough to give access to his laboratory and research facilities, and also provide us with devices that were utilized for study in the thesis. I would also like to thank Dr. Boris Hudec (Post-doctorate at NCTU, Taiwan), Mr. V. Mani Teja (Postgraduate at NCTU, Taiwan currently enrolled as a Ph.D. student at KAUST, UAE), Mr. Paritosh Sahu (Postgraduate

student at NCTU, Taiwan currently working at TSMC, Taiwan), Mr. Che Chia Chang (PhD scholar at NCTU, Taiwan) and Ms. Ying Chen (Graduated from NCTU, Taiwan) for their constant and rigorous discussions related to the studies performed in this thesis. Without their precious support, it would not be possible to conduct this research.

I would also like to thank Prof. Basabi Bhowmik and Prof. M. Jagadesh Kumar, who taught courses on MOS-VLSI and Microelectronics respectively. These courses helped me in better connecting the dots between devices and circuit designs. Furthermore, I am grateful to Dr. Kaushik Saha (CTO, Samsung Electronics, India) for teaching a very valuable course on Memory Design and Testing and also appreciating me in all the work that I have done.

I also thank my fellow lab-mates, specially Supriya Chakraborty, Sai Sukruth Bezugam, Abhilash Garg, Manoj Kumar, and Tinish Bhattacharya, for the stimulating discussions, for the sleepless nights we were working together before deadlines, and for all the fun we have had in the last five years.

Lastly, I would like to thank Dr. Turbo Majumder, who undertook me as a doctoral student at IIT Delhi. Although I could not work with him for long, his guidance and support meant a lot to me during my early days of research.

Unofficial:

I would like to express my sincere gratitude to my fellow PhD colleagues, with special mention to Atul Thakur, Rajib Ghosh, Supriya Chakraborty, Shubham Sahay, Abhilash Garg, Manoj Kumar; my juniors at IIT Delhi, Sai Sukruth Bezugam and Salam Thoi Thoi Singh; and my colleagues Alok and V. Mani Teja, for being my pillars of support and being my agony aunt whenever I needed them. They have helped me create memories I will cherish my entire life.

Last but not least, I would like to thank my parents for making me who I am. Words fail me while conveying my indebtedness to them for showering eternal love, care and support, without which none of the accomplishments would have been its worth. I would also like to thank my sister, Anulekha, for being there when I needed her the most.

Swatilekha Majumdar

New Delhi, India

ABSTRACT

Advances in silicon technology have enabled the semiconductor industry to shrink the area of a transistor by roughly a factor of two with each successive technology node. This trend has continued unabated for the past five decades and has made computing devices ubiquitous in modern culture. Due to continuous advances in CMOS technology fueled by a growing and fiercely competitive market, there have been sustained innovations in the field of memory devices and circuits. This has led to a very advanced and hybrid computer memory hierarchy. Leading technology reports have shown the growing importance of memory in overall system architecture. Therefore, development in optimizing memory designs and schemes has been a primary criterion for computer architecture engineers. SRAM is typically used to realize memory due to its high speed of operation. Unlike DRAM, where the data is stored as a charge on the capacitor and needs constant refreshing, SRAM uses digital logic to store the data in its internal node. The requirement of a refresh scheme gives rise to additional circuitry and timing requirements, leading to complicated modules for DRAM memory. On the other hand, SRAM modules are more straightforward compared to DRAM, which makes it easier for design engineers to create an interface to access the memory.

However, almost all implementations of conventional SRAM circuits in literature are volatile. SRAM circuits lose data during the power-down state and thus need a hold voltage to maintain the memory state. This results in significant leakage power and energy dissipation. Various schemes, such as power gating, has been proposed to mitigate such issues. In power gating, a low voltage (hold voltage) is used for volatile memory to retain data while all logic circuits are turned off. However, even maintenance of this hold voltage (during power-down mode) in high-performance processing units leads to colossal power dissipation. Moreover, such schemes add more on-chip area and the supply scaling affects the stability performance of the bit-cells. Even worse, during unexpected power failures, the data in volatile memory may be lost, and computation tasks restart. Thus, it is essential to introduce non-volatility in these memories. Traditional non-volatile schemes use a backup

memory block (Flash), where data is off-loaded to it from SRAM block when a power-down signal is applied. However, this technique degrades memory performance, as more data transfers are required. Multiple circuits have been proposed in the literature to backup data from on-chip memory (SRAM), FFs and register to off-chip non-volatile memory (NVM) such as PCM, OxRAM, MRAM, thus preserving the system state in case of power failures. OxRAM devices have several advantages over other existing non-volatile memory solutions, such as low fabrication cost, fabrication at the back-end, manufacturing in vias along with its property of being non-volatile.

All the NVSRAM designs proposed in the literature are based on ‘*last bit non-volatility*’ and requires a controlled power-down signal to manage the data off-loading. This increases routing congestion and sophisticated control signal mechanisms. In this thesis, we present a ‘real-time non-volatile’ SRAM (NVSRAM) cell based on oxide-based random access memory (OxRAM) devices. This thesis explores the programming scheme of NVSRAM, optimizing the cell for faster and power-efficient performance, analyzing the stability of the cell which will determine the reliability of the memory design, advantages when using the proposed NVSRAM at a system level, and studies the implications on performance parameters when NVSRAM is used in last level cache. The thesis also covers the electrical characterization and modelling of various OxRAM devices to understand the device behaviour under different operating conditions.

सार

मूर के लॉ के अंतर्गत, पिछले चार-पांच दशकों से सिलिकॉन प्रौद्योगिकी में हुई प्रगति के कारण ट्रांजिस्टर के भूमिगत क्षेत्रफल में हर अठारह महीनों में लगभग पचास फीसदी की कमी दर्ज हुई है। सिलिकॉन ट्रांजिस्टर के न्यूनतम क्षेत्रफल तथा ऊर्जा उपभोग में आई कमी के कारण ही आधुनिक इलेक्ट्रॉनिक तथा कंप्यूटिंग उपकरण वर्तमान रूप में सर्वव्यापी हुए हैं। प्रतिस्पर्धात्मिक तथा वर्तमान बाजार द्वारा पोषित सिमोस (CMOS) टेक्नोलॉजी में हुई प्रगति के कारण, मेमोरी डीवाइसेस तथा सर्किट के क्षेत्र में सतत आविष्कार हुए हैं। अग्रणी प्रौद्योगिकी रिपोर्टों ने कंप्यूटर आर्किटेक्चर में मेमोरी के बढ़ते महत्व को दिखाया है इसीलिए, मेमोरी डिज़ाइन और योजनाओं के क्षेत्र में विकास, डिज़ाइन अभियंताओं के लिए एक प्राथमिक मापदंड रही है। एसराम (SRAM) के तीव्र संचालन और पेरिफेरल सर्किट की सुगम सुसंगतता के कारण वर्तमान मेमोरी के क्षेत्र में इसका उपयोग बहुव्यापी है। हालांकि एसराम डिजिटल लॉजिक की सहायता से डाटा को संग्रह करता है, किन्तु पारम्परिक एसराम सेल डिज़ाइन पॉवर-डाउन के पश्चात डाटा संग्रहण में सक्षम नहीं है। किसी भी समय एसराम मेमोरी से बिजली की कटौती, संग्रहित डाटा को लुप्त कर देता है। पारंपरिक एसराम में पॉवर-डाउन के पश्चात डाटा संग्रह की इस प्रमुख चुनौती की वजह से एनवीएसराम (NVS RAM) की आवश्यकता प्रतीत होती है। आज तक मेमोरी डिज़ाइन में नॉन-वोलैटिलिटी को लागु करने के लिए विभिन्न योजनाओं का प्रयोग किया गया है, जिसमें पॉवर-गैटिंग तथा फ्लैश (Flash) मेमोरी में डाटा को ऑफ-लोड करने की प्रक्रिया सबसे ज़्यादा प्रचलित है। परन्तु ऊर्जा उपभोग और जियोमेट्रिक क्षेत्रफल, उपरोक्त वर्णित योजनाओं के सम्मुख प्रमुख चुनौतियाँ हैं। इन समस्याओं के समाधान हेतु इमर्जिंग नॉन वोलेटाइल मेमोरी डीवाइसेस पर अनुसंधान एवं विकास कार्य सतत जारी है। फ्लैश डीवाइसेस की तरह चार्ज का प्रयोग न करते हुए उपरोक्त वर्णित डीवाइसेस अपने रेजिस्टेंस में परिवर्तन की वजह से डाटा को समाहित करती है। इनमें से एक नयी टेक्नोलॉजी जिसे हम ऑक्सराम (OxRAM) मेमोरी के नाम से जानते हैं, वैज्ञानिक दृष्टिकोण से आशाजनक है। एसराम को ई-एनवीएम (eNVM) के उपयोग से नॉन वोलेटाइल बनाने के लिए वर्तमान में विभिन्न शोधकार्य किये गए हैं, लेकिन ये सब एनवीएसराम केवल आखरी डाटा संग्रहण में सक्षम है। इस चुनौती को ध्यान में रखते हुए हमने इस शोध प्रबंध में एक ऐसे एनवीएसराम का उल्लेख तथा विश्लेषण किया है जो न केवल एसराम को नॉन वोलेटाइल बनाता है, बल्कि उस एसराम के सभी डाटा को हमेशा के लिए संग्रह करने की क्षमता भी प्रदान करता है। प्रस्तावित एनवीएसराम में चार ट्रांजिस्टर और दो ओक्सराम डीवाइसेस (4T2R) का उपयोग किया

गया है। इसके साथ हमने प्रस्तावित सेल डिज़ाइन की विश्वसनीयता और अनुकूलित कार्यचालन पर भी विस्तारपूर्वक उल्लेख किया है। अंत में हमने इस प्रस्तारित एनवीएसराम को आईओटी (IoT) एप्लीकेशन में इस्तेमाल हुए आखरी स्तरीय कैश के रूप में इसके प्रयोग का विश्लेषण किया है।

Contents

ACKNOWLEDGEMENTS	i
ABSTRACT	iii
LIST OF FIGURES	xxi
LIST OF TABLES	xxiii
1 Introduction	1
1.1 Semiconductor Memory Market	1
1.2 Memory Hierarchy	7
1.3 Static Random Access Memory (SRAM)	11
1.3.1 Importance of SRAM	11
1.3.2 Conventional 6T SRAM bitcell	12
1.3.3 Scaling Trends of SRAM	13
1.3.4 Design challenges in 6T SRAM	13
1.4 Why Non-volatile Caches are needed	15
1.5 Methodologies to make SRAM non-volatile	17
1.5.1 Device Modifications	18
1.5.2 Circuit Modifications	19
1.6 Emerging Non-volatile Memory Devices	20
1.6.1 Why OxRAM for NVSRAM?	21
1.7 Thesis Contributions and Organization	25
2 OxRAM Electrical Characterization	27
2.1 Oxide-Based Random Access Memory (OxRAM)	27
2.1.1 Introduction	27
2.1.2 Classification of OxRAM Devices	29
2.2 Test Equipment and Experimental Setup	35

2.3	Filamentary OxRAM Device: Ni/HfO _x /TiN	36
2.3.1	Device Fabrication	37
2.3.2	Electrical Characterization	37
2.3.3	Characterization Comparison with some other Published Data . . .	42
2.4	Non-filamentary Device: Ni/HfO _x /TiO ₂ /TiN	44
2.4.1	Device Fabrication	45
2.4.2	Electrical Characterization	45
2.4.3	Characterization Comparison with some other Published Data . . .	53
2.5	Summary	56
3	Electrical Compact Modelling of OxRAM	57
3.1	Filamentary OxRAM Model: Background Study	57
3.2	Modified Filamentary Model	59
3.3	Model for Non-filamentary OxRAM	61
3.3.1	Background Study	62
3.3.2	Proposed RC Circuit Based Electrical Model	64
3.4	Conclusion	74
4	Real-time NVSRAM	75
4.1	Existing NVSRAM architectures and Their Limitations	75
4.2	Proposed 4T2R ‘Real-time’ NVSRAM	77
4.3	Operating Modes of 4T2R NVSRAM	78
4.3.1	Write Mode	78
4.3.2	Read Mode	79
4.4	Improving power and energy of NVSRAM cell	81
4.4.1	HRS1-HRS2 Scheme for 4T-2R NVSRAM	82
4.5	Architectural Analysis of NVSRAM	84
4.6	Drawbacks	86
4.7	Optimized Programming scheme for 4T-2R NVSRAM	86
4.8	Operating Modes	86
4.8.1	Write Mode	87
4.8.2	Read Mode	90

4.9	Analysis of the proposed programming scheme	91
4.9.1	Impact of peak amplitudes of BL and PL	91
4.9.2	Impact of the duration of Rising/Falling edge of PL	93
4.10	Discussion and Summary	95
5	Stability Analysis of the 4T-2R NVSRAM	100
5.1	Introduction	100
5.2	Parameters to Analyze Stability of NVSRAM bit-cell	101
5.2.1	Static Noise Margin (SNM)	101
5.2.2	N-curve Method	103
5.3	Effect of OxRAM Variability on Stability	106
5.3.1	Effect on Static Noise Margin (SNM)	106
5.3.2	Effect on N-curve parameters	108
5.4	Summary	111
6	Utilization of NVSRAM as an NVFF	112
6.1	Background Study	112
6.2	Real-time NV-FF based on 4T-2R NV-SRAM circuit	115
6.3	Operating Modes of the Real-Time NV-FF	116
6.4	Limitations of Real-time NVFF	118
6.5	Modified NV-FF Design for Improved Performance	120
6.6	Operating Modes of the Proposed NV-FF	122
6.7	Summary	125
7	Optimizing Cache with NVSRAM	127
7.1	Introduction	127
7.2	Wireless Sensor Nodes	127
7.3	Emerging NVM devices used for study	128
7.3.1	Spin-transfer Torque MRAM (STT-MRAM)	128
7.3.2	Phase-Change Memory (PCM)	130
7.4	Benchmarks for SRAM/NVSRAM as LLC	131
7.4.1	Proposed Unified Memory Architecture	131
7.4.2	Experimental Setup for Benchmarking	131

7.4.3	Memory profiling results	137
7.5	Discussion and analysis	139
7.5.1	Solutions to limitations of NVM for unified-memory architectures in the context of IoT-WSN	140
7.5.2	Performance of NVM based NVSRAM for unified-memory in IoT- WSN	142
7.5.3	Implications of technology evolution	144
7.6	Conclusion	145
8	Conclusion	147
8.1	Summary	147
8.2	Future and On-going Work	149
8.2.1	Fabrication of 4T-2R NVSRAM	150
8.2.2	The Road Ahead	152
A	Voltage evolution in RC model	153

List of Figures

1.1	A plot of MOS transistor counts for microprocessors against dates of introduction (Source: Wikipedia).	2
1.2	The constant-field scaling theory predicts increased speed and lower power consumption of MOS transistors when the critical dimensions are scaled down [198].	3
1.3	Vicious cycle of semiconductor industry showing progress in development of technology nodes (Source: ITRS).	3
1.4	Evolution of memory and computer technologies due to revolution in the field of transistor scaling and performance improvement (a) Vacuum tube based UNIVAC computer (1953) that provided a memory of 1000 12-character words with an average access time of 300 μ s (b) IBM305 computer was the first commercial computer that used a moving-head hard disk drive, launched in 1956 which was able to store the equivalent of 64,000 punched cards (c) The University of Manchester Atlas in January 1963 with core storage of 96 kB and ROM of 8 kB (d) The die from an Intel 8742 (1971) with a 40-byte RAM (e) Intel 8088 used in IBM 5150 PC launched in August 1981 (1 MB memory using 29,000 transistors) (f) Apple A11 micrograph (2017) with 3 GB RAM used in recently launched iPhone X (Source: Google).	4
1.5	Estimated Global Semiconductor Market share (in US \$) trends for 2015-2025 (Source: Semi [91]).	5
1.6	Silicon area consumed by logic (blue and orange) vs. memory (green) (Source: Semico Research)	6
1.7	Market trends showing (a) Revenue market share and production capacity for major NOR and NAND Flash memory, respectively, for various suppliers. (b) Global memory chip market trend as predicted in the recent ‘Allied Market Research’ Report published in 2019 (https://www.alliedmarketresearch.com/memory-chip-market).	6
1.8	Unisantis and Imec claim to have designed a smaller SRAM bitcell than Samsung, Intel and TSMC. (Images: Imec).	7
1.9	(a) 7nm FinFET based SRAM as proposed by Samsung in ISSCC’18 [177] (b) 6T SRAM Area trends in recent publications (all fabricated) (c) SEM and scanning capacitance microscope (SCM) images of the 1T SRAM cell proposed by Zeno [69]. The memory device is fabricated in 28 nm process.	8
1.10	Memory Hierarchy showing different levels. Memories at the top are fast whereas memories at the bottom are dense, cheap and slow.	9

1.11	Cache Hierarchy showing private L1 and L2 caches and shared L3/LLC cache [188]	11
1.12	Chip die micrograph for (a) NVIDIA Jetson AGX Xavier (https://www.nvidia.com/en-us/autonomous-machines/embedded-systems/jetson-agx-xavier/) (b) Apple A9 core processor (Image Source: AnandTech). The memory hierarchy sections (L1, L2, L3, core) are marked on the micrograph.	12
1.13	SRAM based memory array and the conventional 6T SRAM bit-cell	13
1.14	(a) Trend in SRAM cell size with scaling based on published cell sizes (b) SRAM scaling trends as shown in recent ISSCC'19 paper by Fujiwara et al. [59]. DP SRAM signifies dual port SRAM.	14
1.15	(a) Leakage current projections for SRAM cell at different technology nodes. (b) Leakage power contribution in the total power consumption for a 1MB SRAM based cache across different technology node. The simulations were obtained from NVSim tool for 2-way associative cache with 64 bit data bus.	15
1.16	Power gating techniques in typical 6T SRAM cells (a) PMOS gating (b) NMOS gating (c) Dual gating (d) Conventional handshaking and pipeline architecture to control the gating scheme in 6T SRAM cell array [123]. . .	16
1.17	Reduction of power parameters (@ 10Mbps Input Rate) of (a) Short-Circuit Power and (b) Leakage Power [123].	17
1.18	Methodologies to make SRAM non-volatile: (a) using pull-down NMOS transistor asymmetry by hot-electron injection [174], (b) using modified gate material to store charge when power-down (SONOS) [212].	18
1.19	(a) Battery backup block diagram (b) 512K battery backup SRAM Module for all I-8000 Embedded Controllers, extension board, PLC (available online @ http://www.a2s.pl/en/s512-p-5707.html).	19
1.20	Two-macro Scheme. Schematics of FPGAs. (a) SRAM-based FPGA (b) Conventional nonvolatile FPGA with embedded flash and SRAM-based configuration memory. The flash memory and logic transistors are fabricated in separate areas (c) Conventional nonvolatile FPGA. All transistors have floating-gate structure. (d) Nonvolatile flash-based FPGA reported in [232]. High-speed logic circuit and configuration flash memory with MONOS gate-stack are finely integrated. Power cut switch in each block provides low-power operation by power gating.	20
1.21	Emerging Non-volatile Memory Devices (a) Flash Memories and its storage mechanism [22] (b) Magnetic storage based memories (Magnetic tape (Source: Google) (top-left), MRAM chips by Everspin (Source: Everspin) (top-right), MTJ and STT-MRAM cells [7] (bottom) (c) PCM fabricated by IBM [47, 157], crossbar structure of OxRAM [125], filament formation in OxRAM [6] (bottom).	22

1.22	(a) Cost/bit for Flash and emerging technologies. After 10 nm when scaling issues will prevent further reduction in size of Flash memories, the cost/bit for the said technology will saturate unlike emerging technologies where with scaling, the cost/bit will reduce (Source: Electronic Design) (b) Write current (c) Write access time (d) Maximum capacity achieved (commercial) for PCM, STT-MTJ and OxRAM (here mentioned as RRAM) [29].	24
2.1	(a) Metal-insulator-metal (MIM) structure of OxRAM devices. RESET and SET state due to dissolution and formation of conductive filament (CF) (b) Illustration of V-OxRAM arrays for realizing high-bit-density memories [77] (c) Cross-sectional TEM image of the 3D double-layer V-OxRAM, showing a steep sidewall profile. (d) Enlarged picture of the Ta/TaO _x /TiO ₂ /Ti MIM unit cell as indicated in (c) [77].	28
2.2	IV characteristics showing (a) Unipolar and (b) Bipolar switching [62]. . .	29
2.3	Classification of OxRAM devices based on the underlying switching mechanism.	30
2.4	Schematic of the forming process (a) Pristine device, (b) vacancy generation, drift/diffusion processes under an external electric field, (c) vacancy drift/diffusion processes result in a non-uniform distribution of vacancy concentration. TE and BE represent top electrode and bottom electrode, respectively.	31
2.5	Stack structure of non-filamentary OxRAM device (a) The device is generally an MIM or an MIS type of a structure. (b) band-bending and tunneling leads to conduction of current in SET and RESET state [201].	32
2.6	(a) The resistive switching results from the oxygen diffusion and modulations of the local electronic interface states within the Nb _x O _y layer, which affects the interface properties of the Au (Schottky) contact and of the Al ₂ O ₃ tunneling barrier (b) I-V characteristics of the LRS and HRS branch of the double barrier device in the reverse voltage regime of the Schottky contact (device area is normalized to 1 μm ²) (c) Comparison between the Schottky contact resistance at the LRS and HRS branch and the tunnelling resistance. Inset: Shift of the diode forward current onset [70].	33
2.7	In situ TEM resistive switching of a TiN/PCMO/Pt junction device to the HRS (a) A series of TEM snapshots captured at V _{RESET} during sequential positive bias sweeps (0 → +V _{RESET} → 0) by applying V _{RESET} from 1 V to 5 V in 1 V increments. Changes in the thickness of the a-TiO _x N _y reaction layer are indicated by red arrows. (b) Movement of the two reaction fronts of the a-TiO _x N _y layer, i.e., the a-TiO _x N _y /TiN (upper) and the PCMO/a-TiO _x N _y (lower) interfaces, traced with the increase in V _{RESET} . The a-TiO _x N _y /TiN interface moves faster than the PCMO/a-TiO _x N _y interface indicating that the drift of not only oxygen but also Ti ions contribute to the growth process with stronger influence of the oxygen ions [12].	33

2.8	The two general energy band configurations of SCLC mechanism. (a) M/I1/I2/M, where the two M layers are made of a commonly low-work-function metal while the I layer is actually a double-layered structure with an I1 layer as the low E_g material and an I2 layer as the high E_g material. (b) M1/I/M2, where the two M layers had different work functions (M1 had a low work function and M2 had a high work function) while the I could have been either a single or double layer. Middle and right panels correspond to set and reset energy band diagrams, respectively. (c) BRS I–V curves of Al/TiO _x /Al. (d)-(g) cross-section low magnification of the entire MIM structure, and HRTEM images across the TiO _x structure near the TE and BE interfaces, respectively. [168].	34
2.9	(a),(b) the multilevel state non-filamentary type OxRAM [206] and (c), (d) the binary state filamentary type OxRAM [227] operate at pulse schemes.	34
2.10	(a) Keithley 4200A semiconductor characterization and DC probe station (b) Keithley 4225 PMU card for pulse characteristics measurements (c) Everbeing C-6 12" vacuum chuck analytical probe station	35
2.11	Illustration of DUT probed by the Everbeing probe station connected to the Keithley 4200A SCS	36
2.12	Fabrication process flow for 9nm thick HfO _x device. The TE and BE is of platinum and the device dimension is 100 μ m $\times$ 100 μ m.	37
2.13	(a) I-V characteristics showing forming, SET and RESET for Ni/HfO _x /TiN (100 μ m $\times$ 100 μ m device) (b) 500 SET/RESET sweeps showing cycle-to-cycle (C2C) for the Ni/HfO _x /TiN device (c) Cumulative distributive (CDF) plot for resistive states achieved by the device.	38
2.14	Illustration of formation of parasitic filaments due to migration of Ni ⁺ ions in the switching layer (HfO _x) leading to parasitic SET states in the RESET regime.	38
2.15	(a) Parasitic SET during application of RESET signal to the device (b) Illustration of Ni ion migration causing parasitic conductive filament paths which leads to SET during RESET. (c) Read-out resistances showing parasitic SET during RESET state read.	39
2.16	Illustration of formation of conductive filaments due to migration of O ²⁻ ions in the switching (HfO _x) and blocking (Al ₂ O ₃) layer leading to device being programmed to SET state.	40
2.17	Illustration of filament formation prevention due to migration of Ni ⁺ ions in the switching (HfO _x) by blocking (Al ₂ O ₃) layer leading to prevention of parasitic SET states during RESET programming.	40
2.18	Illustration of filament formation due to migration of Ni ⁺ ions in the switching (HfO _x) and blocking (Al ₂ O ₃) layer due to abundant source at TE leading to parasitic SET states during RESET programming.	41

2.19	(a) Reduced parasitic SET in RESET regime when Al_2O_3 blocking layer is added between HfO_x and TiN (BE) interface (b) Comparison of the SET and the RESET resistance spread with and without blocking layer in the OxRAM stack, respectively.	41
2.20	I-V characteristics of (a)-(f) some of the published works for filamentary OxRAM devices (g) and (h) OxRAM devices studied in this thesis.	43
2.21	(a) Illustration of device fabrication flow (b) TEM image of Ni/ HfO_x / TiO_2 /TiN with 3nm HfO_x and 7nm ATO.	45
2.22	(a) I-V characteristics for $100\mu\text{m} \times 100\mu\text{m}$ Ni/ HfO_x / TiO_2 /TiN device (b) 100 SET and 100 RESET pulses applied to the Ni/ HfO_x / TiO_2 /TiN device. SET pulse applied is +3 V, 0.01 ms and RESET pulse applied is -3 V, 70ms. Read pulse is of -1.5 V, 100 μs	46
2.23	(a) Energy band diagram on applying a negative voltage (RESET), (b) and a positive voltage (SET) at the top electrode of the OxRAM device. The bottom electrode is grounded in both the cases.	47
2.24	(a) Schematic diagrams showing O^{2-} migration in the V_O -rich (oxygen-deficient) layer near the top Ta electrode during bipolar SET and RESET operations. (b) Calculated band diagrams of the HRS and LRS in a Ta/ TaO_x (20 nm)/ TiO_2 (60 nm)/Ti MIIM in ± 2 V read operations [77]. The stack is similar to the stack studied in this work.	48
2.25	(a) Read current for SET state (LRS) when applying positive read voltage of magnitudes in range $0.2 \text{ V} \leq V_{\text{read}} \leq 2 \text{ V}$ to the OxRAM (b) Low resistance-state (LRS) as read by the read voltages. The color-map is same as that of the read currents in (a) (c) Read currents (zoomed) for $0.2 \text{ V} \leq V_{\text{read}} \leq 1.2 \text{ V}$ showing current drift due to forward bias Schottky effect (d) Spread of read current on SET state when positive read is applied.	49
2.26	(a) Read current for SET state (LRS) when applying negative read voltage of magnitudes in range $-0.2 \text{ V} \geq V_{\text{read}} \geq -2 \text{ V}$ to the OxRAM for a read time of 250 ms (b) Low resistance-state (LRS) as read by the read voltages. The color-map is same as that of the read currents in (a) (c) Read currents (zoomed) for $-0.2 \text{ V} \geq V_{\text{read}} \geq -1 \text{ V}$ (d) Spread of read current on SET state when negative read is applied.	50
2.27	(a) Read current for RESET state (HRS) when applying positive read voltage of magnitudes in range $0.2 \text{ V} \leq V_{\text{read}} \leq 2 \text{ V}$ to the OxRAM device (b) High resistance-state (HRS) as read by the read voltages. The color-map is same as that of the read currents in (a) (c) Read currents (zoomed) for $0.2 \text{ V} \leq V_{\text{read}} \leq 1.2 \text{ V}$ (d) Spread of read current on RESET state when positive read is applied.	51

2.28	(a) Read current for RESET state (HRS) when applying negative read voltage of magnitudes in range $-0.2 \text{ V} \geq V_{read} \geq -2 \text{ V}$ to the OxRAM device (b) High resistance-state (HRS) as read by the read voltages. The color-map is same as that of the read currents in (a) (c) Read currents (zoomed) for $-0.2 \text{ V} \geq V_{read} \geq -1 \text{ V}$ (d) Spread of read current on RESET state when negative read is applied.	52
2.29	(a) Resistance window for the resistance states read by positive read bias (b) Resistance window for the resistance states read by negative read bias for SET and RESET states. The x-axis in the figure (b) is in absolute scale (c) Comparative chart showing the resistance-states read by the read bias voltage applied.	53
2.30	I-V characteristics of (a)-(g) some of the published works for non-filamentary OxRAM devices (h) OxRAM devices studied in this thesis. (e) DC Reset characteristics of a-VMCO devices in Regular regime conditions (Positive: 5.5 V). After regime inversion with strong negative bias of -4.0 V, (f) Set is observed in the positive (inverted) polarity but (g) further positive bias sweep can restore the device back to regular regime [181].	55
3.1	Schematic of modeling conductive filament (CF) evolution processes during SET and RESET operations on OxRAM cell. Key physical variables are gap distance (g) and CF radius (w/2).	58
3.2	Emulated I-V characteristics from proposed modified Stanford Model (a) for 10 DC sweeps. Note that model provided in [118] could only switch for one DC sweep unlike modified model which shows switching in all the applied DC sweeps (b) I-V characteristics for modified model for 10 SET/RESET cycles (c), (d) for 10 SET and RESET cycles, respectively. Note that for repeated SET/RESET sweeps as in (c) and (d) it is essential to RESET/SET the device after each sweep in simulation as well.	61
3.3	Illustration of equivalent RC model of a bi-layer OxRAM device	65
3.4	C-V measurements of the single layer MIM structures at 50 kHz which yield κ -values of (a) 18.7 for a Ta/(4.8 nm) HfO ₂ /TiN and (b) 22.9 for a Pt/(9.5 nm) Al:TiO ₂ /TiN.	67
3.5	DC I-V characteristics of (a) Ta/HfO ₂ /Al:TiO ₂ /TiN [25]; (b) TiN/TaO/HfO _x /TiON/TiN [124]; (c) Al/AlO _σ /Ta ₂ O _{5-x} /TaO _y /W [120].	70
3.6	AC characteristics and internal state variable evolution: (a), (b) when 50 consecutive SET and RESET pulses (SET +3 V, 0.1 ms; RESET -3 V, 70 ms) are applied to Ta/HfO ₂ /Al:TiO ₂ /TiN [25]. (c), (d) when consecutive SET and RESET pulses (SET +7 V, 100 μs; RESET -7 V, 100 μs) are applied to the device Al/AlO _σ /Ta ₂ O _{5-x} /TaO _y /W [120].	71

3.7	Modeling of the analog switching behavior of the studied devices. First, measured and modeled DC I-V characteristics for Ta/HfO ₂ /Al:TiO ₂ /TiN device [25] showing good agreement are shown for different RESET (a) and SET (b). For clarity, the red and blue curves are up-shifted by one and two orders of magnitude, respectively. Next, (c) and (d) show modeled DC I-V for devices TiN/TaO/HfO _x /TiON/TiN [124] and Al/AlO _σ /Ta ₂ O _{5-x} /TaO _y /W [120], respectively. Finally, AC characteristics under varying voltages and varying pulse widths for (e), (f) device [25] and (g), (h) device [120].	72
3.8	(a) Change in the device current and in the internal state variable 's' when arbitrary sequence of pulses (S-S-S-R-R-S-S-R) are applied to the Ta/HfO ₂ /Al:TiO ₂ /TiN device [25] (SET +3 V, 0.1 ms; RESET -3 V, 70 ms; Read -1.5 V, 100 μs). (b) The effects of varying the rate of internal state variable evolution (ds(t)/dt) and also the extreme case when capacitors are not considered in the model on the change in device current.	73
3.9	(a) DC I-V variability reproduction by the proposed model for Al/AlO _σ /Ta ₂ O _{5-x} /TaO _y /W [120] (SET +3.5 V; RESET -3.0 V) (b) ds(t)/dt evolution at each voltage iteration for 10 SET/RESET sweeps as calculated in SPICE tool.	74
4.1	Circuit schematics of different NVSRAM bit-cells proposed in literature: (a) 9T-2R: WLL and WLR are separate WLs to control 1T-1R cells, (b) 8T-2R: SWL indicates NVM switch line, (c) 8T-1R, (d) 7T-2R, (e) 7T-1R, and (f) 6T-2R (redrawn from [216, 39, 191, 172, 208, 204]). Variable resistance here indicates the NVM element.	76
4.2	(a) Circuit schematic of 4T2R NV-SRAM bit-cell (redrawn from [130]), (b) DC IV characteristics of 3 nm thick HfO _x based OxRAM device used in this study (modelled in [118]).	77
4.3	Write operation being performed on the 4T2R NVSRAM cell. (a) The cell first loads the data to bit-lines (b) the access transistors turned on by WL (c) feedback action facilitating data write in internal node (d), (e) Ox1 and Ox2 getting programmed at PL transitions (f) Data read out from the bit-cell via Ox1 and Ox2.	78
4.4	Set and reset voltages as a function of pulse width. The required pulse width to successfully program the device exponentially increases with decreasing pulse amplitudes [211]. The experiment is repeated for multiple cycles over multiple devices. The dotted black line represents the approximate prediction line.	80
4.5	Operational modes for Read and Write for two-cycle programming based 4T-2R NVSRAM bit-cell. The initial SET state is at 3.3 kΩ indicates the first SET state after forming. The subsequent SET states will not be 3.3 kΩ but ~500 kΩ. V _{read} = 1.6 V with t _{read} = 200 ns in simulations (for better resolution of resistance).	81
4.6	Conductive filament evolution on applying (a) Strong SET voltage (in this case V = 1.6 V) and (b) Weak SET voltage (in this case V = 1.2 V). . . .	83

4.7	During Write '1' operation: Switching in (a) Ox1 and (b) Ox2 devices for LRS-HRS and HRS1-HRS2 programming schemes [130].	83
4.8	(a) Static noise margin (SNM) curve for LRS-HRS and HRS1-HRS2 scheme (b) Single bit-cell layout for 4T2R NVSRAM. The transistors used here are from UMC 90nm library.	84
4.9	(a) Write latency, bandwidth (throughput), dynamic energy and total leakage for both the schemes (normalized) (b) Read latency, bandwidth, dynamic energy and area of implementation for both the schemes (normalized). . . .	85
4.10	Write operation being performed on the 4T2R NVSRAM cell. (a) The cell first loads the data to bit-lines (b) the access transistors turned on by WL (c) feedback action facilitating data write in internal node (d) Ox1 and Ox2 getting programmed at PL transitions (e) Data read out from the bit-cell via Ox1 and Ox2.	87
4.11	Operational modes for Read and Write (a) two-cycle programming based 4T-2R NVSRAM bit-cell and (b) proposed single-cycle/parallel programming based 4T-2R NVSRAM bit-cell using pulse engineered signals at PL and BL.	88
4.12	(a) Applied PL and BL signals during write logic '1' operation (b) Ox1 switching during RESET and SET regions. Final Ox1 state is SET signifying '1' is written at node Q. The inset shows the switching of virgin Ox1 device (initialized to SET by pre-processing or forming). The initial RESET condition switches the Ox1 in RESET and then to SET state according to potential developed across it.	89
4.13	(a) Applied PL and BLB signals during write logic '1' operation (b) Ox2 switching during RESET region	90
4.14	Effect on V_{TB} required for switching, due to change in peak amplitude of BL (1–1.3 V) keeping peak amplitude of PL = 1.6 V for (a) Ox1 and (b) Ox2. Effect of change in peak amplitude of BL on (c) switching time, and (d) Resistance of OxRAM devices.	92
4.15	Effect on V_{TB} required for switching, due to change in the peak amplitude of PL (1.5–1.8 V) keeping peak amplitude of BL = 1V for (a) Ox1 and (b) Ox2. Effect of change in peak amplitude of PL on (c) switching time, and (d) Resistance of OxRAM devices.	95
4.16	Change in V_{TB} at switching instant, for (a) Ox1 and (b) Ox2 with change in the duration of rising edge of PL voltage pulse.	96
4.17	Change in the (a) switching time and (b) resistance of OxRAM devices (after successful write operation) by modulating the duration of rising edge of the pulse applied at PL, keeping peak amplitude of BL signal at 1V.	96
4.18	Layout of 4T-2R NVSRAM bit-cell implemented at 130nm technology node.	97
5.1	Top) Schematic showing the noise voltage sources V_n for measuring bit-cell SNM [66]. (Bottom left) Butterfly curve for SNM calculations [166]. (Bottom right) N-curve for calculating cell SVN, SINM, WTI and WTV.	102

5.2	Simulated- (a) hold, (b) read, and (c) write- SNM comparison. (d) N-curve comparison. Optimized 6T SRAM at 90nm node and proposed OxRAM based 4T-2R NVSRAM bit-cells were simulated.	103
5.3	Simulated 4T-2R NVSRAM bit-cell- (a-b) Hold SNM, (c-d) Read SNM, and (e-f) Write SNM, for different V_{DD} values (a,c,e) and different pull-down transistor widths (b,d,f). For transistor widths lower than 400nm read is destructive.	104
5.4	Dependence of N-curve metrics on CR by modulating- (a) pull down transistor width, and (b) supply voltage V_{DD} , of the 4T-2R NVSRAM bit-cell.	106
5.5	(a) LRS/HRS resistance spreads considering cycle-to-cycle and device-to-device OxRAM variability. For each case (C2C and D2D), 1000 simulating instances were considered. Impact of variability on 4T-2R bit-cell (b) read SNM, and (c) write SNM.	108
5.6	(a) Simulated N-curves for 4T-2R NVSRAM with OxRAM resistance state variability (both in the HRS and the LRS states). (b) Effect on SINM due to variability in OxRAM device resistance states (c) Effect on SVNIM due to variability in OxRAM device resistance states (d) Effect on SINM due to resistance state variability only in HRS states; LRS is fixed at 550 k Ω (e) Effect on SINM due to resistance state variability only in LRS states; LRS is fixed at 3.3 M Ω (f) Effect on SVNIM due to resistance state variability only in LRS states; LRS is fixed at 3.3 M Ω	110
6.1	Different NV-FF schematics proposed in literature (a) OxRAM based NV-FF [145] (b) STT-MTJ based NV-FF [219] (c) SHE-MTJ based NV-FF [109] (d) Ferroelectric capacitors based NV-FF [200]. The figures have been redrawn from the referenced papers.	113
6.2	Schematic of the real-time NV-FF. It is similar to the conventional CMOS based FF in terms of modules constituting it – Master Block and Slave Block	116
6.3	Timing diagram of the 4T-2R based NV-FF. When CLK = 0, the OxRAM in master block gets programmed and when CLK = 1, OxRAM in slave block gets programmed. R1 (feed-forward) and R2 (feedback) are master block OxRAM, R3 (feed-forward) and R4 (feedback) are slave block OxRAM. The value at y-axis for R1-R4 is in M Ω . All the OxRAM devices are initialized to a HRS state before the write operation is performed (only valid for first cycle).	119
6.4	Schematic of the proposed modified NV-FF depicting the 3 major operating blocks	120
6.5	The off-loading block showing the three sub-blocks. The data is off-loaded during controlled power-down in a single OxRAM device. The control clock is a simple OR gate controlled by two control signals STR and RSTR. The data generation block is used to program the device during data off-loading and providing supply during restore operation	121

6.6	Store operation in the proposed modified NV-FF. Green data shows the polarities and data values at off-loading block circuit nodes when $Q = 0$ is to be stored in OxRAM. Blue data shows the polarities and the values at off-loading block circuit nodes when $Q = 1$ is to be stored. The red data shows the control block signals	123
6.7	Restore operation in the proposed modified NV-FF. Here V_{RD} provides the read voltage that is needed to read the state stored in the OxRAM. The I_{read} current obtained from the OxRAM charges the load capacitance at the output to a logic value '1' or '0' depending on the state of the OxRAM (LRS or HRS)	124
6.8	Timing diagram showing different operating modes of the modified NV-FF. The off-loading is controlled by the control signals STR and RSTR	124
7.1	(a) Basic structure of STT-MRAM (b) Parallel (P) and Anti-parallel (AP) states in MTJ that determines LRS and HRS; Normalized resistance v/s applied voltage for STT-MRAM [167].	129
7.2	(a) Basic structure of PCM devices showing the programmable area which is crystallized or amorphosized based on the signal that is applied to it, determining the state of the device (b) SET/RESET and Read signals applied to the PCM device determine the temperature which leads to crystallization and amorphization of the GST. (c) Intel's Optane processor.	130
7.3	IoT SoC Architectures : (a) Conventional IoT SoC (b) Proposed IoT SoC (unified memory design).	132
7.4	(a) Illustration of the experimental setup used for this work (b) TI MSP430 available commercially (mage source: Geletu, Biruk Silase. "Modeling the Behavior of an Electronically Switchable Directional Antenna for Wireless Sensor Networks." (2011).	133
7.5	SPsim simulating Contiki's Blinker application on an ESB.	134
7.6	MSPsim simulation with an MSP430 microcontroller and connected peripherals (redrawn from [58]).	135
7.7	Screenshot of an Ubuntu system showing Contiki 2.6 running on 41 nodes forming an IPv6-RPL-6LoWPAN network in the Cooja Contiki network simulator (Source: Wikipedia).	136
7.8	Memory array organization modeled in NVSim: a hierarchical memory organization includes banks, mats, and subarrays with decoders, multiplexers, sense amplifiers, and output drivers [54].	137
7.9	Functional block diagram of TI MSP430F1611 [85]	138
7.10	Memory breakdown based on type of memory for MSP430F1611.	139
7.11	Memory write hit profile for IoT application Sky-collect. It can be observed that the writes are concentrated in localized RAM address rather than being uniformly distributed. Thus, the write profile is fairly sporadic in nature.	140

7.12	Variation of (a) maximum write hits and (b) total max writes/cycle with time for Sky-collect application over the entire RAM.	141
7.13	(a) Dynamic Energy for Read and Write Operations with SRAM and different NVM based NVSRAM. While the dynamic read energy for all NVM based NVSRAM is comparable to that of SRAM, the write dynamic energy is quite high for PCM based NVSRAM, while STT-MRAM and OxRAM based NVSRAM shows comparable values to SRAM (b) Leakage power and total power consumption of the system for IoT WSN application for SRAM and different NVM based NVSRAM. The blue dots in the plot shows the % contribution of the leakage power in the total power of the system.	143
7.14	(a) Latency and Delay estimates for the MSP430 processor for SRAM based RAM and different NVM devices based NVSRAM. The processor is operating at a frequency of 80 MHz (b) Energy-Delay Product (EDP) for SRAM and different NVM based RAM.	144
8.1	(a) Illustration of HfO ₂ based OxRAM device with stack TiN/Ti/HfO ₂ /TiN as fabricated during MAD-II. (d) Resistance state distribution of the fabricated device.	150
8.2	(a) Illustration of the layout of the 4T-1R NVSRAM cell fabricated (b) Micrograph of the final die from the foundry (c) 4×4 NVSRAM array implemented in 130nm technology.	151

List of Tables

1.1	Effect on various memory/core parameters with and without power-gating [89]	17
1.2	Operational specifications of different memory technologies [189, 194, 182, 82, 55]	23
1.3	Operational specifications of different emerging memory technologies [189]	23
2.1	Comparison of some of the published works for filamentary OxRAM devices and filamentary OxRAM devices studied in the thesis (For I-V characteristics see Fig. 2.20).	44
2.2	Resistance window for read bias applied to read SET and RESET states for the OxRAM device	50
2.3	Comparison of some of the published works for non-filamentary OxRAM devices and non-filamentary OxRAM devices studied in the thesis (For I-V characteristics see Fig. 2.30).	54
3.1	Benchmarking different compact models proposed in literature	64
3.2	Parameter values obtained from model	70
4.1	Comparison of 4T2R NVSRAM bit-cell parameters for different programming schemes (LRS-HRS and HRS1-HRS2) during write ‘1’ operation. Read pulse width used to read the cell is 200 ns in both the schemes	84
4.2	Comparison of Write logic-‘1’ and ‘0’ operations.	90
4.3	Absolute programming time for programming the OxRAM Devices used in 4T-2R NVSRAM bit-cell.	94
4.4	Comparison of Write logic-‘1’ and ‘0’ operations.	94
4.5	Dependence of V_{TB} , OxRAM switching time, and bit-cell program energy (E), on PL rise time modulation (200–800 ns).	97
4.6	Comparison of different 4T-2R NV-SRAM bit-cells and state-of-the art 6T SRAM bit-cell [129].	99
5.1	SNM Comparison of Conventional 6T-SRAM and 4T-2R NVSRAM bit-cell	105
5.2	N-curve metric comparison of 6T-SRAM and 4T-2R NVSRAM bit-cell . .	106

5.3	N-curve metric for different pull-down transistor width and supply voltage (V_{DD}) for 4T-2R NVSRAM bit-cell	107
6.1	Operations performed by the control block during off-loading of data to the non-volatile block	122
6.2	Comparison of various NV-FF designs proposed in literature and the proposed NV-FF designs	126
7.1	Benchmarking emerging resistive NVM and SRAM [226]	128
7.2	Memory organization of MSP430F1611 [85]	137
7.3	Memory Footprint of typical Contiki IoT WSN applications	139
7.4	RAM usage statistics for Sky-Collect application (12s emulated time) . . .	140
7.5	Memory Write Statistics for Sky-Collect Application	141
7.6	Performance Benchmarking of emerging NVM and SRAM for a simulated application using NVSIM.	146