Design and Analysis of Drain-extended MOS (DeMOS) for Improved Switching Performance and Electrothermal Switching Reliability

SHRADDHA PALI

CENTRE FOR APPLIED RESEARCH IN ELECTRONICS
INDIAN INSTITUTE OF TECHNOLOGY DELHI
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Design and Analysis of Drain-extended MOS (DeMOS) for Improved Switching Performance and Electrothermal Switching Reliability

by

SHRADDHA PALI

Centre for Applied Research in Electronics

Submitted

in fulfilment of the requirements for the degree of Doctor of Philosophy
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Dedicated to

My Family

CERTIFICATE

This is to certify that thesis entitled, **"Design and Analysis of Drain-extended MOS (DeMOS) for Improved Switching Performance and Electrothermal Switching Reliability",** being submitted by **Shraddha Pali** to the Centre for Applied Research in Electronics (CARE), Indian Institute of Technology Delhi, for the award of the degree of Doctor of Philosophy, is a record of bonafide research work carried out by her. She has worked under my guidance and supervision and has fulfilled the requirments for the submission of this thesis, which to my knowledge, has reached the requisite standard.

The research reports and results presented in this thesis have not been submitted, in part or full, to any other university or institute for the award of any degree or diploma.

Dr. Ankur Gupta
Associate Professor
Centre for Applied Research in Electronics (CARE)
Indian Institute of Technology Delhi
New Delhi-110016,
India

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Abstract

Power MOSFETs are devices that can support high drain voltage and finds application in interface circuit design between different voltage modules of a system. The drain-extended NMOS (DeNMOS) is a low-voltage power MOSFET compatible with CMOS process technology and is used as a switching device in electronic control units. For efficient performance at high-frequency switching applications, the gate charge of DeNMOS should be minimized to increase switching speed and reduce switching losses. Hence, DeNMOS is optimized for high-switching applications by incorporating solutions that reduce gate charges. Moreover, power device switching at very high current conditions in the presence of unclamped inductive loads (UIL) is a critical concern when device turn-off increases the lattice heating followed by secondary high current events like space charge modulation, regenerative feedback, and finally, catastrophic thermal runaway. UIL switching from on-to-off state triggers the parasitic bipolar to discharge the off-state drain current through the body diode. However, the presence of off-state avalanche generation and subsequent self-heating effects can prevent the safe turn-off of the device if secondary high current effects become dominant. This work presents various DeNMOS design solutions to optimize the device's gate charge performance and electrothermal switching reliability without compromising the DC safe operating area and avalanche reliability.

The first phase of work extensively examined the role of various drift region layout RESURF solutions in optimizing the switching performance and electrothermal switching reliability of DeNMOS. Layout RESURF techniques have been used before to optimize the on-resistance and breakdown voltage trade-off; however, the impact of RESURF on gate charge performance and electrothermal switching reliability under unclamped inductive load conditions has not been explored. Therefore, a comprehensive and comparative investigation of drift region engineering using RESURF solutions has been presented to optimize the switching speed, loss, reverse recovery, and gate charge performance. Moreover, the dependence of electrothermal switching reliability on drift region engineering using RESURF techniques with doping optimization has been presented for the first time in this work.

The second phase of work deals with RESURF techniques based on high-k dielectric field plate-based techniques. The high-k dielectric is an efficient RESURF solution that can optimize the on-resistance and breakdown voltage but limits the switching performance of the device due to large surface charge accumulation. The Planar and Trench structure of DeNMOS using a high-k field plate has been

proposed to limit the surface charge accumulation without compromising the RESURF action. As a result, proposed high-k DeNMOS have improved gate charge and reverse recovery performance and high electrothermal switching reliability under UIS conditions.

Finally, in the last phase of work, techniques using body region engineering are presented to enhance unclamped inductive load switching reliability without compromising the mixed signal performance of the device. Avalanche ruggedness and robustness are the key factors that should be optimized to improve UIS reliability. Past research used body region engineering solutions like doping or source contact optimization to reduce the base resistance of parasitic bipolar to suppress the rate of carrier injection from the source and improve the avalanche ruggedness of the device. The proposed body contact and body region engineering solutions presented in this work achieve high avalanche ruggedness and enhanced robustness by improving the thermal stability of the device without compromising the mixed signal performance of the device.

सार

पावर MOSFET ऐसे उपकरण हैं जो उच्च ड्रेन वोल्टेज का समर्थन कर सकते हैं और सिस्टम के विभिन्न वोल्टेज मॉड्यूल के बीच इन-टेरफेस सर्किट डिजाइन में उपयोग पाते हैं। ड्रेन-एक्सटेंडेड NMOS (DeNMOS) एक कम वोल्टेज पावर MOSFET है जो CMOS प्रक्रिया प्रौद्योगिकी के साथ संगत है और इसका उपयोग इलेक्ट्रॉनिक नियंत्रण इकाइयों में स्विचिंग डिवाइस के रूप में किया जाता है। उच्च-आवृत्ति स्विचिंग अनुप्रयोगों में कुशल प्रदर्शन के लिए, स्विचिंग गति बढ़ाने और स्विचिंग नुकसान को कम करने के लिए DeNMOS के गेट चार्ज को कम किया जाना चाहिए। इसलिए, गेट चार्ज को कम करने वाले समाधानों को शामिल करके DeNMOS को उच्च-स्विचिंग अनुप्रयोगों के लिए अनुकूलित किया गया है। इसके अलावा, अनक्लैम्प्ड इंडक्टिव लोड (UIL) की उपस्थिति में बहुत अधिक ड्रेन करंट की स्थिति में पावर डिवाइस स्विचिंग एक गंभीर चिंता का विषय है, जब डिवाइस बंद होने से हीटिंग बढ़ जाती है, जिसके बाद स्पेस चार्ज मॉड्यूलेशन, पुनर्योजी प्रतिक्रिया और अंत में, विनाशकारी थर्मल रनवे जैसी उच्च करंट घटनाएं होती हैं। UIL का स्विचिंग ऑन-टू-ऑफ स्थिति से बॉडी डायोड के माध्यम से ऑफ-स्टेट ड्रेन करंट को डिस्चार्ज करने के लिए पैरासिटिक BJT को चालू करता है। हालाँकि, ऑफ-स्टेट एवा-लांच की उपस्थिति और बाद में स्व-हीटिंग प्रभाव डिवाइस के सुरक्षित टर्न-ऑफ को रोक सकते हैं यदि उच्च करंट प्रभाव प्रभावी हो जाते हैं। यह कार्य डीसी सुरक्षित ऑपरेटिंग क्षेत्र और एवा-लांच विश्वसनीयता से समझौता किए बिना डिवाइस के गेट चार्ज प्रदर्शन और इलेक्ट्रोथर्मल स्विचिंग विश्वसनीयता को अनुकूलित करने के लिए विभिन्न DeNMOS डिज़ाइन समाधान प्रस्तुत करता है।

कार्य के पहले चरण में DeN-MOS के स्विचिंग प्रदर्शन और इलेक्ट्रोथर्मल स्विचिंग विश्वसनीयता को अनुकूलित करने में विभिन्न ड्रिफ्ट क्षेत्र लेआउट RESURF समाधानों की भूमिका की व्यापक जांच की गई। ऑन-रेजिस्टेंस और ब्रेक-डाउन वोल्टेज ट्रेड-ऑफ को अनुकूलित करने के लिए लेआउट RESURF तकनीकों का उपयोग पहले भी किया जा चुका है; हालाँकि, गेट चार्ज प्रदर्शन और अनक्लैम्प्ड इंडक्टिव लोड स्थितियों के तहत इलेक्ट्रो-थर्मल स्विचिंग विश्वसनीयता पर RESURF के प्रभाव का पता नहीं लगाया गया है। इसलिए, स्विचिंग

गति, हानि, रिवर्स रिकवरी और गेट चार्ज प्रदर्शन को अनुकूलित करने के लिए RESURF समाधानों का उपयोग करके ड्रिफ्ट क्षेत्र इंजीनियरिंग की एक व्यापक और तुलनात्मक जांच प्रस्तुत की गई है। इसके अलावा, डोपिंग अनुकूलन के साथ RESURF तकनीकों का उपयोग करके ड्रिफ्ट क्षेत्र इंजीनियरिंग पर इलेक्ट्रोथर्मल स्विचिंग विश्वसनीयता की निर्भरता को इस काम में पहली बार प्रस्तुत किया गया है।

कार्य का दूसरा चरण हाई-के डाइइलेक्ट्रिक पर आधारित RESURF तकनीकों से संबंधित है। हाई-के डाइइलेक्ट्रिक एक कुशल RESURF समाधान है जो ऑन-रेजिस्टेंस और ब्रेकडाउन वोल्टेज को अनुकूलित कर सकता है लेकिन बड़े सतह चार्ज संचय के कारण डिवाइस के स्विचिंग प्रदर्शन को सीमित कर देता है। हाई-के फ़ील्ड प्लेट का उपयोग करके DeNMOS की प्लेनर और ट्रेंच संरचना बनाई गई है। RESURF कार्रवाई से समझौता किए बिना सतह चार्ज संचय को सीमित करने का प्रस्ताव प्रस्तुत किया गया है। परिणामस्वरूप, प्रस्तावित हाई-के DeNMOS ने UIS शर्तों के तहत गेट चार्ज और रिवर्स रिकवरी प्रदर्शन और उच्च इलेक्ट्रोथर्मल स्विचिंग विश्वसनीयता में सुधार किया है।

काम के अंतिम चरण में, डिवाइस के मिश्रित सिग्नल प्रदर्शन से समझौता किए बिना अनक्लैम्प्ड इंडक्टिव लोड स्विचिंग विश्वसनीयता को बढ़ाने के लिए बॉडी रीजन इंजीनियरिंग का उपयोग करने वाली तकनीकों को प्रस्तुत किया जाता है। अवालांचे रुग्गदनेस और रोबस्टनेस प्रमुख कारक हैं जिन्हें UIS विश्वसनीयता में सुधार के लिए अनुकूलित किया जाना चाहिए। पिछले शोध में स्रोत से इलेक्ट्रॉन इंजेक्शन की दर को दबाने और डिवाइस की अवालांचे रुग्गदनेस में सुधार करने के लिए पैरासिटिक BJT के प्रभाव को कम करने के लिए डोपिंग या स्रोत संपर्क अनुकूलन जैसे बॉडी क्षेत्र इंजीनियरिंग समाधान का उपयोग किया गया था। इस कार्य में प्रस्तुत प्रस्तावित बॉडी संपर्क और बॉडी क्षेत्र इंजीनियरिंग समाधान डिवाइस के मिश्रित सिग्नल प्रदर्शन से समझौता किए बिना डिवाइस की थर्मल स्थिरता में सुधार करके उच्च एवा-लांच रुग्गदनेस और बढ़ी हुई रोबस्टनेस प्राप्त करते हैं।

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List of Symbols

C_{OX}	Oxide capacitance
C_{gg}	Total gate capacitance
C_{gd}	Gate-to-drain capacitance
C_{dd}	Total drain capacitance
C_{gs}	Gate-to-source capacitance
DeMOS	Drain-extended Metal Oxide Semiconductor
DeNMOS	Drain-extended N-type Metal Oxide Semiconductor
DePMOS	Drain-extended P-type Metal Oxide Semiconductor
G_m	Transconductance
I_{ON}	Drain current in presence of VGS
I_{OFF}	Drain current in absence of VGS
I_{rr}	Reverse recovery current of DeMOS
L_{OV}	Gate-to-drain overlap length
L_{CH}	Inversion channel length
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
Q_g	Total gate charge
Q_{gs}	Gate-to-drain coupling charge
Q_{rr}	Reverse recovery charge
R_{ON}	ON-state resistance of DeMOS
R_{OUT}	Output resistance of DeMOS
STI	Shallow Trench Isolation
T_{rr}	Reverse recovery time

T_{ox}	Gate oxide thickness
UIS	Unclamped Inductive Switching
UIL	Unclamped Inductive Load
V_{DD}	Supply voltage to drain
V_{GS}	Input voltage to gate
V_{th}	Threshold voltage