

**NON-LINEARITY ESTIMATION FOR PHASE
INTERPOLATORS
USED IN BANG-BANG CLOCK AND DATA
RECOVERY CIRCUITS**

ARCHIT JOSHI



DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

JULY 2019

© Indian Institute of Technology Delhi (IITD), New Delhi, 2019

**NON-LINEARITY ESTIMATION FOR PHASE
INTERPOLATORS
USED IN BANG-BANG CLOCK AND DATA
RECOVERY CIRCUITS**

by

Archit Joshi

Department of Electrical Engineering

Submitted

in fulfillment of the requirement of the degree of Doctor of Philosophy

to the



DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

JULY 2019

CERTIFICATE

This is to certify that the thesis entitled "**Non-linearity Estimation for Phase Interpolators Used in Bang-Bang Clock and Data recovery Circuits**" being submitted by **Archit Joshi** to Indian Institute of Technology - Delhi (India), for the award of the **Doctor of Philosophy** in Electrical Engineering is a bona fide research work carried out by him under my guidance and supervision. The research work has reached the requisite standard. I hereby declare that the content of the thesis has not been submitted to any other university for award of any degree or diploma.

Supervisor

Dr. Mukul Sarkar,

Associate Professor,

Department of Electrical Engineering,

IIT. Delhi

ACKNOWLEDGEMENTS

My foremost appreciation must go to my advisor, Dr. Mukul Sarkar. His extensive vision and creative thinking have provided the source of inspiration for me. The academic research experiences have encouraged me for exploring the integrated circuits further. I am especially grateful to the members of committee, Dr. Suri, Dr. Chatterjee and Dr. Panda for their valuable suggestions and help. Through their instructions, I learned how to pursue research. It has been a great pleasure to work in the Electrical Engineering Lab. I would like to acknowledge to all of my colleagues for their suggestions and help.

My sincere appreciation goes to my parents, wife and son who have always given me unconditional love, guidance, and support. Without them, none of these could have been accomplished.

Archit Joshi

ABSTRACT

Phase Interpolators are Digital-to-Phase (time) converters and are widely used for providing the adjustable delay needed for phase locking in Clock and Data Recovery (CDR) circuits with Bang-Bang Phase Detectors (BBPD). The non-linearity of the Phase interpolators injects unwanted jitter into the clocks of the CDR which degrade the performance of the CDR. Hence non-linearity needs to be reduced/corrected.

This research focuses on a technique to estimate the non-linearity of the PI during real circuit operation. When the non-linearity estimates are available, useful insight into the behavior of the PI in run time can be obtained. A mathematical model of the basic estimation technique and the accuracy of estimation is presented. Results of proposed mathematical model and MATLAB model are compared.

The non-linearity estimates are used to correct the non-linearity of the PI in a closed loop manner. In this work, two different methods are used to correct the non-linearity of the PI. The first one focuses on adaptation of the bandwidth of Low pass filter of the PI, using a 'reference non-linearity' approach. A mathematical model for the accuracy of estimation using this reference non-linearity approach and tradeoffs of various design parameters is presented. The circuits are fabricated in 180nm CMOS technology. The second approach uses the trimming of the weights of the Phase interpolator to reduce the non-linearity. This approach minimizes the Differential (DNL) as well as Integral Non-linearity (INL) of the PI. A weight update equation is also presented.

सार

फेज इंटरपोलर डिजिटल-टू-फेज (समय) कन्वर्टर्स हैं और इन्हें बैंग-बैंग फेज डिटेक्टर (बीबीपीडी) के साथ क्लॉक और डेटा रिकवरी (सीडीआर) सर्किट में फेज लॉकिंग के लिए आवश्यक समायोज्य विलंब प्रदान करने के लिए उपयोग किया जाता है। फेज इंटरपोलर्स की गैर-रैखिकता सीडीआर की घड़ियों में अवांछित घबराहट का इंजेक्शन लगाती है जो सीडीआर के प्रदर्शन को नीचा दिखाती है। इसलिए गैर-रैखिकता को कम / दुरुस्त करने की आवश्यकता है। यह शोध वास्तविक सर्किट ऑपरेशन के दौरान पीआई की गैर-रैखिकता का अनुमान लगाने की तकनीक पर केंद्रित है। जब गैर-रैखिकता अनुमान उपलब्ध होते हैं, तो रन समय में पीआई के व्यवहार में उपयोगी अंतर्दृष्टि प्राप्त की जा सकती है। मूल अनुमान तकनीक और अनुमान की सटीकता का एक गणितीय मॉडल प्रस्तुत किया गया है। प्रस्तावित गणितीय मॉडल और MATLAB मॉडल के परिणामों की तुलना की जाती है। गैर-रैखिकता अनुमानों का उपयोग पीआई की गैर-रैखिकता को बंद लूप तरीके से ठीक करने के लिए किया जाता है। इस काम में, पीआई की गैर-रैखिकता को सही करने के लिए दो अलग-अलग तरीकों का उपयोग किया जाता है। पहले एक 'संदर्भ गैर-रैखिकता' दृष्टिकोण का उपयोग करके, पीआई के लो पास फिल्टर की बैंडविड्थ के अनुकूलन पर ध्यान केंद्रित करता है। इस संदर्भ का उपयोग करते हुए अनुमान की सटीकता के लिए एक गणितीय मॉडल गैर-रैखिकता दृष्टिकोण और विभिन्न डिजाइन मापदंडों के ट्रेडऑफ़ प्रस्तुत किया गया है। सर्किट 180nm CMOS तकनीक में गढ़े गए हैं। दूसरा दृष्टिकोण गैर-रैखिकता को कम करने के लिए चरण प्रक्षेपक के भार के ट्रिमिंग का उपयोग करता है। यह दृष्टिकोण विभेदक (DNL) के साथ-साथ PI के इंटीग्रल नॉन-लीनियरिटी (INL) को कम करता है। एक वजन अद्यतन समीकरण भी प्रस्तुत किया गया है।

TABLE OF CONTENTS

CHAPTER 1. Introduction	1
1.1 Bang-Bang Clock and Data Recovery Circuits	1
1.1.1 PI Basics	6
1.1.2 PI Non-linearity	11
1.2 Motivation	12
1.3 Design Goals	15
1.4 Major contribution of this work	15
1.5 Thesis Organization	16
CHAPTER 2. Literature Review	18
2.1 Summary	24
CHAPTER 3. Non-Linearity Estimation	25
3.1 Sensing and Estimating Non-linearity	26
3.2 Mathematical Model for the accuracy of Non-linearity estimation	32
3.3 Simulation Results	40
3.4 Summary	44
CHAPTER 4. LPF Bandwidth Adaptation	45
4.1 PI and reference non-linearity	47
4.1.1 Case $\tau \gg \Delta T$: Introducing the reference nonlinearity	50
4.1.2 Case $\tau \ll \Delta T$: Location of state skipping and loop settling	52
4.2 Adaptation analysis in the presence of noise	53
4.3 Summary	62
CHAPTER 5. Implementation and Results	63
5.1 CDR Architecture	63
5.2 Measurements and Simulation results	69
5.3 Summary	76
CHAPTER 6. PI Weight Trimming	77
6.1 PI weight Trimming	77
6.1.1 Parameter Analysis	81
6.2 CDR Architecture	82
6.3 Simulation results	85
6.4 Summary	89
CHAPTER 7. Conclusion	90
7.1 Comparison with original design goals	92

7.2	A design approach to linear PIs	93
7.3	Future work	96
	List of Publications	97
	REFERENCES	98

LIST OF FIGURES

Figure 1– (a) Blocks of Tx and Rx (b) Phase locking	2
Figure 2– Block diagram of a PI based CDR with BBPD. The phase error ϵ between the clock and data and the quantized error from BBPD output ϵ	5
Figure 3– Weighted vector superposition of two vectors A & B to generate a new vector	6
Figure 4– Clock phase generation from 8 uniformly spaced clock phases	7
Figure 5– A MUX based adjacent phase selection for phase interpolation.	8
Figure 6– An inverter based interpolation stage	9
Figure 7– Incoming data, recovered clock and allowed maximum jitter in the	10
Figure 8– PI with input code k , the Low Pass Filter after MUX selection and weights α & β	11
Figure 9– Dual reference Phase Interpolation for Non-linearity improvement [23].	19
Figure 10– Octagonal Phase Interpolator characteristics [25].	22
Figure 11– CDR with phase averaging interpolator [17]	23
Figure 12– Z- Domain block diagram of a PI based CDR with BBPD	25
Figure 13– An actual PI characteristics compared with an Ideal characteristics	26
Figure 14– A linearized model of the CDR along with an ideal PI and injected PI non-linearity $I(K_n)$.	27
Figure 15– Block diagram of the CDR with the various blocks	28
Figure 16– Linearized model of CDR and PI for K_{PD} estimation	30
Figure 17– A linearized model of the CDR	33
Figure 18– Codes K_n shown as a function of time n. Also shown are the various probabilities $P_{k l}$ and PDFs $f_{K_n K_{n-i}}$ and $\dot{f}_{K_n K_{n-1}}$	36
Figure 19– Input non-linearity $I(k)$, simulated non-linearity $\bar{\epsilon}_I(k)$ and estimated non-linearity $\hat{I}(k)$ for various input conditions.	41

Figure 20– Input, simulation and Math result comparison. Unit of A, σ is UI and F is MHz. $\{I(0) .. I(7)\} = \{3, 6, -6, 3, -6, -3, 3, 0\}$ LSB.	42
Figure 21– Settling of $I(k)$ s during compensation for various cases	42
Figure 22 – (a) PDF of the PI input code K, (b) normalized \hat{K}_{PD} curves	43
Figure 23– A typical PI with weight banks, Low Pass Filer and adjacent phase select MUX.	45
Figure 24– (a) Actual PI non-linearity characteristics compared with Ideal, (b) A typical PI with weight banks 0 and 1 and LPF.	47
Figure 25– Interpolation between $v_0(t)$ and $v_1(t)$ with α varying from 0 to 1 in the steps of 0.1. Here $\alpha_1=0.2$ and $\alpha_2=0.4$.	49
Figure 26– (a) $dt/d\alpha$ with respect to α for $\tau/\Delta T=0.2, 0.4, 2$ & 3. (b) Linear output phase with respect to index k, characteristics with state skipping, ideal reference for characteristics with state skipping.	50
Figure 27. A linearized model of the CDR loop with PI, BBPD and noise sources	54
Figure 28– Linear output phase with respect to index k, characteristics with state skipping, ideal reference for characteristics with state skipping, identical to Figure 26b.	55
Figure 29. PI characteristics for $\tau = 0.5\Delta T$ and $1.5\Delta T$ with 2-state skipping.	56
Figure 30. Non-linearity of the PI for $\tau = 0.5\Delta T$ and $1.5\Delta T$ with 2-state skipping.	56
Figure 31. (a) Simulated standard deviation σ_n of the noise \bar{n}_k as a function of count V for $\sigma(\Delta\phi_D) = 0.025UI$ for 4 trails of the same simulation. Each trial has a different noise waveform (b) Plots of S_I/S_n with respect to M for L=8 and $\sigma_n=0.15, 0.2$ and 0.3 LSB.	61
Figure 32. Phase interpolator with the complete CDR	63
Figure 33. PI input phases, input buffers, phase selection MUX and the low pass filter capacitor bank	64
Figure 34. Phase interpolator core section with thermometric weights and WREF implementation.	65
Figure 35. Simulated non-linearity of PI compared with the Model (4.3) for $\tau = 0.2\Delta T, 0.5\Delta T$ and $1.2\Delta T$.	67
Figure 36. PI Non-linearity settling during bandwidth adaptation starting from $\tau = 0.18\Delta T$.	68

Figure 37. Image of the testchip on left and the chip micrograph on right	69
Figure 38. Non-linearity from Math model, simulated PI non-linearity, estimated non-linearity $\hat{I}(k)$ from circuit simulations and Si-measurements for $\sigma_D \sim 0.03UI$ and $\tau = 1.5\Delta T$.	71
Figure 39. (a) Average PI Non-linearity from simulations and Si-measurements after bandwidth adaptation is complete for different PI clock frequencies and input data jitter σ_D . (b). Si-measured (0.125GHz) and circuit simulated (1GHz) PI characteristics with respect to the PI code k , before and after the LPF bandwidth adaptation.	71
Figure 40. A basic PI model with two weights banks, each having its thermometric weights $W_0 .. W_{N-1}$	78
Figure 41. A basic PI non-linearity characteristics	78
Figure 42. DNL and INL after weight trimming for PI weight trimming bits	81
Figure 43. Trimmed weights of the PI after weight trimming for trimming bits	81
Figure 44. CDR architecture with PI, correlator and compensator.	82
Figure 45. Strong arm samplers for sampling the data	83
Figure 46. PI sector select Mux along with the core interpolator	84
Figure 47. PI weight trimming circuit	84
Figure 48. Settling of PI weights during trimming found from circuit simulations. TEST=12.3 μs	85
Figure 49. PI weights after trimming for different LPF bandwidth, using Verilog-A model of the trimming loop.	86
Figure 50. Settling of INL, DNL during closed loop trimming from circuit simulations.	87
Figure 51. INL and DNL for few worst case PVT, σ , A with F=100-500 MHz found from circuit simulations .	88

LIST OF TABLES

Table 1– Comparison with other work	75
Table 2– PI non-linearity comparison	88

LIST OF SYMBOLS AND ABBREVIATIONS

Symbols

Φ, ϕ, Θ	Phase of the PI input and output clock or the phase of the incoming data
$\Delta\emptyset$	One LSB phase step of the PI
α, β	Weights of the clock phase vectors which are used for interpolation
$I(k)$	Nonlinearity of the PI compared to an ideal characteristics
$\hat{I}(k)$	Estimated Non-linearity of the PI $I(k)$
ϵ	Phase error between the recovered clock and the data phase
ε	Quantized value of the phase error ϵ .
ε_l	Quantized phase error obtained after filtering ε through inverse filter
$\bar{\varepsilon}_l$	Average value of ε_l obtained after collecting multiple samples
k, \mathbf{K}	Input code to the PI and its corresponding random variable.
\mathbf{K}_n	PI input code random variable at time sample n
K_{PD}	Linearized gain of the BBPD
$H(z), h[n]$	Z-Domain Transfer function and its impulse response
V_n	Pseudo-Random White Noise Sequence at time sample n
Q_n	Quantization noise at time sample n
$E\{X\}$	Stastical expectation operator
P_{lki}^{\leftarrow}	Backward - state transition probability $P\{\mathbf{K}_{n-i} = l \mathbf{K}_n = k\}$
P_{lki}^{\rightarrow}	Forward - state transition probability $P\{\mathbf{K}_n = l \mathbf{K}_{n-i} = k\}$
$f_{\mathbf{K}_{n-i}, \mathbf{K}_n}$	Joint PDF of \mathbf{K}_{n-i} and \mathbf{K}_n
$R_K[i]$	Autocorrelation function of \mathbf{K}
ρ	Ratio of actual and estimated BBPD gain
f_B	3dB Bandwidth of the LPF in the PI.

$\varphi_{M0}, \varphi_{M1}$	Adjacent clock phases used for interpolation
φ_C	Output clock phase obtained after interpolation

Abbreviations

PI	Phase Interpolator
LPF	Low Pass Filter
CDR	Clock and Data Recovery circuit
LF	Digital Loop Filter of the CDR
Des.	Deserializer
PI Cont.	Phase Interpolator Controller
BBPD	Bang-bang Phase Detector
UI	Unit Interval representing one bit period of the incoming data
DCCA	Digital Controlled Capacitor Array
TSPI	Two Step Phase Interpolator