NON-LINEARITY ESTIMATION FOR PHASE INTERPOLATORS USED IN BANG-BANG CLOCK AND DATA RECOVERY CIRCUITS

ARCHIT JOSHI

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

JULY 2019

NON-LINEARITY ESTIMATION FOR PHASE INTERPOLATORS
USED IN BANG-BANG CLOCK AND DATA RECOVERY CIRCUITS

by

Archit Joshi

Department of Electrical Engineering

Submitted

in fulfillment of the requirement of the degree of Doctor of Philosophy

to the

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

JULY 2019

CERTIFICATE

This is to certify that the thesis entitled "**Non-linearity Estimation for Phase Interpolators Used in Bang-Bang Clock and Data recovery Circuits**" being submitted by **Archit Joshi** to Indian Institute of Technology - Delhi (India), for the award of the **Doctor of Philosophy** in Electrical Engineering is a bona fide research work carried out by him under my guidance and supervision. The research work has reached the requisite standard. I hereby declare that the content of the thesis has not been submitted to any other university for award of any degree or diploma.

Supervisor

Dr. Mukul Sarkar,
Associate Professor,
Department of Electrical Engineering,
IIT. Delhi

ACKNOWLEDGEMENTS

My foremost appreciation must go to my advisor, Dr. Mukul Sarkar. His extensive vision and creative thinking have provided the source of inspiration for me. The academic research experiences have encouraged me for exploring the integrated circuits further. I am especially grateful to the members of committee, Dr. Suri, Dr. Chatterjee and Dr. Panda for their valuable suggestions and help. Through their instructions, I learned how to pursue research. It has been a great pleasure to work in the Electrical Engineering Lab. I would like to acknowledge to all of my colleagues for their suggestions and help.

My sincere appreciation goes to my parents, wife and son who have always given me unconditional love, guidance, and support. Without them, none of these could have been accomplished.

Archit Joshi

ABSTRACT

Phase Interpolators are Digital-to-Phase (time) converters and are widely used for providing the adjustable delay needed for phase locking in Clock and Data Recovery (CDR) circuits with Bang-Bang Phase Detectors (BBPD). The non-linearity of the Phase interpolators injects unwanted jitter into the clocks of the CDR which degrade the performance of the CDR. Hence non-linearity needs to be reduced/corrected.

This research focuses on a technique to estimate the non-linearity of the PI during real circuit operation. When the non-linearity estimates are available, useful insight into the behavior of the PI in run time can be obtained. A mathematical model of the basic estimation technique and the accuracy of estimation is presented. Results of proposed mathematical model and MATLAB model are compared.

The non-linearity estimates are used to correct the non-linearity of the PI in a closed loop manner. In this work, two different methods are used to correct the non-linearity of the PI. The first one focuses on adaptation of the bandwidth of Low pass filter of the PI, using a 'reference non-linearity' approach. A mathematical model for the accuracy of estimation using this reference non-linearity approach and tradeoffs of various design parameters is presented. The circuits are fabricated in 180nm CMOS technology. The second approach uses the trimming of the weights of the Phase interpolator to reduce the non-linearity. This approach minimizes the Differential (DNL) as well as Integral Non-linearity (INL) of the PI. A weight update equation is also presented.

सार

फेज इंटरपोलर डिजिटल-टू-फेज (समय) कन्वर्टर्स हैं और इन्हें बैंग-बैंग फेज डिटेक्टर (बीबीपीडी) के साथ क्लॉक और डेटा रिकवरी (सीडीआर) सर्किट में फेज लॉकिंग के लिए आवश्यक समायोज्य विलंब प्रदान करने के लिए उपयोग किया जाता है। फेज इंटरपोलर्स की गैर-रैखिकता सीडीआर की घड़ियों में अवांछित घबराहट का इंजेक्शन लगाती है जो सीडीआर के प्रदर्शन को नीचा दिखाती है। इसलिए गैर-रैखिकता को कम / दुरुस्त करने की आवश्यकता है। यह शोध वास्तविक सर्किट ऑपरेशन के दौरान पीआई की गैर-रैखिकता का अनुमान लगाने की तकनीक पर केंद्रित है। जब गैर-रैखिकता अनुमान उपलब्ध होते हैं, तो रन समय में पीआई के व्यवहार में उपयोगी अंतर्दृष्टि प्राप्त की जा सकती है। मूल अनुमान तकनीक और अनुमान की सटीकता का एक गणितीय मॉडल प्रस्तुत किया गया है। प्रस्तावित गणितीय मॉडल और MATLAB मॉडल के परिणामों की तुलना की जाती है। गैर-रैखिकता अनुमानों का उपयोग पीआई की गैर-रैखिकता को बंद लूप तरीके से ठीक करने के लिए किया जाता है। इस काम में, पीआई की गैर-रैखिकता को सही करने के लिए दो अलग-अलग तरीकों का उपयोग किया जाता है। पहले एक 'संदर्भ गैर-रैखिकता' दृष्टिकोण का उपयोग करके, पीआई के लो पास फिल्टर की बैंडविड्थ के अनुकूलन पर ध्यान केंद्रित करता है। इस संदर्भ का उपयोग करते हुए अनुमान की सटीकता के लिए एक गणितीय मॉडल गैर-रैखिकता दृष्टिकोण और विभिन्न डिजाइन मापदंडों के ट्रेडऑफ़ प्रस्तुत किया गया है। सर्किट 180nm CMOS तकनीक में गढ़े गए हैं। दूसरा दृष्टिकोण गैर-रैखिकता को कम करने के लिए चरण प्रक्षेपक के भार के ट्रिमिंग का उपयोग करता है। यह दृष्टिकोण विभेदक (DNL) के साथ-साथ PI के इंटीग्रल नॉन-लीनियरिटी (INL) को कम करता है। एक वजन अद्यतन समीकरण भी प्रस्तुत किया गया है।

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

Symbols

Φ, ϕ, Θ	Phase of the PI input and output clock or the phase of the incoming data
$\Delta\emptyset$	One LSB phase step of the PI
α, β	Weights of the clock phase vectors which are used for interpolation
$I(k)$	Nonlinearity of the PI compared to an ideal characteristics
$\hat{I}(k)$	Estimated Non-linearity of the PI $I(k)$
$\in$	Phase error between the recovered clock and the data phase
ε	Quantized value of the phase error ϵ.
ε_I	Quantized phase error obtained after filtering ε through inverse filter
$\overline{\varepsilon_I}$	Average value of ε_I obtained after collecting multiple samples
$k, \boldsymbol{K}$	Input code to the PI and its corresponding random variable.
$\boldsymbol{K}_n$	PI input code random variable at time sample n
K_{PD}	Linearized gain of the BBPD
$H(z), h[n]$	Z-Domain Transfer function and its impulse response
$\boldsymbol{V}_n$	Pseudo-Random White Noise Sequence at time sample n
Q_n	Quantization noise at time sample n
$E\{X\}$	Stastical expectation operator
$P_{\overleftarrow{lki}}$	Backward - state transition probability $P\{\boldsymbol{K}_{n-i} = l \mid \boldsymbol{K}_n = k\}$
$P_{\overrightarrow{lki}}$	Forward - state transition probability $P\{\boldsymbol{K}_n = l \mid \boldsymbol{K}_{n-i} = k\}$
$f_{\boldsymbol{K}_{n-i},\boldsymbol{K}_n}$	Joint PDF of $\boldsymbol{K}_{n-i}$ and $\boldsymbol{K}_n$
$R_K[i]$	Autocorrelation function of $\boldsymbol{K}$
ρ	Ratio of actual and estimated BBPD gain
f_B	3dB Bandwidth of the LPF in the PI.

$\varphi_{M0}, \varphi_{M1}$	Adjacent clock phases used for interpolation
φ_C	Output clock phase obtained after interpolation

Abbreviations

PI	Phase Interpolator
LPF	Low Pass Filter
CDR	Clock and Data Recovery circuit
LF	Digital Loop Filter of the CDR
Des.	Deserializer
PI Cont.	Phase Interpolator Controller
BBPD	Bang-bang Phase Detector
UI	Unit Interval representing one bit period of the incoming data
DCCA	Digital Controlled Capacitor Array
TSPI	Two Step Phase Interpolator