DESIGN OF ERROR RESILIENT SRAM

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by

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Dedication

Dedicated to my beloved parents, for their blessings and support throughout my life.

Certificate

This is to certify that the thesis entitled **"Design of Error Resilient SRAM"** being submitted by **Mr. Ashish Kumar** for the award of degree of **Doctor of Philosophy** to the Electrical Engineering Department, Indian Institute of Technology Delhi, is a record of bonafide work done by him under our supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

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Abstract

SRAM design in deep submicron regime is riddled with multiple issues due to increasing device variability, near-threshold and sub-threshold region of operation and increasing on-chip capacity. SRAM cell is normally designed with minimum possible device size to minimize area. This results in large variability amongst devices and thus affects the stability parameters of the SRAM cell. Furthermore, in System on Chip (SoC), wherein memory plays an important role, there is a need to operate at lowest possible supply voltage in order to minimize the power consumption. To enable a lower minimum functional voltage (Vmin), all components of SoC should be functional at targeted Vmin. SRAM comes in the critical path of this requirement. It is thus important to ensure error free operation of the memory.

This issue of error free operation of memory has been addressed by using multiple design strategies. Designing a larger SRAM cell helps to reduce variations and increase the stability. However, area penalty associated with this approach limits its usage. Use of more than six transistors to design SRAM cell has been shown to help increase stability [1]. This also comes with an unacceptable area overhead for applications where large capacity memory is required. Use of Error Correcting Code (ECC) is widely used to detect and correct errors in memory [2] [3]. However, correction of multi-bit failures is difficult to achieve. Multiple assist schemes and design strategies has been used to increase the stability of memory cell [4] [5]. Assist schemes help to achieve a robust read or write operation and come at a cost of Power, Performance and Area (PPA) overhead. Worst-case design approach results in excessive margin at typical Process, Voltage and Temperature (PVT). New design strategies are needed for a robust and low energy operation of the memory.

In order to have a robust memory operation we need to ensure that the design is capable of detecting and correcting failures. This capability is desired with minimum loss in area power and performance. To avoid a failure, we need to ensure a robust design with assist circuits that do not penalize the PPA significantly. Low voltage operation of the memory may induce significant multi-bit error count. Margin failure in memory due to ageing, dynamic IR Drop or substrate noise may also result in multi-bit failures. Hence, we need to design a simple and robust correction mechanism.

This work provides a scheme for the run-time error detection and correction in SRAM. An error can be caused either due to an incorrect write or an incorrect read operation. The proposed solution applies correction mechanism in place with negligible impact on the memory throughput. This correction mechanism is also used to reduce the operational minimum voltage (Vmin). However, this does not detect the read failures due to insufficient static noise margin (SNM). This issue is addressed through the proposed read assist scheme that ensures the read stability of the memory cell. This work also proposes a write assist scheme, where the assist is applied for only those PVTs where they are needed. This helps to avoid power consumption at other PVTs where the assist is not needed. This also helps to avoid excessive electrical stress at higher supply voltages due to assist scheme and ensures operation within reliability limits.

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Abbreviations

6T-SRAM Cell	Six Transistor SRAM Cell
8T-SRAM Cell	Eight Transistor SRAM Cell
BL	Bit Line
BLB	Bit Line Bar
DBL	Dummy Bit Line
DBLB	Dummy Bit Line Bar
ECC	Error Correcting Code
FD-SOI	Fully Depleted Silicon on Insulator
FS,FF	Fast (NMOS) Slow (PMOS), Fast (NMOS) Fast (PMOS) {Process}
FIT	Failure in Time
HCE	Hot Carrier Effect
NBTI	Negative Bias and Temperature Instability
OLT	Operational Life-Time
PD,PG,PU	Pull Down, Pass Gate, Pull Up (Devices)
PPA	Power Performance and Area
PVT	Process, Voltage and Temperature
RA	Read Assist
RDF	Random Dopant Fluctuations
RVDD	Row VDD
SA	Sense Amplifier
SAEN	Sense Amplifier Enable (signal)
SAF	Sense Amplifier False (node)
SAT	Sense Amplifier True (node)
SEU	Single Event Upset
SF, SS	Slow (NMOS) Fast (PMOS), Slow (NMOS) Slow (PMOS) {Process}
SNM	Static Noise Margin
SoC	System on Chip
SRAM	Static Random Access Memory
TDDB	Time Dependent Dielectric Breakdown
TT	Typical (NMOS) Typical (PMOS) {Process}
TVC	Transient Voltage Collapse
VDDMA	VDD Memory Array
VDDMP	VDD Memory Periphery
VMIN	Minimum Functional Voltage
WA	Write Assist
WL	Word Line
WLUD	Word-Line Under-Drive
WM	Write Margin