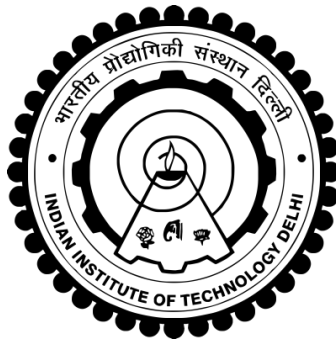


LOW-FREQUENCY NOISE REDUCTION TECHNIQUES FOR CMOS IMAGE SENSORS

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LOW-FREQUENCY NOISE REDUCTION TECHNIQUES FOR CMOS IMAGE SENSORS

by

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Department Of Electrical Engineering

Submitted

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To Krishna...

Certificate

This is to certify that the thesis entitled, “**Low-Frequency Noise Reduction Techniques for CMOS Image Sensors,**” being submitted by **Mr. Kapil Jainwal** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

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Abstract

Mother nature created life and blessed us with this beautiful world. Mankind always takes inspiration and resources from nature to train the brain and to do innovations for making the life easier. There are countless inventions that make this world a better and comfortable place to live in. With the evolution of technology, humans have begun to build artificial replicas similar to their own body.

Eyes, one of the most important senses of the human body, became the inspiration behind the invention of the camera. Eyes respond to the light information in a scene, extract and transfer it into the electrical signal and send the information to the brain for processing. Based on the working principle of eyes, a camera extracts the information from a scene, processes, stores, and reuses it. Being one of the finest inventions in the history of mankind, cameras found their applications in fields like entertainment, information, biomedical, geology, and space. In some critical applications, it becomes very important to extract and process the information from a scene with a fine accuracy and precision.

The performance parameters of a camera decide the quality of a picture taken from it. One of the very important parameters is the dynamic range (DR). The DR is a function of maximum and minimum perceivable input light by an image sensor or imager. The saturation level of the pixel sensor limits the maximum value of the input. The minimum detectable light depends on the pixel noise under the dark or low-illumination conditions. Therefore, to increase DR, it is important to reduce the noise of a pixel. In order to remove, it is critical to know and develop an understanding of all the sources of the noise

components associated with the circuitry of a camera.

Most of the modern age digital cameras are based on CMOS image sensors. Unfortunately, these image sensors show a poor noise performance compared to their counterpart, charge-coupled device (CCD) based image sensors.

With the growing technology, cameras became a system-on-a-chip, to achieve portability, lower cost, and lower power consumption. CMOS cameras are mostly embedded in battery-operated systems such as mobile phones, where power consumption is a major issue. Low-power budget and miniaturized circuitry, employed with components shrunk up to the nanometer range, severely hamper noise performance. The minimum detectable signal is limited by pixel offset and random noise, including the low-frequency noise of the in-pixel source follower (SF) and the thermal noise of the switches. In-pixel offset and thermal noise from the reset switch can be canceled by techniques like double sampling (DS) and thus, the source follower low-frequency noise remains as a major noise source to limit the dynamic range of an image sensor. In addition, the non-linearity of the SF also hampers the output of a pixel sensor.

The low-frequency noise includes phenomenon like RTS, burst, and $1/f$ noise. Random trapping and de-trapping of mobile charge carriers, into the lattice defects, present at Si-SiO₂ interface of a MOS device in the form of unsaturated energy states or traps, are considered as a major cause of the low-frequency noise. Although many models have been proposed by many researchers, yet the exact origin of the $1/f$ noise is still unclear. The low-frequency noise model presented in this thesis is based on McWhorter's carrier density

fluctuation (ΔN), which considers that the $1/f$ noise originates from the number of mobile charge carrier fluctuation into the channel and its spectrum is the superposition of the RTS noise from multiple traps. In the explored mathematical model, the low-frequency noise power spectral density is derived for a MOSFET device under variable biasing conditions. The model considers the non-stationarity in the noise behavior due to time-varying biasing conditions, which is more suitable for the application such as CMOS image sensors. The theoretical modeling and analysis of the RTS and $1/f$ noise in MOS transistor show that the $1/f$ noise power can be reduced by decreasing the duty cycle (D) of switched biasing signal. In this thesis, an analysis of $1/f$ noise reduction model is presented, and it is shown that the RTS noise reduction is accompanied with a shift in the corner frequency (f_c) of the $1/f$ noise and the value of the shift is a function of continuous ON time (T_{on}) of the device. The reduction in $1/f$ noise is also shown experimentally. The circuit configuration with multiple identical transistor stages is used to produce a continuous output instead of a discrete signal. The measured results show that the proposed technique reduces the integrated $1/f$ noise power by approximately 5.9 dB at switching frequency (f_s) of 100 KHz for 2 stage configuration, which is extended up to 16 dB at f_s of 5 MHz for 6 stage configuration.

The latter part of this thesis presents a low-noise CMOS image sensor prototype with enhanced dynamic range (DR) using a novel in-pixel chopping technique. The proposed in-pixel chopping technique is used to reduce the low-frequency or $1/f$ noise of the SF. A conventional 3T active pixel, with n-well/p-sub photodiode (PD), is modified to implement a chopper inside a pixel. A single minimum sized nMOS transistor is used in each pixel,

without any considerable compromise in the fill-factor (FF). The reduction in the temporal noise also results in an enhanced dynamic range of the image sensor. Moreover, the readout comprises a column level high gain chopper amplifier that also reduces the non-linearity of the source follower.

To validate the proposed technique, a prototype sensor has been fabricated in 350 nm standard CMOS technology, which consists of a 128×128 sized pixel array with in-pixel chopping and column level read-out circuitry. The temporal noise is measured as $280 \mu\text{V}_{\text{RMS}}$ at the chopping frequency (f_{ch}) of 8 MHz, which shows a reduction in the integrated noise power by 11 dB. In addition, the column level high-gain amplifier makes the output follow the PD node linearly for a wider range of light integration, increasing the linearity and hence, the usable output swing. Due to the reduced noise floor, the dynamic range is enhanced from 65 dB to 76 dB, using the proposed technique.

सार

माँ प्रकृति ने जीवन बनाया और हमें इस खूबसूरत दुनिया के साथ आशीर्वाद दिया। मैनकाइंड हमेशा लेता है मस्तिष्क को प्रशिक्षित करने और बनाने के लिए नवाचार करने के लिए प्रकृति से प्रेरणा और संसाधन आसान है। ऐसे अनगिनत आविष्कार हैं जो इस दुनिया को बेहतर और आरामदायक बनाते हैं रहने के लिए जगह। प्रौद्योगिकी के विकास के साथ, मानव ने कृत्रिम निर्माण करना शुरू कर दिया है अपने शरीर के समान प्रतिकृतियां।

आंखें, मानव शरीर की सबसे महत्वपूर्ण इंद्रियों में से एक, प्रेरणा बन गई कैमरे के आविष्कार के पीछे। आंखें एक दृश्य में प्रकाश की जानकारी का जवाब देती हैं, निकालने और इसे विद्युत संकेत में स्थानांतरित करने और मस्तिष्क के लिए जानकारी भेजने के लिए प्रसंस्करण। आंखों के कार्य सिद्धांत के आधार पर, एक कैमरा जानकारी को निकालता है एक दृश्य, प्रक्रियाएं, भंडार, और इसका पुनः उपयोग करता है। इतिहास के सबसे बेहतरीन आविष्कारों में से एक होने के नाते मानव जाति के, कैमरों ने मनोरंजन, सूचना, बायोमेडिकल जैसे क्षेत्रों में अपने आवेदन पाए। भूविज्ञान, और अंतरिक्ष। कुछ महत्वपूर्ण अनुप्रयोगों में, यह बहुत महत्वपूर्ण हो जाता है एक दृश्य से जानकारी को ठीक सटीकता और सटीकता के साथ निकालें और संसाधित करें।

एक कैमरे के प्रदर्शन मापदंडों से लिया गया एक तस्वीर की गुणवत्ता तय करते हैं। बहुत महत्वपूर्ण मापदंडों में से एक गतिशील रेंज (DR) है। DR एक फंक्शन है एक छवि संवेदक या इमेजर द्वारा अधिकतम और न्यूनतम विचार करने योग्य इनपुट प्रकाश। पिक्सेल सेंसर का संतृप्ति स्तर इनपुट के अधिकतम मूल्य को सीमित करता है। न्यूनतम पता लगाने योग्य प्रकाश अंधेरे या कम रोशनी की स्थिति के तहत पिक्सेल शोर पर निर्भर करता है। इसलिए, DR बढ़ाने के लिए, पिक्सेल के शोर को कम करना महत्वपूर्ण है। हटाने के लिए, शोर के सभी स्रोतों की समझ को जानना और विकसित करना महत्वपूर्ण है एक कैमरे के सर्किट्री से जुड़े घटक।

आधुनिक युग के अधिकांश डिजिटल कैमरे CMOS इमेज सेंसर पर आधारित हैं। दुर्भाग्य से, ये छवि सेंसर अपने समकक्ष की तुलना में खराब शोर प्रदर्शन दिखाते हैं, प्रभारी-युग्मित डिवाइस (सीसीडी) आधारित छवि सेंसर।

बढ़ती प्रौद्योगिकी के साथ, कैमरे पोर्टेबिलिटी प्राप्त करने के लिए एक सिस्टम-ऑन-ए-चिप बन गए, कम लागत, और कम बिजली की खपत। CMOS कैमरे ज्यादातर एम्बेडेड होते हैं बैटरी चालित प्रणालियों में जैसे कि मोबाइल फोन, जहां बिजली की खपत एक प्रमुख है मुद्दा। कम बिजली के बजट और लघु सर्किटरी, घटकों के साथ नियोजित नैनोमीटर रेंज तक, गंभीर रूप से शोर प्रदर्शन में बाधा। न्यूनतम पता लगाने योग्य संकेत पिक्सेल ऑफसेट और यादृच्छिक शोर द्वारा सीमित है, जिसमें निम्न-आवृत्ति शोर शामिल है इन-पिक्सेल स्रोत अनुयायी (एसएफ) और स्विच का थर्मल शोर। इन-पिक्सेल ऑफसेट और रीसेट स्विच से थर्मल शोर को डबल सैंपलिंग जैसी तकनीकों द्वारा रद्द किया जा सकता है (डीएस) और इस प्रकार, स्रोत अनुयायी कम आवृत्ति शोर एक प्रमुख शोर स्रोत के रूप में रहता है एक छवि सेंसर की गतिशील सीमा को सीमित करें। इसके अलावा, एसएफ की गैर-रैखिकता भी पिक्सेल सेंसर के आउटपुट को बाधित करता है।

कम आवृत्ति के शोर में आरटीएस, फट और $1 = \text{एफ शोर}$ जैसी घटना शामिल है। बिना सोचे समझेजाली चार्ज में वर्तमान में मोबाइल चार्ज कैरियर्स को फँसाना और गिराना असंतृप्त ऊर्जा राज्यों या जाल के रूप में MOS डिवाइस के Si-SiO₂ इंटरफ़ेस पर, कम आवृत्ति के शोर का एक प्रमुख कारण माना जाता है। हालांकि कई मॉडल हैं कई शोधकर्ताओं द्वारा प्रस्तावित किया गया है, फिर भी $1 / \text{एफ शोर}$ की सटीक उत्पत्ति अभी भी स्पष्ट नहीं है। इस थीसिस में प्रस्तुत कम-आवृत्ति शोर मॉडल मैकहॉटर के वाहक घनत्व पर आधारित है उतार-चढ़ाव (एन), जो मानता है कि $1 / \text{एफ शोर}$ मोबाइल की संख्या से उत्पन्न होता है पटेल और उसके स्पेक्ट्रम में चार्ज वाहक उतार-चढ़ाव आरटीएस का सुपरपोजिशन है कई जाल से बैल। खोजे गए गणितीय मॉडल में, कम आवृत्ति वाला भाईपावर वर्णक्रमीय घनत्व MOSFET डिवाइस के लिए वैरिबल बायसिंग परिस्थितियों में बनाया गया है। मॉडल समय-अलग-अलग पूर्वाग्रह के कारण शोर व्यवहार में गैर-स्थिरता पर विचार करता है स्थितियाँ, जो कि CMOS इमेज सेंसर जैसे एप्लिकेशन के लिए अधिक उपयुक्त हैं। सैद्धांतिक प्रशिक्षण और आरटीएस का विश्लेषण और एमोइटिस्टर में $1 / f$ शोर से पता चलता है कि $1 = \text{चोकर शक्ति को कम किया जा सकता है}$ स्विचिंग पूर्वाग्रह के कर्म चक्र (डी) को कम करके संकेत। इस थीसिस में, $1 = f$ शोर में कमी मॉडल का विश्लेषण प्रस्तुत किया गया है, और यह दिखाया गया है आरटीएस शोर में कमी के कोने की आवृत्ति (एफसी) में परिवर्तन के साथ है $1 = \text{फा और शिफ्ट का मान डिवाइस के निरंतर समय (टन) का एक कार्य है।}$ $1 = \text{एफ शोर में कमी को प्रभावी रूप से भी दिखाया गया है।}$ सर्किट विन्यास कई समान ट्रांजिस्टर चरणों का उपयोग असतत के बजाय एक निरंतर उत्पादन करने के लिए किया जाता है संकेत। परीक्षा परिणाम बताते हैं कि प्रस्तावित तकनीक एकीकृत को कम करती है 2 के लिए 100 KHz की स्विचिंग आवृत्ति (एफएस) पर लगभग 5.9 डीबीआई $1 = \text{एफएवी शक्ति स्टेज सहमत, जिसे 6 चरण सहमत के लिए 5 मेगाहर्ट्ज के एफएस पर 16 डीबी तक बढ़ाया जाता है।}$

यह थीसिस का उत्तरार्द्ध एक कम-शोर सीएमओ छवि छायांकन के साथ प्रस्तुत करता है संलग्न डायनामिक रेंज (DR) एक उपन्यास इन-पिक्सेल चॉपिंग तकनीक का उपयोग कर रहा है। प्रस्तावित इन-पिक्सेल चॉपिंग तकनीक का इस्तेमाल एसएफ की कम आवृत्ति या $1 = \text{एफ शोर को कम करने के लिए किया जाता है।}$ एन-well / p-sub photodiode (PD) के साथ पारंपरिक 3T सक्रिय पिक्सेल को लागू करने के लिए संशोधित किया गया है) एक पिक्सेल के अंदर एक हेलिकॉप्टर। प्रत्येक पिक्सेल में एक न्यूनतम न्यूनतम nMOS ट्रांजिस्टर का उपयोग किया जाता है, फिल-फैक्टर (एफएफ) में किसी भी काफी समझौता किए बिना। लौकिक में कमी शोर भी छवि संवेदक के एक बढ़ाया गतिशील रेंज में परिणाम है। इसके अलावा, रीडआउट एक स्तंभ स्तर उच्च लाभ हेलिकॉप्टर एम्पलीफायर शामिल है जो की गैर-रैखिकता को भी कम करता है स्रोत अनुयायी।

प्रस्तावित तकनीक को मान्य करने के लिए, 350 एनएम में एक प्रोटोटाइप सेंसर तैयार किया गया है मानक CMOS तकनीक, जिसमें इन-पिक्सेल के साथ 128 128 पिक्सेल पिक्सेल सरणी होती है चॉपिंग और कॉलम स्तर रीड-आउट सर्किटरी। अस्थायी शोर को 280 के रूप में मापा जाता है 8 मेगाहर्ट्ज के चॉपिंग फ्रीक्वेंसी (f_{ch}) पर वीआरएमएस, जो एकीकृत में कमी दर्शाता है 11 dB द्वारा शोर शक्ति। इसके अलावा, स्तंभ स्तर उच्च-लाभ एम्पलीफायर आउटपुट बनाता है रैखिक एकीकरण को बढ़ाते हुए प्रकाश एकीकरण की एक विस्तृत श्रृंखला के लिए पीडी नोड का रैखिक रूप से पालन करें और इसलिए, प्रयोग करने योग्य आउटपुट स्विंग। कम शोर मंजिल के कारण, गतिशील रेंज है प्रस्तावित तकनीक का उपयोग कर 65 डीबी से बढ़ाकर 76 डीबी कर दिया गया है।

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