Low Frequency Noise Characterization and Modeling of Advanced CMOS Devices

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Low Frequency Noise Characterization and Modeling of Advanced CMOS Devices

by

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to the

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Dedicated

to

My Beloved Family

Certificate

This is to certify that the thesis entitled ***"Low Frequency Noise Characterization and Modeling of Advanced CMOS Devices"***, being submitted by **Ms. Shruti Pathak** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering is a record of bonafide research work carried out by her under my supervision and guidance. The results contained in the thesis have not been submitted in part or full to any other University or Institute for the award of any degree or diploma.

I certify that she has pursued the prescribed course of research.

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ABSTRACT

The relentless demand for high-speed processing and improved integration in modern electronic systems has compelled device engineers to pursue aggressive scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs). This downscaling has led to remarkable improvements in transistor performance and speed, achieved by reducing the geometric dimensions of these devices and substituting conventional material combinations with newer, superior alternatives. However, the advantages of scaling down are accompanied by considerable challenges, as various short-channel effects (SCEs) start to emerge. Key SCEs such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and punch-through start to affect device behavior, presenting obstacles to achieving optimal performance.

One critical challenge that arises from continued scaling is the increase in low frequency noise, particularly flicker noise ($1/f$ noise). This type of noise is intrinsic to the operation of MOS devices and tends to scale with the shrinking dimensions of the transistors. As device sizes are reduced, flicker noise becomes more prominent and poses a serious limitation to the performance of MOS devices, especially in high-precision and low-power applications. Moreover, $1/f$ noise becomes even more critical at cryogenic temperatures, a regime essential for quantum computing applications. The precise control and reduction of this noise at extremely low temperatures is a major concern for researchers aiming to optimize devices for quantum computing, where noise can disrupt quantum coherence.

This thesis focuses on an in-depth investigation of flicker noise in advanced CMOS (complementary metal-oxide-semiconductor) devices. By performing detailed characterization, thorough analysis, and advanced modeling techniques, the study aims to uncover the complexities of flicker noise to enhance understanding and explore its potential applications. To achieve this, comprehensive characterization and analysis are conducted on on-wafer partially depleted silicon-on-insulator field-effect transistors (PDSOI FETs), bulk FETs, and bulk fin field-effect transistors (FinFETs) across a wide

temperature range, from 300K to 10K. The study also investigates how scaling affects flicker noise in MOS devices. In addition, the impact of hot-carrier degradation on flicker noise in 45-nm node PDSOI FETs are explored, offering key insights into the reliability concerns related to this noise phenomenon. Furthermore, low-temperature compact modeling of CMOS devices is achieved by enhancing industry-standard BSIM (Berkeley short-channel IGFET model) models with additional equations in Verilog-A, allowing for more accurate simulation of DC and $1/f$ noise behavior at cryogenic temperatures. The modeling of thin and thick oxide MOSFETs using commercial process design kits (PDK) is also presented.

सार

आधुनिक इलेक्ट्रॉनिक प्रणालियों में उच्च-गति प्रसंस्करण और बेहतर इंटीग्रेशन की बढ़ती मांग ने डिवाइस इंजीनियर्स को मेटल-ऑक्साइड-सेमीकंडक्टर फील्ड-इफेक्ट ट्रांजिस्टर (MOSFETs) का आक्रामक रूप से स्केलिंग करने के लिए प्रेरित किया है। इस डाउनस्केलिंग ने ट्रांजिस्टर के परफॉर्मेंस और स्पीड में उल्लेखनीय सुधार किए हैं, जो इन डिवाइस के ज्योमेट्रिक डाइमेंशन्स को घटाकर और ट्रेडिशनल मटीरियल कॉम्बिनेशन्स को नई, सुपीरियर अल्टरनेटिव्स से रिप्लेस करके प्राप्त किए गए हैं। हालांकि, स्केलिंग के लाभों के साथ कई चुनौतियां भी उत्पन्न होती हैं, क्योंकि विभिन्न शॉर्ट-चैनल इफेक्ट्स (SCEs) उभरने लगते हैं। प्रमुख SCEs जैसे थ्रेशोल्ड वोल्टेज रोल-ऑफ, ड्रेन-इंड्यूस्ड बैरियर लोअरिंग (DIBL), और पंच-थ्रू डिवाइस के बिहेवियर को प्रभावित करते हैं और ऑप्टिमल परफॉर्मेंस प्राप्त करने में बाधा उत्पन्न करते हैं।

कंटीन्यूड स्केलिंग से उत्पन्न होने वाली एक प्रमुख चैलेंज लो-फ्रिक्वेंसी नॉइज़, विशेष रूप से फ्लिकर नॉइज़ ($1/f$ नॉइज़), में वृद्धि है। यह प्रकार का नॉइज़ MOS डिवाइस के ऑपरेशन का एक इंट्रिंसिक पहलू है और ट्रांजिस्टर के डाइमेंशन्स के सिकुड़ने के साथ बढ़ता है। जैसे-जैसे डिवाइस का साइज कम होता है, फ्लिकर नॉइज़ अधिक प्रमुख हो जाता है और हाई-प्रिसीजन और लो-पावर एप्लिकेशन्स में MOS डिवाइस के परफॉर्मेंस के लिए एक सीरियस लिमिटेशन प्रस्तुत करता है। इसके अलावा, $1/f$ नॉइज़ क्रायोजेनिक टेंपरेचर पर और भी ज्यादा क्रिटिकल हो जाता है, जो क्वांटम कंप्यूटिंग एप्लिकेशन्स के लिए आवश्यक है। अत्यधिक कम तापमान पर इस नॉइज़ को सटीक रूप से कंट्रोल और कम करना उन रिसर्चर्स के लिए एक मेजर कंसर्न है जो क्वांटम कंप्यूटिंग के लिए डिवाइस को ऑप्टिमाइज़ करने का प्रयास कर रहे हैं, क्योंकि नॉइज़ क्वांटम कोहेरेंस को डिस्टर्ब कर सकता है।

यह थीसिस उन्नत CMOS (कॉम्प्लीमेंटरी मेटल-ऑक्साइड-सेमीकंडक्टर) डिवाइस में फ्लिकर नॉइज़ की इन-डेप्थ इन्वेस्टिगेशन पर फोकस करती है। डिटेल्ड कैरेक्टराइजेशन, एनालिसिस, और एडवांस्ड मॉडलिंग तकनीकों का उपयोग करके, यह स्टडी फ्लिकर नॉइज़ की जटिलताओं को समझने और इसके पोटेंशियल एप्लिकेशन्स का पता लगाने का प्रयास करती है। इस उद्देश्य को प्राप्त करने के लिए, 300K से 10K तक के विस्तृत टेंपरेचर रेंज में ऑन-वेफर

पार्शियली डिप्लीटेड सिलिकॉन-ऑन-इन्सुलेटर फील्ड-इफेक्ट ट्रांजिस्टर (PDSOI FETs), बल्क FETs और बल्क फिन फील्ड-इफेक्ट ट्रांजिस्टर (FinFETs) पर व्यापक कैरेक्टराइजेशन और एनालिसिस किया गया है। इसके साथ ही, MOS डिवाइस में स्केलिंग का फ्लिकर नॉइज़ पर प्रभाव भी इन्वेस्टिगेट किया गया है।

इसके अलावा, 45-नैनोमीटर नोड PDSOI FETs में हॉट-कैरियर डिग्रेडेशन का फ्लिकर नॉइज़ पर प्रभाव एक्सप्लोर किया गया है, जो इस नॉइज़ फेनोमेनन से संबंधित रिलायबिलिटी कंसर्न्स पर महत्वपूर्ण इनसाइट्स प्रदान करता है। इसके साथ ही, क्रायोजेनिक टेंपरेचर पर CMOS डिवाइस के लिए लो-टेम्परेचर कॉम्पैक्ट मॉडलिंग Verilog-A में एडिशनल इक्वेशन्स के साथ इंडस्ट्री-स्टैंडर्ड BSIM (बर्कले शॉर्ट-चैनल IGFET मॉडल) मॉडल को एन्हांस करके प्राप्त की गई है। यह मॉडलिंग पतली और मोटी ऑक्साइड MOSFETs को कमर्शियल प्रोसेस डिजाइन किट्स (PDK) का उपयोग करके प्रेजेंट करती है।

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LIST OF ABBREVIATIONS

Abbreviation	Description
BSIM	Berkeley Short-channel IGFET Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device under Test
FET	Field Effect Transistor
FinFET	Fin Field Effect Transistor
GSG	Ground Signal Ground
HCD	Hot-Carrier Degradation
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSM	Measure Stress Measure
PDK	Process Design Kit
PDSOI	Partially Depleted Silicon-on-Insulator
PSD	Power Spectral Density
RTN	Random Telegraph Noise
RVT	Regular Threshold Voltage
SCE	Short-Channel Effect
SLVT	Super-Low Threshold Voltage
SOC	System on Chip
SOI	Silicon-on-Insulator
SS	Subthreshold Swing