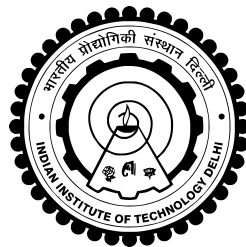


**DESIGN OF  
TIME DELAY INTEGRATION (TDI)  
CMOS IMAGE SENSORS**

**RAHUL KUMAR SINGH**



**Department of Electrical Engineering  
Indian Institute of Technology Delhi  
JULY 2025**

© Indian Institute of Technology Delhi (IITD), New Delhi, 2025

**DESIGN OF  
TIME DELAY INTEGRATION (TDI)  
CMOS IMAGE SENSORS**

by

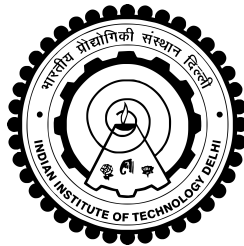
**RAHUL KUMAR SINGH**

Department of Electrical Engineering

Submitted in fulfillment of the requirements  
of the degree of

**Doctor of Philosophy**

to the



**Indian Institute of Technology Delhi**

**JULY 2025**

In loving memory of my baba late Shri Dalshringar Singh

# Certificate

This is to certify that the thesis entitled “**Design Of Time Delay Integration (TDI) CMOS Image Sensors**”, being submitted by **Mr. Rahul Kumar Singh** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by her under my supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

**Mukul Sarkar**

Professor,  
Department of Electrical Engineering,  
Indian Institute of Technology Delhi,  
Hauz Khas, New Delhi - 110016,  
INDIA.

# Acknowledgements

I offer my deepest gratitude to my thesis advisor, Dr. Mukul Sarkar, for his unwavering support and mentorship. I will remain grateful to him for providing me the opportunity to work in the field of image sensors. He not only taught me the basics of image sensors but also valuable life lessons that shaped my personality.

I would like to thank my dissertation committee, Dr. Shouri Chatterjee, Dr. Sumantra Dutta Roy, and Dr. Samaresh Das for their constructive criticism and valuable feedback throughout my PhD journey.

I extend my heartfelt gratitude to my dear friends Aashish T. R., Nitin Gupta, Shubham Sahay, Neha Priyadarshini, Tusha Tanya, and Akhlesh Rajak for their unwavering support and enriching discussions throughout my PhD journey. More than anything, thank you for infusing it with warmth, humor, and life. It would've been unimaginably dull without you. You stood by me and lifted me up during my lowest moments, when the chips were down quite literally.

I am grateful to the past and present members of our research group at IIT Delhi namely B. Bhuvan, Chandani Anand, Kapil Jainwal, Amandeep kaur, Deepak Mishra, Shivangi mani, Sanchita Chaudhary, Iram Ali, Suraj, Gargi, Shrikrishna Sharma, Abhishek Pradhan, Shivani, Yash Juyal, Yash Gupta and Madhav. I got introduced to new topics and ideas by interacting with them.

I have been fortunate to work with motivated students namely Prayag Wakale, Aashish Bora, Prabhleen Singh and Abhinav Bhattacharya. I am thankful to you all for teaching

me innovative and smarter ways. My special thanks to Aakash Vishwakarma and Siddhant Jain for their valuable feedback and suggestions during Imager characterization.

I am also grateful to the Department of Electrical Engineering at the Indian Institute of Technology Delhi for providing me with all the necessary facilities. I would also like to thank Mr. Rakesh Kumar, Mr. Satish and Mr. Yatindra who have helped me navigate administrative aspects during my research work.

I am deeply thankful to my parents, Mrs. Nilam Singh and Mr. Nagendra Singh, for their unwavering support and constant encouragement throughout this long and transformative journey. Their belief in me has been my greatest strength. I am deeply grateful to my wife Priya Kumari and my daughter Vaidehi for their unwavering love and support during the most challenging times of my journey. I am thankful to my family members Saurabh Singh, Suchi Singh and Abhay Singh for their motivation and support. I express my profound gratitude to my late grandfather, Shri Dalsringar Singh, whose wisdom and encouragement inspired me to pursue higher education.

Finally, I extend my sincere appreciation to all those both known and unsung who supported me directly or indirectly throughout my journey at IIT Delhi and whose names I could not accommodate in this brief acknowledgment.

# Abstract

In imaging applications whenever there is a relative motion between the sensor and the object, a limited integration time is available for photodiode to collect sufficient photons. Further, the number of available photons in pushbroom imaging and machine vision applications, are already very low. The low number of integrated photons lowers the signal-to-noise ratio (SNR), thus degrading the image quality. Time Delay Integration (TDI) is a well-known technique to enhance the SNR by increasing the signal level by using multiple capturing.

In present times, there is a great focus on increasing the total number of TDI stages in order to have better SNR. Increasing the TDI stage also has a side effect. Since conventional TDI sensors add the accumulated signals before analog to digital conversion (ADC), thus the accumulated signal is highly prone to saturation. Saturation may happen because of the change in scene from low light to moderate light. Furthermore, conventional TDI sensors use switched capacitor integrator based accumulators to store the integrated signal. These accumulator utilise operational amplifiers in accumulators. The operational amplifiers are limited in output voltage swing and are prone to saturation when higher number of TDI stages or moderate light exposure is used. In addition to this layout of the TDI sensors are long thus operational amplifiers suffer from loading effects too. This limits the use of operational amplifiers in TDI accumulators. Thus there is a need to evolve the accumulator architectures in order to overcome above mentioned issues.

The TDI sensors are required in applications such as remote sensing and push broom

imaging. These applications require the operating image sensor to work with low power consumption. The prominent way to reduce the power budget is to reduce the supply voltage but it results in direct degradation of SNR. A reduced SNR nullifies the efforts made by TDI sensors. Thus trimming down on supply voltage is not a good choice for TDI sensors. The power consumption can also be reduced by trimming the operation of the power hungry column processing circuits but it results in reduced performance of column blocks such as CDS (Correlated double sampling), PGA (Programmable gain amplifiers) and ADCs (Analog to digital converter). All these blocks consume constant dc current and so are the biggest source of power consumption. TDI sensors accumulate output from all the stages so in addition to signal, noise gets added too. It results in dynamic range degradation. This also puts a limitation on number of TDI stages that can be used.

This thesis presents a solution to the saturation in the TDI sensors. A charge pump based accumulator combined with hybrid accumulation is proposed. To reduce the power consumption, a pulse width modulated (PWM) based pixel is proposed. The PWM is operated to achieve low power as well as high dynamic range. Two prototype sensors were fabricated and tested. The two prototype sensors are given below.

The prototype 1 presents an 8 stage, charge pump based analog accumulator for time delay integration CMOS image sensors. It addresses the accumulator saturation problem for higher TDI stages, overexposure and non linearity associated with integration based accumulators by using charge pump based accumulators. It introduces a novel solution to TDI saturation problem because of overexposure. A saturation prevention algorithm

has been presented that detects overexposure and stops the further integration of scene at the ADC level itself. A prototype chip of 128 x 8 TDI image sensor has been designed and fabricated in AMS 0.35  $\mu\text{m}$ , one-poly four-metal 3.3 V CMOS technology with a pixel pitch of 10  $\mu\text{m}$ . Measured SNR improvement for 8 stages is 10.6 dB. The measured dynamic range for 8 stage accumulation is 45 dB. Sensitivity for designed sensor has been measured to be 42.16 V/lux-s.

The prototype 2 addresses the power consumption and presents a low power consuming sensor. A 128 x 128 PWM based 4T pixel is designed and fabricated in TSMC 0.18  $\mu\text{m}$  one-poly six-metal (1P6M) 3.3/1.8 V CIS process. This pixel utilises a ramp to implement the slope ADC operation inside the pixel itself. The ADC conversion in the pixel allows for removing the power consuming circuits like PGA and ADC in the column. The ADC conversion in the pixel consumes much lower power compared to column ADC. Along with the low power operation, the dynamic range of the sensor is also enhanced by operating the pixel as 3T and using the discharge properties of the sensing node. A dynamic range of 100 dB is obtained in the measurement in a single-shot mode.

## सारांश

इमेजिंग अनुप्रयोगों में, जब सेंसर और वस्तु के बीच सापेक्ष गति होती है, तो फोटोडायोड को पर्याप्त फोटॉन एकत्र करने के लिए सीमित एकीकरण समय उपलब्ध होता है। पुशब्रूम इमेजिंग और मशीन विज्ञान अनुप्रयोगों में पहले से ही उपलब्ध फोटॉनों की संख्या बहुत कम होती है। कम संख्या में एकीकृत फोटॉन सिग्नल-टू-नॉइज़ अनुपात (SNR) को कम कर देते हैं, जिससे छवि की गुणवत्ता खराब होती है। टाइम डिले इंटीग्रेशन (TDI) एक प्रसिद्ध तकनीक है जो कई बार कैप्चरिंग करके सिग्नल स्तर को बढ़ाकर SNR को बेहतर बनाती है।

वर्तमान समय में बेहतर SNR प्राप्त करने के लिए TDI चरणों की संख्या बढ़ाने पर विशेष ध्यान दिया जा रहा है। हालांकि, TDI चरणों को बढ़ाने से एक दुष्प्रभाव भी होता है। पारंपरिक TDI सेंसर ADC से पहले एकीकृत सिग्नल को जोड़ते हैं, जिससे सिग्नल संतृप्ति (सैचुरेशन) के प्रति संवेदनशील हो जाता है। यह तब होता है जब दृश्य कम रोशनी से मध्यम रोशनी में बदलता है। इसके अलावा, पारंपरिक TDI सेंसर स्विचड कैपेसिटर इंटीग्रेटर आधारित एक्ज्युमुलेटर का उपयोग करते हैं, जो ऑपरेशनल एम्पलीफायर पर आधारित होते हैं। ये एम्पलीफायर आउटपुट वोल्टेज स्विंग में सीमित होते हैं और अधिक TDI चरणों या मध्यम प्रकाश में संतृप्त हो सकते हैं। लंबी लेआउट के कारण लोडिंग प्रभाव भी होता है, जिससे इनका उपयोग सीमित हो जाता है।

TDI सेंसर का उपयोग रिमोट सेंसिंग और पुश-ब्रूम इमेजिंग जैसे अनुप्रयोगों में किया जाता है। इन अनुप्रयोगों में इमेज सेंसर को कम पावर खपत के साथ कार्य करना होता है। पावर बजट को कम करने का प्रमुख तरीका सप्लाइ वोल्टेज को घटाना है, लेकिन इससे सीधे तौर पर सिग्नल-टू-नॉइज़ अनुपात (SNR) में गिरावट आती है। घटा हुआ SNR, TDI सेंसर द्वारा किए गए प्रयासों को निष्फल कर देता है। इसलिए सप्लाइ वोल्टेज को कम करना TDI सेंसर के लिए उपयुक्त विकल्प नहीं है।

पावर खपत को घटाने का एक और तरीका है कॉलम प्रोसेसिंग सर्किट्स के संचालन को सीमित करना, लेकिन इससे CDS (कोरिलेटेड डबल सैंपलिंग), PGA (प्रोग्रामेबल गेन एम्पलीफायर) और ADC (एनालॉग टू डिजिटल कन्वर्टर) जैसे कॉलम ब्लॉक्स के प्रदर्शन में कमी आती है। ये सभी ब्लॉक्स लगातार डीसी करंट का उपयोग करते हैं और पावर खपत के प्रमुख स्रोत होते हैं।

TDI सेंसर सभी चरणों से आउटपुट को एकत्र करते हैं, जिससे सिग्नल के साथ-साथ शोर भी जुड़ता है। इसका परिणाम डायनामिक रेंज में गिरावट के रूप में होता है। यह TDI चरणों की संख्या को सीमित करने का कारण भी बनता है।

इस शोध में TDI सेंसर में संतृप्ति की समस्या का समाधान प्रस्तुत किया गया है। एक चार्ज पंप आधारित एक्ज्युमुलेटर को हाइब्रिड एक्ज्युमुलेशन के साथ प्रस्तावित किया गया है। पावर खपत को कम करने के लिए एक पल्स विड्थ मॉड्युलेटेड (PWM) आधारित पिक्सल प्रस्तावित किया गया है। PWM को कम पावर और उच्च डायनामिक रेंज प्राप्त करने के लिए संचालित किया गया है।

दो प्रोटोटाइप सेंसर डिज़ाइन और परीक्षण किए गए हैं, जो नीचे दिए गए हैं।

प्रोटोटाइप 1 एक 8-स्टेज चार्ज पंप आधारित एनालॉग एक्ज्युमुलेटर प्रस्तुत करता है जो टाइम डिले इंटीग्रेशन (TDI) CMOS इमेज सेंसर के लिए डिज़ाइन किया गया है। यह उच्च TDI चरणों, अधिक

प्रकाश एक्सपोजर और इंटीग्रेशन आधारित एक्यूमुलेटर से जुड़ी नॉन-लिनियरिटी के कारण उत्पन्न होने वाली संतृप्ति (सैचुरेशन) की समस्या को हल करता है। इसमें एक नया समाधान प्रस्तुत किया गया है जो ओवरएक्सपोजर का पता लगाकर ADC स्तर पर दृश्य का आगे का इंटीग्रेशन रोक देता है।

- प्रोटोटाइप चिप:  $128 \times 8$  TDI इमेज सेंसर
- प्रौद्योगिकी: AMS  $0.35 \mu\text{m}$ , वन-पॉली फोर-मेटल  $3.3 \text{ V CMOS}$
- पिक्सल पिच:  $10 \mu\text{m}$
- SNR सुधार:  $10.6 \text{ dB}$  (8 स्टेज के लिए)
- डायनामिक रेंज:  $45 \text{ dB}$
- संवेदनशीलता:  $42.16 \text{ V/lux-s}$

प्रोटोटाइप 2 पावर खपत को संबोधित करता है और एक कम पावर खपत वाला सेंसर प्रस्तुत करता है। इसमें  $128 \times 128$  PWM आधारित 4T पिक्सल डिज़ाइन और TSMC  $0.18 \mu\text{m}$ , वन-पॉली सिक्स-मेटल (1P6M)  $3.3/1.8 \text{ V CIS}$  प्रक्रिया में निर्मित किया गया है। यह पिक्सल रैम्प सिग्नल का उपयोग करके स्लोप ADC ऑपरेशन को पिक्सल के अंदर ही लागू करता है।

- लाभ:
  - कॉलम में PGA और ADC जैसे पावर-हंग्री सर्किट को हटाया जा सकता है
  - इन-पिक्सल ADC कॉलम ADC की तुलना में बहुत कम पावर खपत करता है
  - पिक्सल को 3T मोड में चलाकर और सेंसिंग नोड के डिस्चार्ज गुणों का उपयोग करके डायनामिक रेंज को बढ़ाया गया है
- मापी गई डायनामिक रेंज:  $100 \text{ dB}$  (सिंगल-शॉट मोड में)

# Table of Contents

|   | <b>Page</b> |
|---|-------------|
| <b>List of Figures</b>                        | <b>xi</b>   |
| <b>List of Tables</b>                         | <b>xv</b>   |
| <b>Chapter 1 Introduction</b>                 | <b>1</b>    |
| 1.1 Motivation . . . . .                      | 1           |
| 1.2 Image sensor devices . . . . .            | 5           |
| 1.3 Basic imager performance matrix . . . . . | 10          |
| 1.3.1 Signal-to-noise ratio (SNR) . . . . .   | 10          |
| 1.3.2 Dynamic range . . . . .                 | 10          |
| 1.3.3 Fill factor (FF) . . . . .              | 10          |
| 1.3.4 Conversion gain (CG) . . . . .          | 11          |
| 1.3.5 Frame rate . . . . .                    | 11          |
| 1.4 Principle of TDI sensors . . . . .        | 11          |
| 1.5 Thesis motivation . . . . .               | 14          |

|   |   |           |
|---|---|-----------|
| 1.6   | Thesis organization . . . . .   | 16        |
| <b>Chapter 2 Literature review</b>  |   | <b>18</b> |
| 2.1   | Time delay integration (TDI) sensors . . . . .  | 18        |
| 2.1.1   | Pixel transfer based TDI sensors [1] . . . . .  | 19        |
| 2.1.2   | Time-Delay-Integration Architectures in CMOS Image Sensors [2]  | 21        |
| 2.1.3   | An Antivibration Time-Delay Integration CMOS Image Sensor With<br>Online Deblurring Algorithm [3] . . . . . | 21        |
| 2.1.4   | A 128-Stage Analog Accumulator for CMOS TDI Image Sensor [4]  | 22        |
| 2.2   | Low power image sensors . . . . .   | 23        |
| 2.2.1   | A 0.5 V PWM pixel-based CMOS image sensor [5] . . . . .   | 23        |
| 2.2.2   | Re-configurable ADC based image sensor for always-on operation<br>[6] . . . . .                             | 24        |
| 2.2.3   | Fully dynamic CMOS image sensor for always-on operation [7] . .   | 25        |
| 2.3   | Conclusions . . . . .   | 27        |
| <b>Chapter 3 A Charge Pump based Time Delay Integration Architecture for CMOS<br/>Image Sensors</b> |   | <b>29</b> |
| 3.1   | Introduction . . . . .  | 29        |
| 3.2   | TDI Architecture . . . . .  | 32        |
| 3.2.0.1   | Pixel . . . . .   | 35        |
| 3.2.0.2   | CDS PWM . . . . .   | 36        |

|                  |   |           |
|------------------|---|-----------|
| 3.2.0.3          | TDI cell . . . . .  | 37        |
| 3.2.0.4          | ADC . . . . .   | 39        |
| 3.2.1            | Comparison of charge pump accumulator with switched cap accumulator . . . . .                         | 48        |
| 3.3              | Measurement Results . . . . .   | 50        |
| 3.4              | Conclusion . . . . .  | 57        |
| <b>Chapter 4</b> | <b>A 4T PWM pixel-based CMOS image sensor</b>   | <b>61</b> |
| 4.1              | A 4T PWM based pixel . . . . .  | 62        |
| 4.1.1            | Design challenges in PWM based pixels . . . . .   | 67        |
| 4.1.1.1          | Non-linearity of the comparator . . . . .   | 67        |
| 4.1.1.2          | Noise analysis in PWM pixel . . . . .   | 69        |
| 4.1.2            | Power consumption analysis in PWM based sensors . . . . .   | 79        |
| 4.1.2.1          | Dynamic range extension in 4T PWM-based pixel . . . . .   | 82        |
| 4.2              | PWM based sensor architecture . . . . .   | 84        |
| 4.3              | Measurement results . . . . .   | 87        |
| 4.4              | Conclusion . . . . .  | 92        |
| <b>Chapter 5</b> | <b>Conclusions and Future Scope</b>   | <b>97</b> |
| 5.1              | Prototype 1: A Charge Pump based Time Delay Integration Architecture for CMOS Image Sensors . . . . . | 97        |
| 5.1.1            | Conclusion . . . . .  | 97        |

|       |   |            |
|-------|---|------------|
| 5.1.2 | Future directions . . . . .                                   | 98         |
| 5.2   | Prototype 2: A 4T PWM pixel-based CMOS image sensor . . . . . | 99         |
| 5.2.1 | Conclusion . . . . .  | 99         |
| 5.2.2 | Future directions . . . . .                                   | 100        |
|       | <b>Bibliography</b>   | <b>102</b> |

# List of Figures

|     |   |    |
|-----|---|----|
| 1.1 | TDI integration effect . . . . .  | 3  |
| 1.2 | CMOS image sensor general architecture . . . . .  | 5  |
| 1.3 | CMOS image sensor general architecture . . . . .  | 7  |
| 1.4 | 4T pixel readout architecture . . . . .   | 8  |
| 1.5 | 4T pixel readout timing diagram . . . . .   | 9  |
| 1.6 | Time delay integration architecture . . . . .   | 12 |
| 2.1 | A Time-Delay-Integration CMOS Image Sensor with Pipelined Charge Transfer Architecture [1] . . . . .      | 19 |
| 2.2 | Time-Delay-Integration Architectures in CMOS Image Sensors [2] . . . . .                                  | 20 |
| 2.3 | An Antivibration Time-Delay Integration CMOS Image Sensor With On-line Deblurring Algorithm [3] . . . . . | 21 |
| 2.4 | A 128-Stage Analog Accumulator for CMOS TDI Image Sensor [4] . . . . .                                    | 22 |
| 2.5 | TVC-based pixel and operational timing diagram [5] . . . . .  | 24 |
| 2.6 | Reconfigurable ADC in photo shooting mode and in always on mode [6] . . . . .                             | 25 |

|      |  |    |
|------|--|----|
| 2.7  | Dynamic 4T pixel readout . . . . .   | 26 |
| 3.1  | Time delay integration architecture . . . . .  | 30 |
| 3.2  | TDI architecture . . . . .   | 33 |
| 3.3  | TDI sensor 8 stage operation . . . . .   | 34 |
| 3.4  | TDI readout . . . . .  | 35 |
| 3.5  | TDI Sensor Architecture . . . . .  | 36 |
| 3.6  | Timing diagram for sensor . . . . .  | 37 |
| 3.7  | Timing diagram for charge pump operation . . . . .   | 39 |
| 3.8  | PWM and charge pump output . . . . .   | 40 |
| 3.9  | TDI CP noise model . . . . .   | 41 |
| 3.10 | Comparison of conventional accumulator and charge pump accumulator<br>(a)Low light exposure(b) High light exposure . . . . . | 44 |
| 3.11 | Digital output comparison of conventional accumulator and charge pump<br>accumulator . . . . .                               | 45 |
| 3.12 | (a) Measurement setup (b) Test setup . . . . .   | 46 |
| 3.13 | Microchip photograph of the sensor . . . . .   | 49 |
| 3.14 | Photon Transfer Curve (PTC) plot . . . . .   | 50 |
| 3.15 | Images captured from TDI stage (a) TDI stage 1 to 4 and (b) TDI stage 5<br>to 8. . . . .                                     | 52 |
| 3.16 | SNR boost plot . . . . .   | 53 |
| 3.17 | Proposed novel TDI saturation algorithm . . . . .  | 54 |

|      |   |    |
|------|---|----|
| 3.18 | Comparison of images with saturation algorithm (a)-(e) Image from row 1<br>to row 5 . . . . .                                       | 55 |
| 3.19 | Comparison of images with saturation algorithm (a)-(c) Image from row 6<br>to row 8 (d) Imager after saturation algorithm . . . . . | 55 |
| 3.20 | Histogram of sensor output (a)Row 0 (b)Row 8 (c)Row 8 with saturation<br>protection . . . . .                                       | 56 |
| 4.1  | A 4T PWM based pixel architecture . . . . .   | 63 |
| 4.2  | Pixel with column readout circuit . . . . .   | 65 |
| 4.3  | Timing diagram for pixel readout . . . . .  | 65 |
| 4.4  | Original transfer curve of pixel readout . . . . .  | 68 |
| 4.5  | Difference between the Ideal and Simulated transfer curve . . . . .   | 68 |
| 4.6  | Differential non-linearity . . . . .  | 69 |
| 4.7  | Integral non-linearity . . . . .  | 70 |
| 4.8  | Circuitual noise elements in pixel readout architecture . . . . .   | 72 |
| 4.9  | Timing diagram for digital double sampling (DDS) readout . . . . .  | 73 |
| 4.10 | Effect of noise on comparator output trigger time . . . . .   | 74 |
| 4.11 | Histogram for comparator output trigger time . . . . .  | 75 |
| 4.12 | Noise in RESET voltage read . . . . .   | 76 |
| 4.13 | Noise in SIGNAL voltage read . . . . .  | 77 |
| 4.14 | Noise post DDS correction . . . . .   | 78 |
| 4.15 | PPD device and potential profile across it for HDR mode . . . . .   | 82 |

|      |  |    |
|------|--|----|
| 4.16 | Timing diagram for pixel readout in HDR mode . . . . .         | 83 |
| 4.17 | Photo response for proposed pixel in HDR mode . . . . .        | 84 |
| 4.18 | A 4T PWM pixel-based low power CIS architecture . . . . .      | 85 |
| 4.19 | Layout of designed image sensor . . . . .                      | 88 |
| 4.20 | Fabricated sensor with PCB stack . . . . .                     | 89 |
| 4.21 | Measurement setup . . . . .                                    | 89 |
| 4.22 | Sensor output normal mode . . . . .                            | 90 |
| 4.23 | Sensor output HDR mode . . . . .                               | 91 |
| 4.24 | Sensor output HDR mode (Log) . . . . .                         | 92 |
| 4.25 | Sample images captured without dark pixel correction . . . . . | 93 |
| 4.26 | Sample images captured with dark pixel correction . . . . .    | 94 |
| 4.27 | HDR mode sample images (a) Normal mode (b) HDR mode . . . . .  | 94 |

# List of Tables

|     |   |    |
|-----|---|----|
| 3.1 | Sensor characteristics . . . . .                              | 51 |
| 3.2 | Sensitivity of TDI stages . . . . .                           | 51 |
| 3.3 | Comparison of TDI sensors . . . . .                           | 59 |
| 4.1 | Power calculation for the imager . . . . .                    | 81 |
| 4.2 | Sensor characteristics . . . . .                              | 93 |
| 4.3 | Comparison of this work with existing architectures . . . . . | 95 |