

AN AREA EFFICIENT AND HIGH SPEED READOUT FOR CMOS IMAGE SENSORS

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DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

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AN AREA EFFICIENT AND HIGH SPEED READOUT FOR CMOS IMAGE SENSORS

by

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DEPARTMENT OF ELECTRICAL ENGINEERING

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To my loving family

Certificate

This is to certify that the thesis entitled “**An area efficient and high speed readout for CMOS image sensors**”, being submitted by **Amandeep Kaur** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by her under my supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

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Abstract

Complementary metal oxide semiconductor (CMOS) image sensors have surpassed charge-coupled devices in many field of applications due to their low cost, low power consumption, miniaturization and feasibility to integrate electronics on chip. Due to technology scaling, CMOS image sensors (CIS) allow multiple transistors to be placed inside the pixels taking care of both signal information as well as signal processing. These pixels, therefore, allow CIS to operate as a global shutter in order to meet the requirements in high speed applications. In addition, the parallel data readout of multiple pixels makes it possible to design high speed cameras which are useful for applications like motion detection.

The speed of CIS is limited by the performance of analog to digital converter (ADC), which is a main element of readout circuit. The present work is, therefore, mainly focused on improving the readout speed of ADC. Readout electronics in an image sensor can be implemented at the chip-level, column-level or pixel-level. To achieve high speed and high resolution, column-level ADCs are preferred in the state-of-the-art image sensors as these architectures are best optimized in terms of speed and fill factor. In order to implement ADC in a column pitch of high resolution image sensors, its architecture needs to be area efficient. Slope ADC occupies minimum area, therefore is widely used as a column-parallel readout. A circuit level improvement in increasing the speed of slope ADC can be achieved by reducing the comparator latency. The present work describes three techniques: dynamic bias, recyclic approach and adaptive bias to reduce the latency of comparator. However in general, the speed of slope ADC is limited by its architecture, therefore these ADCs are not preferred for high resolution and high speed CIS. The better alternates to slope ADC are cyclic ADCs and hybrid ADCs.

To design a high speed and high resolution image sensor, this work presents a novel 2.5-bit/phase cyclic ADC wherein 1.5-bit algorithm is implemented in a 2.5-bit framework. A

redundant 2.5-bit stage reduces the total number of comparators to half as compared to the conventional 2.5-bit stage, therefore saves power. Further, to improve the speed, the ADC uses two multiplying digital to analog converters (MDAC) in a pipelined fashion. The ADC is designed and fabricated in UMC 180 nm CMOS technology. A 12-bit ADC results in a sampling rate of 1.1 MS/s, while consuming 650 μ W of total power. The ADC is also designed and fabricated in a column pitch of 5.6 μ m to understand the design issues of implementing ADC in column. To further increase the speed and reduce the power, a two-stage ADC with 2.5-bit architecture is designed, wherein the pipelined operation of two stages improves the conversion rate. Power reduction can be achieved by relaxing the design constraints on the second-stage. A two-stage ADC with 12-bit resolution is designed and fabricated in UMC 180 nm CMOS technology. Measurement results show the ADC conversion rate of 1.67 MS/s for 12-bit resolution.

Two MDACs used in the previous design improve the conversion rate at the cost of large column area. To reduce the column area, while maintaining the speed, a slew rate enhanced cyclic ADC with single MDAC is proposed. An additional saving in area is achieved by reusing the double sampling circuit for input folding operation of ADC in the successive conversion cycles. The ADC is designed as a column-parallel architecture of CIS. An area efficient and high speed CIS is designed and fabricated in AMS 350 nm CMOS OPTO process. The single-stage ADC designed in a column pitch of 9 μ m results in a sampling rate of 1.38 MS/s. A CIS with 96×64 pixel array processed by column parallel readout results in a frame rate greater than 5000 fps. A single ADC consumes 560 μ W of power and the total power consumed by CIS is 59.4 mW. As an extension to this work, a CIS with column-parallel hybrid ADC is designed and fabricated in AMS 350 nm CMOS OPTO process to reduce the readout power. The hybrid ADC consists of cyclic-SAR (successive approximation register) architecture. The

initial images obtained from combination of 6-bits cyclic and 6-bits SAR are included in this work.

Aforementioned techniques ignore the characteristics of input signal. Considering the fact that in natural images, neighboring pixels carry similar information, on-chip compression techniques are explored for further power reduction. Instead of reading all pixels which unnecessarily consume readout power, only one pixel from a group of pixels with similar characteristics is read. The discarded pixels are later reconstructed off-chip using bilinear interpolation. Further, two enhancement approaches are developed to improve the output image quality. The first approach is based on wavelet decomposition whereas the second approach uses a deep convolutional neural network. The on-chip compression circuit is designed and simulated in UMC 180 nm CMOS technology. For 70% compression, the proposed design results in about 33% power saving. However, off-chip compression is undesirable for integrated solutions. Therefore, to reconstruct the image on-chip, an on-chip interpolation circuit is designed and simulated in AMS 350 nm OPTO process. The proposed techniques are, therefore, suitable for area efficient and high speed CIS.

सार

पूरक धातु ऑक्साइड सेमीकंडक्टर (सीएमओएस) छवि संवेदकों ने अपनी कम लागत, कम बिजली की खपत, चिप पर इलेक्ट्रॉनिक्स को एकीकृत करने के लिए लघुकरण और व्यवहार्यता के कारण अनुप्रयोगों के कई क्षेत्रों में चार्ज-युग्मित उपकरणों को पार कर लिया है। टेक्नॉलॉजी स्केलिंग के कारण, सीएमओएस छवि संवेदक (सीआईएस) मल्टीपल ट्रांजिस्टर को सिग्नल की जानकारी के साथ-साथ सिग्नल प्रोसेसिंग का ख्याल रखते हुए पिक्सल के अंदर रखना संभव बनाते हैं। इसलिए, ये पिक्सल उच्च गति अनुप्रयोगों में आवश्यकताओं को पूरा करने के लिए सीआईएस को वैश्विक शटर के रूप में संचालित करने की अनुमति देते हैं। इसके अलावा, कई पिक्सल के समानांतर डेटा रीडआउट उच्च गति वाले कैमरों को डिजाइन करना संभव बनाता है जो गति का पता लगाने जैसे अनुप्रयोगों के लिए उपयोगी होते हैं।

सीआईएस की गति एनालॉग से डिजिटल कनवर्टर (एडीसी) के प्रदर्शन पर निर्भर है, जो रीडआउट सर्किट का एक मुख्य तत्व है। इसलिए, वर्तमान काम मुख्य रूप से एडीसी की रीडआउट गति में सुधार पर केंद्रित है। छवि संवेदक में रीडआउट इलेक्ट्रॉनिक्स को चिप-स्तर, कॉलम-स्तर या पिक्सल-स्तर पर लागू किया जा सकता है। उच्च गति और उच्च रिज़ॉल्यूशन प्राप्त करने के लिए, कॉलम-स्तरीय एडीसी को अत्याधुनिक छवि सेंसर में पसंद किया जाता है क्योंकि ये आर्किटेक्चर गति और भरण कारक के मामले में सबसे अधिक अनुकूलित होते हैं। उच्च रिज़ॉल्यूशन छवि संवेदक के एक कॉलम पिच में एडीसी को बनाने के लिए, इसकी रचना को क्षेत्र में कुशल बनाने की आवश्यकता

है। ढलान एडीसी न्यूनतम क्षेत्र लेता है, इसलिए व्यापक रूप से कॉलम-समानांतर रीडआउट के रूप में उपयोग किया जाता है। तुलनित्र विलंबता को कम करके एडीसी ढलान की गति बढ़ाने में सर्किट स्तर में सुधार किया जा सकता है। वर्तमान कार्य तीन तकनीकों का वर्णन करता है: डायनेमिक पूर्वाग्रह, पुनर्नवीनीकरण दृष्टिकोण और तुलनित्र की विलंबता को कम करने के लिए अनुकूली पूर्वाग्रह। हालांकि सामान्य तौर पर, ढलान एडीसी की गति इसकी रचना द्वारा सीमित है, इसलिए इन एडीसी को उच्च संकल्प और उच्च गति सीआईएस के लिए पसंद नहीं किया जाता है। ढलान एडीसी से बेहतर विकल्प चक्रीय एडीसी और हाइब्रिड एडीसी हैं।

एक उच्च गति और उच्च रिज़ॉल्यूशन वाली छवि संवेदक डिजाइन करने के लिए, यह काम एक नए 2.5-बिट / चरण चक्रीय एडीसी प्रस्तुत करता है जिसमें 1.5-बिट एल्गोरिथ्म 2.5-बिट फ्रेमवर्क में कार्यान्वित किया गया है। एक निरर्थक 2.5-बिट चरण पारंपरिक 2.5-बिट चरण की तुलना में कम्पैरेटर्स की कुल संख्या को आधा कर देता है, इसलिए बिजली की बचत होती है। इसके अलावा, गति में सुधार करने के लिए, एडीसी दो बहुध्रुवीय डिजिटल से एनालॉग कन्वर्टर्स (एमडीएसी) का उपयोग पाइपलाइन फैशन में करता है। एडीसी को यूएमसी 180 nm सीएमओएस तकनीक में डिज़ाइन और निर्मित किया गया है। एक 12-बिट एडीसी का परिणाम 1.1 ms / s के नमूने की दर से होता है, जबकि कुल बिजली का 650 μ W खपत होता है। एडीसी को स्तंभ में एडीसी को लागू करने के डिजाइन मुद्दों को समझने के लिए 5.6 μ m के एक कॉलम पिच में भी डिज़ाइन और निर्मित किया गया है। गति को और बढ़ाने और शक्ति को कम करने के लिए, 2.5-बिट आर्किटेक्चर के साथ एक दो-चरण एडीसी डिज़ाइन किया गया है, जिसमें दो चरणों के पाइपलाइन ऑपरेशन से, रूपांतरण दर में सुधार होता है। दूसरे चरण पर डिजाइन की बाधाओं को कम करके बिजली की कमी को प्राप्त किया जा सकता है। 12-बिट रिज़ॉल्यूशन वाला एक दो-चरण एडीसी यूएमसी 180 nm सीएमओएस तकनीक में डिज़ाइन और निर्मित किया गया है। माप परिणाम 12-बिट

रिज़ॉल्यूशन के लिए 1.67 MS / s की एडीसी रूपांतरण दर दिखाते हैं।

पिछले डिज़ाइन में उपयोग किए गए दो एमडीएसी बड़े कॉलम क्षेत्र की लागत पर रूपांतरण दर में सुधार करते हैं। कॉलम क्षेत्र को कम करने के लिए, गति को बनाए रखते हुए, एकल एमडीएसी के साथ एक विस्तारित दर चक्रीय एडीसी प्रस्तावित है। क्रमिक रूपांतरण चक्रों में एडीसी के इनपुट तह संचालन के लिए डबल सैंपलिंग सर्किट का पुनः उपयोग करके क्षेत्र में एक अतिरिक्त बचत प्राप्त की गई है। एडीसी को सीआईएस के कॉलम-समानांतर आर्किटेक्चर के रूप में डिज़ाइन किया गया है। एक क्षेत्र कुशल और उच्च गति सीआईएस को एएमएस 350 nm सीएमओएस OPTO प्रक्रिया में डिज़ाइन और निर्मित किया गया है। एकल चरण एडीसी को 9 μm के एक कॉलम पिच में डिज़ाइन किया गया है, जिसका परिणाम 1.38 MS / s की नमूना दर है। कॉलम के समानांतर रीडआउट परिणाम द्वारा संसाधित 96×64 पिक्सेल सरणी के साथ एक सीआईएस फ्रेम दर 5000 एफपीएस से अधिक है। एक एकल एडीसी में 560 μW बिजली की खपत होती है और सीआईएस द्वारा खपत की जाने वाली कुल बिजली 59.4 mW है। इस काम के विस्तार के रूप में, स्तंभ-समानांतर हाइब्रिड एडीसी के साथ एक सीआईएस रीडआउट शक्ति को कम करने के लिए एएमएस 350 nm सीएमओएस OPTO प्रक्रिया में डिज़ाइन और निर्मित किया गया है। हाइब्रिड एडीसी में चक्रीय-एसएआर (क्रमिक सन्निकटन रजिस्टर) रचना शामिल है। 6-बिट चक्रीय और 6-बिट एसएआर के संयोजन से प्राप्त प्रारंभिक छवियां इस काम में शामिल हैं।

उपरोक्त तकनीक इनपुट सिग्नल की विशेषताओं को अनदेखा करती है। इस तथ्य को ध्यान में रखते हुए कि प्राकृतिक छवियों में, पड़ोसी पिक्सेल समान जानकारी रखते हैं, आगे की बिजली कटौती के लिए ऑन-चिप संपीड़न तकनीकों का पता लगाया गया है। सभी पिक्सेल पढ़ने के बजाय जो अनावश्यक रूप से रीडआउट शक्ति का उपभोग करते हैं, समान विशेषताओं वाले पिक्सेल के समूह में से केवल एक पिक्सेल पढ़ा गया है। त्याग किए गए पिक्सेल बाद में बिलिनियर इंटरपोलेशन का उपयोग करते

हुए ऑफ-चिप का पुनर्निर्माण किया गया है। इसके अलावा, आउटपुट इमेज क्वालिटी को बेहतर बनाने के लिए दो एन्हांसमेंट एप्रोच विकसित किए गए हैं। पहला दृष्टिकोण तरंगिका अपघटन पर आधारित है जबकि दूसरा दृष्टिकोण एक डीप लर्निंग नेटवर्क का उपयोग करता है। ऑन-चिप संपीड़न सर्किट को यूएमसी 180 nm सीएमओएस तकनीक में डिज़ाइन और अनुकरण किया गया है। 70% संपीड़न के लिए, प्रस्तावित डिज़ाइन के परिणामस्वरूप लगभग 33% बिजली की बचत होती है। हालांकि, एकीकृत समाधान के लिए ऑफ-चिप संपीड़न अवांछनीय है। इसलिए, छवि को चिप में फिर से संगठित करने के लिए, एक चिप पर प्रक्षेप सर्किट को एएमएस 350 nm OPTO प्रक्रिया में डिज़ाइन और अनुकरण किया गया है। इसलिए, प्रस्तावित तकनीकें क्षेत्र कुशल और उच्च गति सीआईएस के लिए उपयुक्त हैं।

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List of Abbreviations

ADC	Analog to digital converter
A/D	Analog to digital
APS	Active pixel sensor
CA	Cascode amplifier
CDS	Correlated double sampling
CF	Compression factor
CIS	CMOS image sensor
CMOS	Complementary metal oxide semiconductor
CNN	Convolutional neural network
CS	Compressive sensing
DAC	Digital to analog converter
DAQ	Data acquisition
D/A	Digital to analog
DEC	Digital error correction
DS	Double sampling
DDS	Delta double sampling
DL	Detection logic
DNL	Differential non-linearity

DUT	Device under test
ENoB	Effective number of bits
IG	Interstage gain
INL	Integral non-linearity
FFT	Fast Fourier transform
FoM	Figure of merit
FPN	Fixed pattern noise
FCNN	Fully convolutional neural network
LDO	Low dropout regulator
LSB	Least significant bit
MDAC	Multiplying Digital to analog converter
MDEC	Modified digital error correction
MSB	Most significant bit
NNI	Natural neighbour interpolation
PCB	Printed circuit board
PRI	Pixel read/interpolate
PSNR	Peak signal to noise ratio
RB	Redundant binary
SAR	Successive approximation register
SC	Switched capacitor
SPD	Superpixel detection
SPD_C	Column-level superpixel detection
SPD_R	Row-level superpixel detection
S/H	Sample and hold

SNR	Signal to noise ratio
SNDR	Signal to noise and distortion ratio
SR	Set-reset
SRE	Slew rate enhancement
SSIM	Structural similarity index measure
VFPN	Vertical fixed pattern noise