EVOLUTION OF QUADRATIC FOLLOWING BOOST TOPOLOGIES AND ROBUST CONTROLLER DESIGN: A PARAMETER SPACE APPROACH

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by

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CERTIFICATE

This is to certify that the thesis entitled **"Evolution Of Quadratic Following Boost Topologies And Robust Controller Design: A Parameter Space Approach"** is being submitted by **Mr. Nikhil Kumar** in fulfillment of the requirements for the degree of **Doctor of Philosophy** in the Department Electrical Engineering of Indian Institute of Technology Delhi, New Delhi.

Mr. Nikhil Kumar has worked under my supervision and fulfilled the requirement for submission of the thesis, which to my knowledge reached the requisite standards. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any Degree or Diploma.

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ABSTRACT

Two quadratic following boost converter (QFBC) topologies are evolved with voltage gain trend following the conventional quadratic boost converter (QBC). Both these topologies are capable of realizing high voltage gain at trade-off duty ratios. Detailed mathematical analysis is established to bring out salient features of the proposed QFBC topologies. Both these topologies have similarity as their gain variation closely follows the conventional quadratic boost converter. The QFBC Type-1 topology gain is slightly lower than the conventional quadratic boost converter while QFBC Type-2 exhibits a little higher gain. QFBC Type-1 has lesser voltage gain sensitivity and control complexity than traditional QBC whereas QFBC Type-2 has lesser capacitor voltage stress than the conventional QBC. Quadratic following voltage gain features and other steady-state performance aspects of the proposed topologies are verified through experimental investigations. Detailed state-space analysis is established for both the QFBC topologies and control-to-output plant along with other transfer functions are formulated. Subsequently, these transfer functions are used as plant models to design the robust controllers.

After topological evolutions, suitable controller selection and design aspects to achieve load voltage regulation are investigated. Closed-loop stabilization of the proposed topologies is carried out using the single-loop and double-loop voltage-mode control strategies. In case of single-loop voltage-mode control, a proportional plus integral plus derivative (PID) controller structure is adopted. Proportional plus integral (PI), proportional plus derivative (PD) controller combinations are adopted for the double-loop voltage-mode control scheme. These controllers are designed such that the proposed QFBC topologies reliably operates while delivering the desired voltage boosting ratios. To achieve this, the designed single-loop as well as double-loop controller configurations must be ensure robustness and performance specifications. In this context, firstly stabilizing region for the controller parameters is generated using stability boundary locus approach. Thereafter, controller parameter region is squeezed by adding (i) Kharitonov polynomials based constraints to handle the plant uncertainties and (ii) relative stability performance quantification constraints: gain margin and phase margin. Final controller parameters are chosen from this region based on minimum integral error index and for PID controller it is inversely proportional to the maximum value of the integral constant.

It is easy to deal with parameter uncertainty using Kharitonov polynomials but the resultant controller parameter stabilizing region is conservative and hence controller performance may not be guaranteed. Moreover, for the QFBC topologies (which are non-minimum phase systems) it is difficult to achieve desired performance and robustness range using single-loop voltage-mode control scheme alone. In an attempt to enhance the performance and robustness aspects of the proposed QFBC topologies, a double-loop voltage-mode control strategy is proposed in this thesis. Though this double-loop controller works by using load voltage information only and yet its performance is close to two-loop control scheme (i.e. inner current-loop and outer voltage-loop). On the basis of parameter-space approach, firstly the stabilizing regions in the controller parameter plane are generated. Thereafter, these stabilizing regions are squeezed upon enforcement of robustness and performance related constraints which are: (i) absolute stability criterion, (ii) the guaranteed combined sensitivity and (iii) guaranteed up-down glitch margin. From this region, the final robust controller parameters are chosen based on 'fmincon' solver based constrained optimization. Integral time square error (ITSE) performance index is used for optimization. Though this controller is sufficiently robust but there is no guarantee that it ensures performance quantification such as settling time and overshoot. With performance realization being the prime consideration, generation of double-loop voltage-mode controller parameter stabilizing region which ensures guaranteed dominant pole region is investigated. Like in single-loop voltage-mode controller, here also ITSE performance index along with constrained optimization is used to obtain the final controller which ensures settling time and overshoot requirement. The efficacy of single-loop and double-loop controllers for closed-loop stabilization of quadratic following boost converter topologies are verified experimentally. Controllers effectiveness in terms of load voltage regulation, disturbance rejection, reference tracking, ensuring settling time and overshoot requirements are also demonstrated experimentally. Also to highlight double-loop voltage-mode controller performance improvement, dynamic responses are compared and illustrated with the PID controller dynamic performance characteristics.

सारांश

पारंपरिक द्विघात बूस्ट कन्वर्टर (QBC) के बाद वोल्टेज गेन ट्रेंड के साथ दो द्विघात निम्नलिखित बूस्ट कन्वर्टर (QFBC) टोपोलॉजी विकसित किए गए हैं। ये दोनों टोपोलॉजी ट्रेड-ऑफ ड्यूटी अनुपात पर उच्च वोल्टेज लाभ प्राप्त करने में सक्षम हैं। प्रस्तावित QFBC टोपोलॉजी की मुख्य विशेषताओं को सामने लाने के लिए विस्तृत गणितीय विश्लेषण स्थापित किया गया है। इन दोनों टोपोलॉजी में समानता है क्योंकि उनके लाभ भिन्नता पारंपरिक द्विघात बूस्ट कनवर्टर का बारीकी से अनुसरण करते हैं। QFBC टाइप-1 टोपोलॉजी लाभ पारंपरिक द्विघात बूस्ट कनवर्टर की तुलना में थोड़ा कम है जबकि QFBC टाइप-2 थोड़ा अधिक लाभ प्रदर्शित करता है। QFBC टाइप -1 में पारंपरिक QBC की तुलना में कम वोल्टेज लाभ संवेदनशीलता और नियंत्रण जटिलता है जबकि QFBC टाइप -2 में पारंपरिक QBC की तुलना में कम कैपेसिटर वोल्टेज तनाव है। प्रस्तावित टोपोलॉजी के द्विघात निम्नलिखित वोल्टेज लाभ सुविधाओं और अन्य स्थिर-राज्य प्रदर्शन पहलुओं को प्रयोगात्मक जांच के माध्यम से सत्यापित किया जाता है। QFBC टोपोलॉजी दोनों के लिए विस्तृत राज्य-अंतरिक्ष विश्लेषण स्थापित किया गया है और अन्य हस्तांतरण कार्यों के साथ-साथ नियंत्रण-से-आउटपुट संयंत्र तैयार किए गए हैं। इसके बाद, इन स्थानांतरण कार्यों को मजबूत नियंत्रकों को डिजाइन करने के लिए संयंत्र मॉडल के रूप में उपयोग किया जाता है।

टोपोलॉजिकल विकास के बाद, लोड वोल्टेज विनियमन को प्राप्त करने के लिए उपयुक्त नियंत्रक चयन और डिजाइन पहलुओं की जांच की जाती है। प्रस्तावित टोपोलॉजी का क्लोज्ड-लूप स्थिरीकरण सिंगल-लूप और डबल-लूप वोल्टेज-मोड नियंत्रण रणनीतियों का उपयोग करके किया जाता है। सिंगल-लूप वोल्टेज-मोड नियंत्रण के मामले में, आनुपातिक प्लस इंटीग्रल प्लस डेरिवेटिव (पीआईडी) नियंत्रक संरचना को अपनाया जाता है। आनुपातिक प्लस इंटीग्रल (पीआई), आनुपातिक प्लस व्युत्पन्न (पीडी) नियंत्रक संयोजन डबल-लूप वोल्टेज-मोड नियंत्रण योजना के लिए अपनाया जाता है। इन नियंत्रकों को इस तरह डिज़ाइन किया गया है कि प्रस्तावित क्यूएफबीसी टोपोलॉजी वांछित वोल्टेज बूस्टिंग अनुपात प्रदान करते समय विश्वसनीय रूप से संचालित होती है। इसे प्राप्त करने के लिए, डिज़ाइन किए गए सिंगल-लूप के साथ-साथ डबल-लूप कंट्रोलर कॉन्फ़िगरेशन को मजबूती और प्रदर्शन विनिर्देशों को सुनिश्चित करना चाहिए। इस संदर्भ में, नियंत्रक मापदंडों के लिए सबसे पहले क्षेत्र को स्थिर करने के लिए स्थिरता सीमा स्थान दृष्टिकोण का उपयोग करके उत्पन्न किया जाता है। इसके बाद, नियंत्रक पैरामीटर क्षेत्र को (i) खारितोनोव बहुपद आधारित बाधाओं को संयंत्र अनिश्चितताओं से निपटने के लिए जोड़कर निचोड़ा जाता है और (ii) सापेक्ष स्थिरता प्रदर्शन परिमाणीकरण बाधाएं: लाभ मार्जिन और चरण मार्जिन। अंतिम नियंत्रक पैरामीटर इस क्षेत्र से न्यूनतम अभिन्न त्रुटि सूचकांक के आधार पर चुने जाते हैं और पीआईडी नियंत्रक के लिए यह अभिन्न स्थिरांक के अधिकतम मूल्य के व्युत्क्रमानुपाती होता है।

खारिटोनोव बहुपदों का उपयोग करके पैरामीटर अनिश्चितता से निपटना आसान है लेकिन परिणामी नियंत्रक पैरामीटर स्थिरीकरण क्षेत्र रूढ़िवादी है और इसलिए नियंत्रक प्रदर्शन की गारंटी नहीं हो सकती है। इसके अलावा, क्यूएफबीसी टोपोलॉजी (जो गैर-न्यूनतम चरण प्रणाली हैं) के लिए अकेले सिंगल-लूप वोल्टेज-मोड नियंत्रण योजना का उपयोग करके वांछित प्रदर्शन और मजबूती रेंज हासिल करना मुश्किल है। प्रस्तावित क्यूएफबीसी टोपोलॉजी के प्रदर्शन और मजबूती के पहलुओं को बढ़ाने के प्रयास में, इस थीसिस में एक डबल-लूप वोल्टेज-मोड नियंत्रण रणनीति प्रस्तावित है। यद्यपि यह डबल-लूप नियंत्रक केवल लोड वोल्टेज जानकारी का उपयोग करके काम करता है और फिर भी इसका प्रदर्शन दो-लूप नियंत्रण

योजना (यानी आंतरिक वर्तमान-लूप और बाहरी वोल्टेज-लूप) के करीब है। पैरामीटर-स्पेस दृष्टिकोण के आधार पर, सबसे पहले नियंत्रक पैरामीटर विमान में स्थिर क्षेत्र उत्पन्न होते हैं। इसके बाद, इन स्थिर क्षेत्रों को मजबूती और प्रदर्शन संबंधी बाधाओं को लागू करने पर निचोड़ा जाता है जो हैं: (i) पूर्ण स्थिरता मानदंड, (ii) गारंटीकृत संयुक्त संवेदनशीलता और (iii) गारंटीकृत अप-डाउन ग्लिच मार्जिन। इस क्षेत्र से, अंतिम मजबूत नियंत्रक मापदंडों को 'fmincon' सॉल्वर आधारित विवश अनुकूलन के आधार पर चुना जाता है। इंटीग्रल टाइम स्क्वेयर एरर (ITSE) परफॉर्मेंस इंडेक्स का इस्तेमाल ऑप्टिमाइजेशन के लिए किया जाता है। हालांकि यह नियंत्रक पर्याप्त रूप से मजबूत है लेकिन इस बात की कोई गारंटी नहीं है कि यह समय और ओवरशूट को व्यवस्थित करने जैसे प्रदर्शन मात्रा का ठहराव सुनिश्चित करता है। प्रदर्शन प्राप्ति प्रमुख विचार होने के साथ, डबल-लूप वोल्टेज-मोड नियंत्रक पैरामीटर स्थिरीकरण क्षेत्र की पीढ़ी जो गारंटीकृत प्रमुख ध्रुव क्षेत्र सुनिश्चित करता है, की जांच की जाती है। सिंगल-लूप वोल्टेज-मोड कंट्रोलर की तरह, यहां भी आईटीएसई परफॉर्मेंस इंडेक्स के साथ-साथ विवश अनुकूलन का उपयोग अंतिम नियंत्रक को प्राप्त करने के लिए किया जाता है जो समय और ओवरशूट की आवश्यकता को सुनिश्चित करता है। बूस्ट कन्वर्टर टोपोलॉजी के बाद द्विघात के बंद-लूप स्थिरीकरण के लिए सिंगल-लूप और डबल-लूप नियंत्रकों की प्रभावकारिता को प्रयोगात्मक रूप से सत्यापित किया गया है। लोड वोल्टेज विनियमन, गड़बड़ी अस्वीकृति, संदर्भ ट्रैकिंग, निपटान समय सुनिश्चित करने और ओवरशूट आवश्यकताओं के संदर्भ में नियंत्रक प्रभावशीलता भी प्रयोगात्मक रूप से प्रदर्शित की जाती है। इसके अलावा डबल-लूप वोल्टेज-मोड नियंत्रक प्रदर्शन सुधार को उजागर करने के लिए, गतिशील प्रतिक्रियाओं की तुलना की जाती है और पीआईडी नियंत्रक गतिशील प्रदर्शन विशेषताओं के साथ चित्रित किया जाता है।

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LIST OF SYMBOLS

Symbol	**Description**
D	Duty-ratio
D_1	Diode D_1
D_2	Diode D_2
D_3	Diode D_3
L_1	Inductor L_1
L_2	Inductor L_2
S_1	Switch S_1
S_2	Switch S_2
C_1	Capacitor C_1
C_2	Capacitor C_2
C_3	Capacitor C_3
r_{L1}	ESL of inductor L_1
r_{L2}	ESL of inductor L_2
r_{c1}	ESR of capacitor C_1
r_{c2}	ESR of capacitor C_2
r_{c3}	ESR of capacitor C_3
i_o	Load current
v_o	Load voltage
T_s	Time period
V_g	Source voltage
v_{c1}	Voltage across capacitor C_1
v_{c2}	Voltage across capacitor C_2
v_{c3}	Voltage across capacitor C_3
v_{L1}	Voltage across inductor L_1
v_{L2}	Voltage across inductor L_2
i_{L1}	Current through inductor L_1
i_{L2}	Current through inductor L_2
v_{D1}	Voltage across diode D_1
v_{D2}	Voltage across diode D_2
v_{S1}	Voltage across switch S_1
v_{S2}	Voltage across switch S_2
M	Voltage gain
I_{L1}	Average value of inductor L_1
I_{L2}	Average value of inductor L_2
i_{11}	Peak value of inductor L_1 current
i_{12}	Valley value of inductor L_1 current
i_{21}	Peak value of inductor L_2 current
i_{22}	Valley value of inductor L_2 current
I_g	Average value of source current
i_g	Instantaneous value of source current
i_{g1}	Valley value of source current
i_{g2}	Peak value of source current

Δi_{L1}	Ripple current of inductor L_1
Δi_{L2}	Ripple current of inductor L_2
Δv_{C1}	Ripple voltage of capacitor C_1
Δv_{C2}	Ripple voltage of capacitor C_2
R	Load resistance
A	System matrix
B	Input matrix
E	Output matrix
F	Feed-through matrix
u	Input/control vector
x	State vector
y	Output
$\hat{x}$	Small-signal variation in input
$\hat{y}$	Small-signal variation in output
W	Watts
P_o	Load power
G_{vd}	Control-to-output transfer function
G_P	Plant transfer function
G_{vg}	Output-to-input voltage transfer function
G_{vi}	Output-to-load disturbance transfer function
$\hat{d}$	Perturbation in duty-ratio
$\hat{v}_g$	Perturbation in source voltage
$\hat{i}_o$	Perturbation in load current
V_{ref}	Reference voltage
G_c	Controller transfer function
$\hat{v}_o$	Perturbation in load voltage
$\hat{e}$	Perturbation in error signal
$\hat{v}_{ref}$	Perturbation in reference voltage
Z_{out}	Load impedance
L_g	Loopgain of the system
G_{vr}	Closed-loop system transfer function
ω	Frequency (rad/s)
$Ae^{-j\theta}$	Gain margin phase margin transfer function
G_{c1}	Controller first part
G_{c2}	Controller second part
$G(s)$	Plant transfer function
R_p	Real part of transfer function
I_p	Imaginary part of transfer function
L_p	Loopgain
GK_{ij}	Kharitonov plant
$FI_{\Delta 20}$	Robustness-Fragility index
M_{SO}	Peak value of sensitivity function for nominal controller

$M_{S\Delta 20M}$	Peak value of sensitivity function for ±20 % change in the component values of the controller
G_{PWM}	PWM modulator transfer function
V_{PK}	Peak-to-peak voltage of saw-tooth
k_1	PI controller coefficient
k_2	PI controller coefficient
M_s	Peak value of sensitivity (S)
M_t	Complementary sensitivity (T)
S_o	Nominal sensitivity
S_Δ	Sensitivity under parameter variation
CR1,2,3	Controller-1,2,3
CP	PID type controller
FR	Final robust stabilizing region
G_{CQBFC1}	Controller of QFBC Type-1
k_p	Proportional constant
k_i	Integral constant
k_d	Derivative constant
G_{CPI}	PI controller transfer function
G_{CPD}	PD controller transfer function
L_{p1}	Transmittance of loop-1
L_{p2}	Transmittance of loop-2
L_{pt1}	Transmittance of forward path-1
L_{pt2}	Transmittance of forward path-2
G_p	Plant transfer function
P_t	Path transmittance
v_{oref}	Load voltage reference
Δ_{Pt}	Determinant obtained with non-touching loops
Δ	Determinant of the signal flow graph
G_{PPD}	Augmented plant transfer function
C_{tr}	Centre of circle
R_d	Radius of circle
δ	Distance of up-down glitch in the absolute scale
ω,ω_p	Frequency
Γ_{FR}	Final robust controller parameter region
Γ_{AS}	Absolute stability region
Γ_{CS}	Guaranteed combined sensitivity region
Γ_{UM}	Guaranteed up-down glitch margin region
G_{out}	Output impedance
G_{in}	Input impedance
G_{co}	Outer loop compensators
G_{cin}	Inner loop compensators
G_{PIN}	Augmented plant TF
σ	Real part of equation $s=(\sigma+j\omega)$