CHARACTERIZATION STUDIES OF 4T PIXEL FOR DYNAMIC PPD CAPACITANCE AND BARRIER MODULATION IN CMOS IMAGE SENSORS

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INDIAN INSTITUTE OF TECHNOLOGY DELHI

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by

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Dedicated to my family

Certificate

This is to certify that the thesis entitled **"Characterization studies of 4T pixel for dynamic PPD capacitance and barrier modulation in CMOS image sensors"**, submitted by **Ms. Uzma Khan** to the Indian Institute of Technology Delhi, for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of the original, bona-fide research work carried out by her under my supervision and guidance. The results contained in this thesis have not been submitted in part or in full to any other University or Institute for the award of any degree or diploma to the best of my knowledge.

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Abstract

The continuous scaling down of semiconductor technology has helped achieve low-power and low-cost image sensors. The reduction in pixel pitch has improved the resolution of the image sensors. However, the reduction in the pixel pitch due to technology scaling has made it difficult to achieve high full well capacity (FWC) and high dynamic range while maintaining high resolution. Achieving high sensitivity and high resolution while maintaining high dynamic range requires accurate and efficient estimation of the FWC of a four transistor (4T) pixel in a CMOS image sensor (CIS). The FWC of a 4T pixel depends on the pinned photodiode (PPD) capacitance, pinning voltage, potential barrier, temperature, and operating voltages. Thus, it is inevitable to understand and model the fundamental characteristics of a 4T pixel in a CIS. The thesis primarily focuses on the simulation and characterization based studies of 4T pixels for dynamic PPD capacitance and barrier modulation in CIS. In this thesis, an analytical model for the PPD capacitance is derived. The proposed model relies on the total current flowing through the PPD in low and high illumination conditions. The proposed model is further elaborated due to barrier modulation observed in the transfer gate (TG) channel at the PPD-TG interface in the absence and presence of a potential pocket. Understanding the potential changes in PPD, PPD-TG interface, and TG channel as a function of integrated PPD charges is a complex problem and needs a detailed analysis. The model is evaluated for light intensity, integration time, temperature, and transfer gate voltage values. The model is validated with technology computer-aided design (TCAD) simulations. The PPD capacitance model is validated experimentally by estimating the feedforward charges at the floating diffusion node, collected due to thermionic emission current. The non-linearity observed in the feedforward voltage is also explained using the non-linear behavior of TG channel potential. The non-linear behavior of TG channel potential influences the effective potential barrier, thereby influencing the FWC and PPD capacitance. Further, the barrier modulation study is extended by discussing the influence of interface traps in the charge transfer path. The interface traps influence the potential barrier differently when PPD is in the dark than when illuminated. The study will help better understand FWC, feedforward charges, and dark current generation mechanisms in a PPD. The results presented in the thesis can be a resource for CIS pixel designers to analyze, simulate, and optimize a 4T pixel.

Keywords: CMOS Image Sensors (CIS), Pinned Photodiode (PPD), Full Well Capacity (FWC), Feedforward effect, Photodiode capacitance, Analytical modeling, Potential barrier, Barrier modulation, Charge Transfer Potential Barrier (CTPB), interface traps.

सार

सेमीकंडक्टर प्रौद्योगिकी के निरंतर विस्तार से कम बिजली की खपत और कम लागत वाले छवि सेंसर प्राप्त करने में मदद मिली है। पिक्सेल पिच में कमी से छवि सेंसर के रिज़ॉल्यूशन में सुधार हुआ है। हालाँकि, प्रौद्योगिकी स्केलिंग के कारण पिक्सेल पिच में कमी ने उच्च रिज़ॉल्यूशन को बनाए रखते हुए उच्च पूर्ण क्षमता (एफडब्ल्यूसी) और उच्च गतिशील रेंज हासिल करना मुश्किल बना दिया है। उच्च गतिशील रेंज को बनाए रखते हुए उच्च संवेदनशीलता और उच्च रिज़ॉल्यूशन प्राप्त करने के लिए सीएमओएस इमेज सेंसर (सीआईएस) में चार ट्रांजिस्टर (4T) पिक्सेल के एफडब्ल्यूसी के सटीक और कुशल अनुमान की आवश्यकता होती है। 4T पिक्सेल का फडब्ल्यूसी पिन किए गए फोटोडायोड (पीपीडी) कैपेसिटेंस, पिनिंग वोल्टेज, संभावित अवरोध, तापमान और ऑपरेटिंग वोल्टेज पर निर्भर करता है। इस प्रकार, सीआईएस में 4T पिक्सेल की मूलभूत विशेषताओं को समझना और मॉडल करना अपरिहार्य है। थीसिस मुख्य रूप से सीआईएस में गतिशील पीपीडी कैपेसिटेंस और बैरियर मॉड्यूलेशन के लिए 4T पिक्सल के सिमुलेशन और लक्षण वर्णन-आधारित अध्ययन पर केंद्रित है। इस थीसिस में, पीपीडी कैपेसिटेंस के लिए एक विश्लेषणात्मक मॉडल प्राप्त किया गया है। प्रस्तावित मॉडल कम और उच्च रोशनी की स्थिति में पीपीडी के माध्यम से बहने वाली कुल धारा पर निर्भर करता है। संभावित पॉकेट की अनुपस्थिति और उपस्थिति में पीपीडी-टीजी इंटरफेस पर ट्रांसफर गेट (टीजी) चैनल में देखे गए बैरियर मॉड्यूलेशन के कारण प्रस्तावित मॉडल को और अधिक विस्तृत किया गया है। एकीकृत पीपीडी शुल्कों के कार्य के रूप में पीपीडी, पीपीडी-टीजी इंटरफ़ेस और टीजी चैनल में संभावित परिवर्तनों को समझना एक जटिल समस्या है और इसके विस्तृत विश्लेषण की आवश्यकता है। मॉडल का मूल्यांकन प्रकाश की तीव्रता, एकीकरण समय, तापमान और ट्रांसफर गेट वोल्टेज मानों के लिए किया जाता है। मॉडल को प्रौद्योगिकी कंप्यूटर-एडेड डिज़ाइन (टीसीएडी) सिमुलेशन के साथ मान्य किया गया है। पीपीडी कैपेसिटेंस मॉडल को थर्मोनिक उत्सर्जन धारा के कारण एकत्र किए गए फ्लोटिंग डिफ्यूजन नोड पर फीडफॉरवर्ड चार्ज का अनुमान लगाकर प्रयोगात्मक रूप से मान्य किया गया है। फीडफॉरवर्ड वोल्टेज में देखी गई गैर-रैखिकता को टीजी चैनल क्षमता के गैर-रैखिक व्यवहार का उपयोग करके भी समझाया गया है। टीजी चैनल क्षमता का गैर-रैखिक व्यवहार प्रभावी संभावित अवरोध को प्रभावित करता है, जिससे एफडब्ल्यूसी और पीपीडी कैपेसिटेंस प्रभावित होता है। इसके अलावा, चार्ज ट्रांसफर पथ में इंटरफ़ेस ट्रैप के प्रभाव पर चर्चा करके बैरियर मॉड्यूलेशन अध्ययन को बढ़ाया गया है। इंटरफ़ेस जाल संभावित अवरोध को अलग तरह से प्रभावित करते हैं जब पीपीडी रोशनी की तुलना में अंधेरे में होता है। अध्ययन से पीपीडी में एफडब्ल्यूसी, फीडफॉरवर्ड चार्ज और डार्क करंट जेनरेशन तंत्र को बेहतर ढंग से समझने में मदद मिलेगी। थीसिस में प्रस्तुत परिणाम सीआईएस पिक्सेल डिजाइनरों के लिए 4T पिक्सेल का विश्लेषण, अनुकरण और अनुकूलन करने के लिए एक संसाधन हो सकते हैं।

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Abbreviations

3T	**3** **T**ransistor
4T	**4** **T**ransistor
ADC	**A**nalog **D**igital **C**onverter
APS	**A**ctive **P**ixel **S**ensor
BBD	**B**ucket **B**rigade **D**evice
BSI	**B**ack **S**ide **I**lluminated
CCD	**C**harge **C**oupled **D**evice
CDS	**C**orrelated **D**ouble **S**ampling
CIS	**C**MOS **I**mage **S**ensor
CMOS	**C**omplimentary **M**etal **O**xide **S**emiconductor
CRA	**C**hief **R**ay **A**ngle
CTPB	**C**harge **T**ransfer **P**otential **B**arrier
CVF	**C**harge **V**oltage **F**actor
DIBL	**D**rain **I**nduced **B**arrier **L**owering
DN	**D**igital **N**umber
DR	**D**ynamic **R**ange
DTI	**D**eep **T**rench **I**solation
EFWC	**E**quilibrium **F**ull **W**ell **C**apacity
FB	**F**orward **B**ias
FD	**F**loating **D**iffusion
FSI	**F**ront **S**ide **I**lluminated
FWC	**F**ull **W**ell **C**apacity
ILT	**I**nter **L**ine **T**ransfer
MOS	**M**etal **O**xide **S**emiconductor
MOSFET	**M**etal **O**xide **S**emiconductor **F**eild **E**ffect **T**ransistor
PD	**P**hoto **D**iode

PPD	**P**inned **P**hoto **D**iode
PPS	**P**assive **P**ixel **S**ensor
QE	**Q**unantum **E**fficiency
QV	**Q**(charge) **V**oltage
RB	**R**everse **B**ias
RS	**R**ow **S**elect
RST	**R**eset
SF	**S**ource **F**ollower
SNR	**S**ignal **N**oise **R**atio
STI	**S**hallow **T**rench **I**solation
T	**T**emperature
TG	**T**ransfer **G**ate

Symbols

α	Absorption coefficient
A_{PPD}	Cross-sectional area of PPD
C_1	Parallel plate capacitance of $\mathrm{p}^+ - \mathrm{n}_{\mathrm{well}}$ region in PPD
C_2	Parallel plate capacitance of $\mathrm{n}_{\mathrm{well}} - \mathrm{p}_{\mathrm{epi}}$ region in PPD
C_{DEP}	Depletion capacitance
C_{DEP_0}	Depletion capacitance at equilibrium
C_{diff}	Diffusion capacitance
C_{PPD}	Pinned photodiode capacitance
C_{var}	Variable capacitance
δ_z	Distance traveled by incident light inside semiconductor
e^-	Electron
ϵ_0	Permittivity of free space
ϵ_r	Relative permittivity of silicon
E_1	Electric field from $\mathrm{n}_{\mathrm{well}}$ to p^+ region of PPD
E_2	Electric field from $\mathrm{n}_{\mathrm{well}}$ to p_{epi} region of PPD
E_{cn}	Conduction band energy of n region
E_{cp^+}	Conduction band energy of p^+ region
E_{Fn}	Electron quasi Fermi energy
E_{Fp^+}	Holes quasi Fermi energy
E_t	Trap energy level
E_v	Valence band energy level
h	Planck‘s constant
I_0	Reverse saturation current through PPD
I_ϕ	Light intensity
$I_{D'}$	MOS technological parameter
I_f	Forward current

I_{ph}	Photocurrent
I_{st}	Saturation current
$I_{\text{sub\_TG}}$	Subthreshold leakage current below TG
$I_{\text{sub\_TG1}}$	Subthreshold leakage current from PPD to potential pocket
$I_{\text{sub\_TG2}}$	Subthreshold leakage current from potential pocket to TG/FD
I_{th}	Thermionic emission current
I_{total}	Total current flowing across the PPD
k	Boltzmann constant
l_{abs}	Length of absorption
λ	Wavelength of light
η_{noise}	Total noise at given signal level
η_{psn}	Total photon shot noise at given signal level
n	Resolution of ADC
N_{max}	Maximum output signal
N_{min}	Minimum detectable signal
N_{PPD}	Number of PPD charges
$N_{\text{PPD\_left}}$	Number of charges left in the PPD
N_{sig}	Signal level
N_t	Trap density
N_{TD}	Donor trap density
ϕ	photon flux
$\Psi_{\text{TG\_ch}}$	TG channel potential
$\Psi_{\text{TG\_int}}$	PPD-TG interface potential
$\Psi_{\text{TG\_inv}}$	TG channel inversion potential
p_0	Equilibrium hole concentration
q	Electronic charge
Q_{FIX}	Temperature dependent fixed PPD charge
Q_{inj}	Injected charge in PPD
Q_{PPD}	PPD charge
$Q_{\text{PPD\_i}}$	Instantaneous PPD charge
Q_{VAR}	Light intensity dependent variable PPD charge
σ_t	Capture cross section area of interface traps
τ	Recombination lifetime of minority charge carriers
T	Temperature
t_{int}	Integration time

t_{hold}	Hold time
ν	Frequency of light
V_B	Potential barrier
$V_{\text{B\_eff}}$	Effective potential barrier
V_{bi}	Built-in potential
V_{DD}	Supply voltage
$V_{\text{DD\_RST}}$	Drain voltage of reset transistor
V_{FS}	Full scale voltage of ADC
V_{FW}	Full well voltage of PPD
V_{inj}	Injection voltage
V_n	Potential of n_{well} in PPD
V_{OC}	Open circuit voltage of PPD
V_{p^+}	Potential of p^+ in PPD
$V_{\text{p}_{\text{epi}}}$	Potential of p_{epi} in PPD
V_{pin}	Pinning potential of PPD
V_{PPD}	PPD potential
ΔV_{PPD}	Change in PPD potential
$V_{\text{RST\_low}}$	Reset transistor low voltage
$V_{\text{RST\_high}}$	Reset transistor high voltage
V_T	Threshold voltage
V_{TG}	Transfer gate voltage
$V_{\text{TG\_low}}$	Transfer gate low voltage
$V_{\text{TG\_high}}$	Transfer gate high voltage
V_{th}	Thermal voltage
w_0	Width of the depletion region of PPD at equilibrium
$w_{\text{n}-\text{p}_{\text{epi}}}$	Width of depletion region of $n_{\text{well}} - p_{\text{epi}}$ in PPD
$w_{\text{p}^+-\text{n}}$	Width of depletion region of $\text{p}^+ - \text{n}_{\text{well}}$ in PPD
Δx	Reduction in width of the depletion region in PPD on illumination