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A STUDY OF ANODIC Al_2O_3 FILMS AND THEIR APPLICATION TO A NOVEL TWO PHASE CCD STRUCTURE

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CERTIFICATE

This is to certify that the dissertation "A Study of Anodic Al_2O_3 Films and their application to a novel Two Phase CCD Structure" which is being submitted by K. Srinivasa Chari for the award of Doctor of Philosophy at the Indian Institute of Technology, Delhi, is a record of bonafide research work. He has carried out this research work under our guidance and supervision.

This dissertation has reached the standard fulfilling the requirements of the regulations relating to this degree. The results obtained in this dissertation have not been submitted to any other University or Institute for the award of any degree or diploma.

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ABSTRACT

A Charge Coupled Device technology based on anodic Al_2O_3 films has been proposed and developed in this study. For the development of this technology, the growth of high quality anodic Al_2O_3 films has been studied in detail. An electrolyte bath consisting of 2% tartaric acid of pH 6.0 and ethylene glycol in the ratio of 1:2 was found to give high integrity Al_2O_3 films. Several thousands of films in the thickness range of 50 - 500 nm were reliably and reproducibly grown. These oxides were found to be anhydrous and amorphous for oxide thicknesses below 200 nm. Thicker films were crystaline (γ-Al_2O_3). Thin as-grown oxides (less than 100 nm) exhibited rectification properties and the MIM capacitance was found to follow a $C \propto V^{-1/3}$ law. These behaviours disappeared after suitable post anodization anneal or by allowing for completion of the anodization process. These inhomogeneous films have been modelled as p-i-n structures.

Double dielectric structures were fabricated by complete conversion of aluminum films up to 300 nm in thickness. Using this technique, MAOS capacitors and MAOS transistors were fabricated and tested. The studies on MAOS capacitors indicated the existence of a positive oxide charge close to the SiO_2-Al_2O_3 interface. Both post anodization heat treatment cycles and completeness of anodic conversion reduced the positive oxide charge

density. The $|V_{FB}|$ for a typical annealed MAOS structures (SiO_2 = 120 nm, Al_2O_3 = 95 nm) was in the range 6 to 6.5 V. The $Si-SiO_2$ interface state density in these structures was of the order of 5×10^{10} cm^{-2} eV^{-1}. MAOS FET's with a gm $\approx$ 220 µS and threshold voltages similar to the MAOS capacitors were also fabricated.

A novel 2 Ø overlapping-gate double-dielectric CCD structure using anodic Al_2O_3 in the active area has been proposed and experimentally demonstrated. It is essentially a stepped insulator structure, the double-dielectric (SiO_2-Al_2O_3) region forming the 'barrier area' and the single dielectric (SiO_2) region the 'storage area' of the gates. Test 4-bit p-channel CCD's fabricated with the developed technology exhibited charge transfer inefficiencies of 3×10^{-3} (at 50% FZ) and could be clocked up to 200 kHz.

LIST OF FIGURES

Figure		Page
1.1	Schematic cross section of a two phase double-dielectric CCD	6
2.1	Oxide thickness, forming voltage as a function of growth time for typical constant voltage and constant current anodization processes	16
2.2	Experimental set-up for anodic oxidation	18
2.3	Forming voltage plots as a function of growth time for different bath pH values	23
2.4	Transmission and scanning electron micrographs of oxides	25
	a,b Transmission pictures of oxide grown at pH 2.0	
	c Electron microscope picture of oxide grown at pH 10.0	
2.5	Oxide thickness as a function of bath pH value	28
2.6	Forming voltage as a function of growth time for different bath concentrations	29
2.7	Forming voltage as a function of growth time for oxide growth in contaminated baths	33
2.8	Scanning electron microscopy pictures of oxides grown in Cl^- contaminated baths	34
2.9	Forming voltage as a function of growth time for growth process in different electrolytes	36
2.10	Forming voltage as a function of growth time for oxide growth with different current densities	38
2.11	Scanning electron micrographs of oxides grown in different baths	40
	a Oxide grown in aqueous tartaric acid bath	
	b Oxide grown in tartaric acid-glycol bath	

Figure		Page
2.12	Electron diffraction patterns and transmission micrograph observed on anodic films grown in 2% tartaric acid-glycol bath	43
	a,b Electron diffraction pattern obtained on thick (220 - 300 nm) Al_2O_3 Films	
	c Transmission electro microscopy picture of crystalline Al_2O_3	
	d Electron diffraction pattern obtained on thin anodic Al_2O_3 film	
2.13	Resistivity as a function of oxide thickness	49
2.14	Breakdown field strength as a function of thickness	52
2.15	Volt-ampere characteristics of anodic films grown at different bath pH values	53
3. 1	Cross section of a MIM sandwich structure	60
3. 2	Set up for I-V measurements	62
3. 3	I-V characteristics of thin anodic film (93 nm)	63
3. 4	I-V characteristics of 105 nm thick anodic film	64
3. 5	I-V characteristics of thick (175 nm) anodic film	65
3. 6	Semi-log plot of forward I-V characteristics of 93 nm Al_2O_3 thin film diode	67
3. 7	Semi-log plot of forward I-V characteristics of 105 nm Al_2O_3 thin film	68
3. 8	I-V of stressed and virgin thick (175 nm) anodic film log-log plot	70
3. 9	Forward current as a function of square root of applied voltage for as grown anodic Al_2O_3 film semi-log plot	72
3.10	Dependence of forward I-V characteristics on growth current log-log plot	74

Figure		Page
3.11	Asymmetry in the I-V characteristics as a function of growth current density	76
3.12	Effect of counter-electrode materials on the I-V characteristics of as-grown anodic Al_2O_3 films	77
3.13	Dependence of capacitance on applied voltage for thin anodic films	79
3.14	I-V characteristics of annealed anodic film	81
3.15	Current as a function of square root of applied voltage for annealed anodic films	82
3.16	p-i-n model for anodic films	84
4. 1	Double dielectric process	91
4. 2	Band diagram for MOS capacitor	94
4. 3	Energy band diagram for double dielectric MAOS capacitor	95
4. 4	C-V characteristics of MOS and MAOS capacitors	99
4. 5	Anodization current density, forming voltage versus time plots for complete anodization process	101
4. 6	Dependence of double dielectric flatband voltage on anodization current density	103
4. 7	Effect of low temperature post anodization heat treatment on double dielectric flatband voltage	104
4. 8	Dependence of double dielectric flatband voltage on post-anodization heat treatment temperature	105
4. 9	Diffraction pattern and transmission electron micrographs of high temperature heat treated anodic oxide	106
	a Diffraction pattern	
	b Transmission micrograph	

Figure		Page
4.10	Dependence of double dielectric flatband voltage on Al_2O_3 thickness during etch back sequence	109
4.11	Double dielectric flat band voltage as a function of grown Al_2O_3 thickness	111
4.12	$Si-SiO_2$ interface state density in double dielectric structures as a function of post anodization heat treatment temperature and duration	117
4.13	C-V and C-t plots of MOS capacitor	118
4.14	C-V and C-t plots of MAOS capacitor fabricated by double dielectric process	119
4.15	Cross sectional view of double dielectric MOSFET (MAOST)	129
4.16	Process outline for MAOST	129
5. 1	Energy-band diagrams for surface-channel MOS capacitor	137
	a In deep depletion	
	b With mobile charge	
5. 2	Schematic of a three-phase CCD operation	139
5. 3	Cross section of two phase structures	142
5. 4	Schematic cross section of two phase double dielectric CCD	147
5. 5	Construction of two phase double dielectric CCD	149
5. 6	Calculated values of surface potential as a function of gate bias for single dielectric and double dielectric regions with Al_2O_3 thickness as variable parameter	152
5. 7	Mask layout for test 4-bit double dielectric CCD shift register	153
5. 8	Fabrication sequence of double dielectric CCD	156

Figure | Page

5. 9 Photomicrograph of 4-bit double dielectric CCD shift register 161

5.10 Pre-tests on fabricated test device 162

a Inter-phase isolation in double dielectric CCD

b Drain I-V characteristics of CCD operated as MOSFET

c Transfer characteristics of the CCD operated as MOSFET

5.11 C-V plots of double dielectric CCD phases 166

5.12 Calculated plots of surface potential for single dielectric and double dielectric regions 168

5.13 Charge injection method used in double dielectric CCD's 169

5.14 Charge detection scheme used in double dielectric CCD's 172

5.15 Test set up for analog and digital operation of CCD's 174

5.16 Response of double dielectric CCD shift register to analog and digital inputs 175

5.17 Transfer characteristics of double dielectric CCD 177

5.18 Charge transfer inefficiency measurement technique 180

5.19 Effect of rise time of clock drive waveforms on the observed output 182

5.20 Measured curves of inefficiency product as a function of clock pulse amplitude 184

5.21 Measured plots of inefficiency product as a function of clock resting potential 185

5.22 Dependence of charge transfer inefficiency on signal amplitude 187

5.23 Measured leading edge loss as a function of singal level 189

5.24 Measured plots of loss per transfer versus clock frequency 190

5.25 Measured leading edge loss verus fat zero level for a double dielectric CCD operated with different signal levels 190A

LIST OF TABLES

Table		Page
2.1	Existing electrolyte baths	14
2.2	Electrolyte baths tried	20
2.3	Electrolyte baths used in this study	22
2.4	Chemical analysis results of contaiminated electrolyte baths	31
2.5	Identification of the structure of anodic Al_2O_3 films	44
2.6	Summary of Infrared reflectance spectra results	46
4.1	Flatband voltage distribution across the wafer (MAOS) obtained with double dielectric process	114
4.2	Summary of B-T stress tests	122
4.3	Summary of Lifetime and storage time measurements	122
5.1	Processing sequence for double dielectric CCD fabrication	157 158
5.2	Features of double dielectric CCD	196

NOMENCLATURE

CCD	Charge Couple Device
MOS	Metal-SiO_2-Si structure
MAOS	Metal-Al_2O_3-SiO_2-Si structure
MIM	Metal-Insulator (Al_2O_3)-Metal
M-I-Solution	Metal-Insulator (Al_2O_3) electrolyte system
B-T	Bias-temperature test
ACT	Accelerated Corrosion Test
ATR	Attenuated Transmission Reflectance
AAS	An aqueous tartaric acid process
AGW	A glycol-water process
NAS	Non-aqueous Borate-glycol process
Al_2O_3	Aluminum oxide
Cr_2O_3	Chromic acid
H_3Po_4	Phosphoric acid
BHF	Buffered Hydrofluoric acid
HF	Hydrofluoric acid
DI	Deionised water
BN	Boron Nitride source
$Pocl_3$	Phosphorous Trichloride
ppm	parts per million
pH	the product of Hydrogen-ion concentration and hydroxyl-ion concentration expressed in gramme-molecules per liter
W.No	wave number
J_g	current density during anodic growth process

J	current density
I	current
V	applied voltage
d	thickness of insulator
F	applied field (V/d)
ϵ_o	permittivity of free space
ϵ_{ox}	dielectric constant of SiO_2
ϵ_A	dielectric constant of Al_2O_3
ϵ_s	semiconductor permittivity
k^*	dynamic dielectric constant
T_A	Al_2O_3 thickness
T_{ox}	SiO_2 thickness
Q_{ss}	positive interfacial charge layer (at Si-SiO_2)in SiO_2
Q_A	SiO_2-Al_2O_3 interfacial charge layer in MAOS structure
Q_m	minority carrier charge
Q_i	injected charge
Q_o	full-well capacity
Q	actual amount of charge injected
$\rho_A(x)$	charge density in Al_2O_3
λ_s	semiconductor electron affinity
ϕ_m	metal work function
E_F	fermilevel
E_i	intrinsic fermilevel
ψ_B	$= \frac{E_F - E_i}{q}$ = bulk potential

E_g	band gap
V_{FB}	flatband voltage
V_{TH}	threshold voltage
V_{ID}	input diode potential
V_{IG}	input gate potential
V_{sig}	input signal to CCD
V_R	resting potential of clock drive waveforms
V_p	peak clock pulse voltage
V_i	voltage across the insulator(s)
N_D	substrate donor concentration
n_i	intrinsic carrier concentration
C_o	oxide capacitance per area
C_f	equilibrium capacitance
W	channel width
L	gate length
s_o	surface recombination velocity
τ	minority carrier lifetime
τ_g	generation lifetime = 2τ
τ_d	thermal diffusion time constant
τ_c	available charge injection time
T_s	storage time
T_r	rise time of clock pulse
ψ_{so}	surface potential with empty well
ψ_s	surface potential in the presence of minority carrier charge

V_s change in surface potential with and without signal charge = $\psi_s - \psi_{so}$

ψ_o barrier height

x_d depletion layer width

SHC signal handling capacity

C-V capacitance-voltage

C-t capacitance-time

β_{pf} Poole-Frenkel coefficient

g_m the gain of the **MAOST** expressed in the units of Siemens

Δ_i amounts of signal charge missing from output leading train

Δ_i' amounts of signal charge in excess at trailing edges

ϵ charge transfer inefficiency

η charge transfer efficiency $(1-\epsilon)$

n number of elements (CCD gates)

m number of phases

L_L leading edge loss

L_T trailing edge loss

FZ Fat Zero (background charge)

μ_p surface hole mobility

D diffusion coefficient of minority carriers$(kT/q\mu_p)$

N_{ss} $Si\text{-}SiO_2$ interface state density

R_L load resistance in output drain circuit

k Boltzmann constant

T absolute temperature

q electronic charge

CONTENTS

			Page
		Acknowledgements	i
		Abstract	iii
		List of Figures	v
		List of Tables	x
		Nomenclature	xi
CHAPTER	I	INTRODUCTION	1
CHAPTER	II	GROWTH AND CHARACTERIZATION OF ANODIC Al_2O_3 FILMS	9
CHAPTER	III	ELECTRICAL PROPERTIES	57
CHAPTER	IV	STUDY OF DOUBLE-DIELECTRIC (SiO_2-Al_2O_3) STRUCTURES	88
CHAPTER	V	DOUBLE-DIELECTRIC TWO PHASE CCD	134
CHAPTER	VI	CONCLUSIONS	200
		REFERENCES	205
Appendix	I	Anodic Cell Design	217
Appendix	II	Preclean-Preoxidation Cleaning Procedure	219
Appendix	III	Phosphorous Diffusion Process	220
Appendix	IV	Diode Contact Window Opening	222
Appendix	V	p^+-n Diode Process	224
Appendix	VI	Channel Stop Diffusion (n^+-n) Process	226
		VITA	228