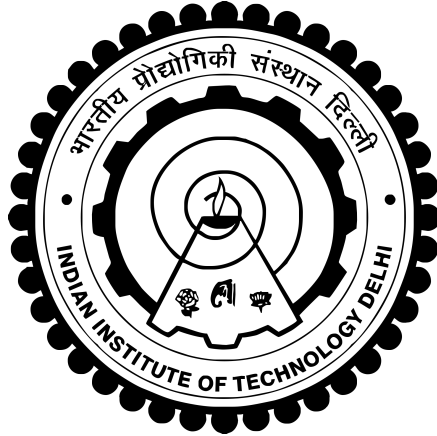


Integrated mm-Wave Receiver Components for Low-Power Applications

Sanjeev Kumar



Centre for Applied Research in Electronics
INDIAN INSTITUTE OF TECHNOLOGY DELHI

July 2025

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Sanjeev Kumar

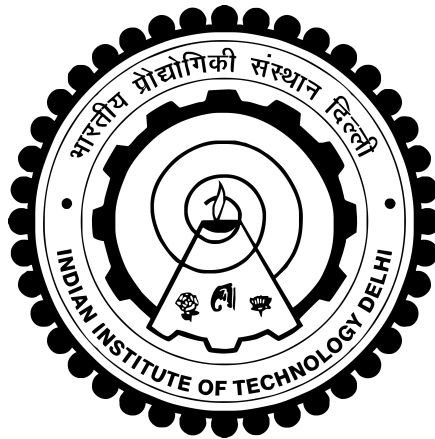
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Submitted

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July 2025

CERTIFICATE

This is to certify that the thesis titled **Integrated mm-Wave Receiver Components for Low-Power Applications**, submitted by **Sanjeev Kumar (2016CRZ8569)**, to the Indian Institute of Technology, Delhi, for the award of the degree of **Doctor of Philosophy**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.



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ABSTRACT

The primary focus of the proposed thesis is on the design and implementation of integrated mm-wave receiver components for low-power. The receiver components consist of an on-chip antenna, a low-noise amplifier, and a quadrature voltage-controlled oscillator. The on-chip antenna is designed and fabricated in a 180 nm CMOS process, and the LNA is designed and fabricated in a TSMC 65 nm CMOS process. The LNA and QVCO are designed for low power consumption.

This work is divided into three parts; the first one discusses the on-chip CMOS antenna, the second one discusses the 36 GHz LNA, and the third one discusses the two QVCOs, one at 36 GHz and the second one at 60 GHz frequency of operation. Two patch antennae are discussed at a nominal resonance frequency of 77 GHz, namely a thin-substrate antenna and a thick-substrate antenna, using a standard 0.18 μm CMOS technology. Both the antennae are implemented on metal-6. The thin-substrate antenna uses metal-5 as the ground plane, and the thick-substrate antenna uses metal-1 as the ground plane. The thin-substrate antenna was fabricated on a 0.18 μm CMOS process and characterized. The thick-substrate antenna was only simulated. Measurements of the thin-substrate antenna show a peak S_{11} of -18.22 dB at 99.8 GHz. In the simulation, the thin-substrate antenna has a peak gain and radiation efficiency of -25 dB and 1%, respectively, at 77 GHz. The thick-substrate antenna has a simulated peak gain and radiation efficiency of 5.18 dB and 58.31% respectively at 77 GHz.

The second part presents G_m boosted CG–CS low power, high gain LNAs for 5G applications. The LNA is cascaded with a CG cascoded stage and a CS cascoded stage. In the first stage, a transformer-based gm boosting technique has been used along with series peaking. The second stage is used to increase the gain in total. The two LNAs are discussed, the Single Stage LNA and a Two Stage LNA. Both the LNAs are designed and fabricated in the TSMC 65 nm CMOS process. The single-stage LNA measured results show a gain of 9 dB and a noise figure of 4.1 dB. The minimum NF obtained is 3.8 dB at 36.2 GHz and is below 4 dB from 33 GHz to 37 GHz. The proposed LNA consumes only 4 mW from a 1-V supply.

The third part presents two QVCOs, one at 36 GHz and the second at 60 GHz. The first one is a 36 GHz quadrature voltage-controlled oscillator (QVCO) designed and fabricated with a transistor coupling mechanism that uses only one single-turn ring inductor. The second QVCO is a 60 GHz transformer-coupled low-power quadrature voltage-controlled oscillator (QVCO), also designed using a single-turn ring inductor. The single-turn inductor

is shared by the pair of oscillators in both the QVCOs. A digital cap bank is used for fine-tuning the oscillator. The circuit is designed in a 65 nm CMOS process. The frequency of the oscillator is tuned from 59.5 to 60.5 GHz. The proposed 60 GHz QVCO exhibits a phase noise of -81 dBc/Hz at 1 MHz offset frequency. The DC power consumption is 3.3 mW with a supply voltage of 1 V.

KEYWORDS: RFIC, Fifth generation millimeter wave (5G mmWave) communication systems, 36-GHz, 60 GHz, 77GHz, receiver (Rx), low noise amplifier, mmWave, QVCO, On-chip antenna

सार

प्रस्तावित थीसिस का प्राथमिक ध्यान कम-शक्ति के लिए एकीकृत मिमी-वेव रिसीवर घटकों के डिजाइन और कार्यान्वयन पर है। रिसीवर घटकों में एक ऑन-चिप एंटीना, एक कम-शोर एम्पलीफायर और एक चतुर्भुज वोल्टेज-नियंत्रित ऑसिलेटर शामिल है। ऑन-चिप एंटीना को 180 एनएम CMOS प्रक्रिया में डिजाइन और निर्मित किया गया है, और LNA को TSMC 65 एनएम CMOS प्रक्रिया में डिजाइन और निर्मित किया गया है। LNA और QVCO को कम बिजली की खपत के लिए डिजाइन किया गया है। यह कार्य तीन भागों में विभाजित है; पहला भाग ऑन-चिप CMOS एंटीना पर चर्चा करता है, दूसरा भाग 36 GHz LNA पर चर्चा करता है, और तीसरा भाग दो QVCO पर चर्चा करता है, एक 36 GHz पर और दूसरा 60 GHz संचालन आवृत्ति पर। 77 गीगाहर्ट्ज की नाममात्र अनुनाद आवृत्ति पर दो पैच एंटीना पर चर्चा की गई है, अर्थात् एक पतला-सब्सट्रेट एंटीना और एक मोटा-सब्सट्रेट एंटीना, जो मानक 0.18 माइक्रोन सीएमओएस तकनीक का उपयोग करता है। दोनों एंटीना धातु-6 पर कार्यान्वित किए जाते हैं। पतला-सब्सट्रेट एंटीना ग्राउंड प्लेन के रूप में धातु-5 का उपयोग करता है, और मोटा-सब्सट्रेट एंटीना ग्राउंड प्लेन के रूप में धातु-1 का उपयोग करता है। पतला-सब्सट्रेट एंटीना 0.18 माइक्रोन सीएमओएस प्रक्रिया पर निर्मित किया गया था और इसकी विशेषता बताई गई थी। मोटा-सब्सट्रेट एंटीना केवल सिमुलेट किया गया था। पतले-सब्सट्रेट एंटीना के माप 99.8 गीगाहर्ट्ज पर -18.22 डीबी का पीक एस11 दिखाते हैं। सिमुलेशन में, पतले-सब्सट्रेट एंटीना में 77 गीगाहर्ट्ज पर क्रमशः -25 डीबी और 1% का पीक लाभ और विकिरण दक्षता है। मोटे सब्सट्रेट वाले एंटीना में 77 गीगाहर्ट्ज पर क्रमशः 5.18 डीबी और 58.31% का सिमुलेटेड पीक गेन और रेडिएशन दक्षता है। दूसरा भाग 5G अनुप्रयोगों के लिए Gm बूस्टेड CG-CS कम पावर, हाई गेन LNA प्रस्तुत करता है। LNA को CG कैस्कोडेड स्टेज और CS कैस्कोडेड स्टेज के साथ कैस्केड किया जाता है। पहले चरण में, श्रृंखला पीकिंग के साथ एक ट्रांसफॉर्मर-आधारित जीएम बूस्टिंग तकनीक का उपयोग किया गया है। दूसरे चरण का उपयोग कुल लाभ को बढ़ाने के लिए किया जाता है। दो LNA पर चर्चा की गई है, सिंगल स्टेज LNA और टू स्टेज LNA। दोनों LNA को TSMC 65 एनएम CMOS प्रक्रिया में डिजाइन और निर्मित किया गया है। सिंगल-स्टेज LNA मापे गए परिणाम 9 dB का लाभ और 4.1 dB का शोर आंकड़ा दिखाते हैं। प्राप्त न्यूनतम एनएफ 36.2 गीगाहर्ट्ज पर 3.8 डीबी है और 33 गीगाहर्ट्ज से 37 गीगाहर्ट्ज तक 4 डीबी से कम है। प्रस्तावित एलएनए 1-वी आपूर्ति से केवल 4 एमडब्ल्यू की खपत करता है। तीसरा भाग दो क्यूवीसीओ प्रस्तुत करता है, एक 36 गीगाहर्ट्ज पर और दूसरा 60 गीगाहर्ट्ज पर। पहला एक 36 गीगाहर्ट्ज क्वाडरेचर वोल्टेज-नियंत्रित ऑसिलेटर (क्यूवीसीओ) है जिसे एक ट्रांजिस्टर युग्मन तंत्र के साथ डिजाइन और निर्मित किया गया है जो केवल एक सिंगल-टर्न रिंग इंडक्टर का उपयोग करता है। दूसरा क्यूवीसीओ एक 60 गीगाहर्ट्ज ट्रांसफॉर्मर-युग्मित कम-शक्ति क्वाडरेचर वोल्टेज-नियंत्रित ऑसिलेटर (क्यूवीसीओ) है, जिसे सिंगल-टर्न रिंग इंडक्टर का उपयोग करके भी डिजाइन किया गया है। सिंगल-टर्न इंडक्टर

दोनों क्यूवीसीओ में ऑसिलेटर की जोड़ी द्वारा साझा किया जाता है। ऑसिलेटर को ठीक करने के लिए एक डिजिटल कैप बैंक का उपयोग किया जाता है। सर्किट को 65 एनएम CMOS प्रक्रिया में डिजाइन किया गया है। ऑसिलेटर की आवृत्ति 59.5 से 60.5 गीगाहर्ट्ज तक ट्यून की गई है। प्रस्तावित 60 गीगाहर्ट्ज QVCO 1 मेगाहर्ट्ज ऑफसेट आवृत्ति पर -81 dBc/Hz का चरण शोर प्रदर्शित करता है। 1 V की आपूर्ति वोल्टेज के साथ DC बिजली की खपत 3.3 mW है।

कीवर्ड: RFIC, पांचवीं पीढ़ी के मिलीमीटर वेव (5G mmWave) संचार प्रणाली, 36-GHz, 60 GHz, 77GHz, रिसीवर (Rx), कम शोर एम्पलीफायर, mmWave, QVCO, ऑन-चिप एंटीना

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ABBREVIATIONS

CMOS	Complementary metal oxide semiconductor
CS	Common source
CG	Common gate
DC	Direct current
EM	Electro-magnetic
GSG	Ground-signal-ground
VCO	Voltage controlled oscillator
Si	Silicon
SiO₂	Silicon dioxide
mm-wave	Millimeter-wave
LNA	Low-noise amplifier
ICs	Integrated circuits
MIM	Metal-insulator-metal
NF	Noise figure
QVCO	Quadrature VCO
P1dB	1 dB compression point
PN	Phase noise
dB	Decibel
RFIC	Radio frequency integrated circuit
TSMC	Taiwan semiconductor manufacturing company
Rx	Receiver
PDK	Process design kit
EM	Electromagnetic
Q-factor	Quality factor
VLSI	Very large scale integration
RF	Radio frequency
μ	Micro
SRF	Self resonating frequency
SoC	System on chip
DFM	Design for manufacturability
NRFR2	New radio frequency range 2
PVT	Process voltage and temperature
NC-LNA	Noise figure
NF_{min}	Minimum noise figure

5G	5 th generation mobile communication
ISM	Industrial scientific and medical
WLAN	Wireless local area network
FOM	Wireless local area network
ISF	Impulse sensitivity function
FMCW	Frequency modulated continuous wave
PCB	Printed circuit board

NOTATION

μ	Micro
Ω	Ohm
L	Series inductance per unit length
mm	millimeter
$NFmin$	Minimum noise figure
Pdc	DC Power consumption