DESIGN AND SIMULATION OF NANOSCALE TUNNELING FIELD EFFECT TRANSISTORS FOR CMOS APPLICATIONS

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CERTIFICATE

This is to certify that the thesis entitled *"**Design and Simulation of Nanoscale Tunneling Field Effect Transistors for CMOS Applications***" being submitted by Sneh Saurabh to the Indian Institute of Technology, Delhi, in the Electrical Engineering Department is a bona fide work carried out by him under my supervision and guidance. The research reports and the results presented in this thesis have not been submitted in parts or in full to any other University or Institute.

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ABSTRACT

The density and the speed of integrated circuit (IC) components have increased roughly exponentially for the last several decades. As the ICs shrink and the devices are scaled downwards, subthreshold leakage current and the associated leakage power are increasing. Keeping the leakage power under control, especially at smaller geometries, poses a serious challenge to the device engineers. Conventional MOSFET technology, with the subthreshold slope limited to 60 mV/decade, cannot achieve low leakage current and high performance, simultaneously, at advanced technology nodes. The Tunnel Field Effect Transistor (TFET) is a novel device that has an extremely low leakage current and exhibits subthreshold slope better than 60 mV/decade. However, a TFET cannot deliver sufficient on-current, especially at low supply voltages (0.5 V or below). Other problems associated with TFETs are: i) high threshold voltage ii) delayed saturation in the output characteristics, and iii) greater susceptibility to DIBL effects. The primary objective of this research work is to identify the problems in the TFETs that are a hurdle in their CMOS applications and find solutions to these problems.

In this work, a novel device called as Strained Double Gate Tunnel Field Effect Transistor (SDGTFET) is proposed. Using 2-D device simulations, it is demonstrated that an SDGTFET has a better electrical characteristics compared to a conventional Double Gate Tunnel Field Effect Transistor (DGTFET). The most important advantage of an SDGTFET is that the on-current improves by around 2 orders of magnitude without significantly degrading the off-current. The parameters of the device can be engineered to achieve a particular ratio of on-current and off-current. The average

subthreshold swing of an SDGTFET is excellent. An SDGTFET also shows good immunity against short channel effects. This research work, for the first time, illustrates the estimation of the process-induced variations in a TFET. It is shown that the impact of process induced variations on the electrical properties of a DGTFET is quite high and can be one of the limiting factors for its wide-scale application. It is demonstrated that an SDGTFET with a high-k gate dielectric can successfully bring down the impact of process induced variations on the on-current and the threshold voltage.

In this work, the implications of the application of a dual material gate (DMG) in a TFET are studied. It is demonstrated that the DMG can be applied in a TFET to obtain a good on-current, off-current and threshold voltage tradeoffs along with an improvement in the average subthreshold slope, improve the nature of the output characteristics and increase the immunity against the DIBL effects. It is also shown that DMG provides a technique to exploit the advantages of both a high and a low work-function gate in a TFET and thereby obviates the problems of both these types of gates. Additionally, this research work demonstrates that an SDGTFET with high-k gate dielectric exhibits a high on-current, excellent average subthreshold slope, extremely low off-current, early onset of saturation and greater immunity against DIBL effects. As a result, an SDGTFET with high-k gate dielectric leads to the realization of a CMOS inverter with improved gain.

In this research work, various novel TFET device structures have been proposed and investigated. It has been demonstrated that the proposed TFETs are capable of ameliorating several known problems in a TFET. A greatly improved on-current, along

with an excellent subthreshold slope, is achieved. The nature of the output characteristics and the immunity of these devices against DIBL effect show considerable improvement. As per latest ITRS report on emerging devices, TFETs are one of the most promising candidates for future low power CMOS applications (V_{DD} < 0.5 V, L < 10 nm) and could even be instrumental in extending the technology beyond the current ITRS roadmap. From this perspective, this research work can be considered as a small step towards this endeavor.

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