DESIGN OF LOW POWER HIGH-SPEED LINKS

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Certificate

This is to certify that the thesis entitled ***"Design of Low Power High-Speed Links"***, being submitted by **Mr. Paramjeet Singh Sahni** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, for the award of the degree of **Doctor of Philosophy**. It is a record of the original bonafide research work carried out by him under our guidance and supervision. The matter embodied in this thesis has not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

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– Paramjeet Singh Sahni

Abstract

One of the key challenges in the design of high-speed links and particularly upcoming multimedia interfaces like High Definition Multimedia Interface 2.0 (HDMI) and DisplayPort 1.2a (DP) is that higher data rates need to be supported over existing low-bandwidth, low-cost transmission media for backward compatibility and cost effectiveness. The proliferation of such physical interfaces in battery driven systems has demanded significant power reduction along with an increase in throughput.

This work proposes architectural and circuit level improvement targeting low-power high-data-rate transmitter and receiver designs. The proposals are implemented in a 28 nm ultra-thin body and buried oxide (UTBB) fully depleted silicon on insulator (FDSOI) technology, for recently developed high data rate specification for display interfaces, HDMI 2.0 and DP. Detailed measurement results emphasizing the improvement in energy efficiency are presented.

For receiver design, a multi-stage continuous-time linear equalizer (CTLE) design with a controllable transfer function is proposed. The entire frequency range of interest, from DC to gain roll-off frequency is divided into six regions and the transfer function of the CTLE in each region is independently controlled and adapted to be the inverse of the channel transfer function in the respective frequency regions. Linear amplifiers are followed by CMOS buffers to provide a rail-to-rail output, which led to the design of a low power slicer, clock data recovery (CDR) circuit, and a low power receiver design. A digital adaptation scheme to adapt the CTLE

transfer function is also proposed.

The equalizer is used for 6.0 Gb/s data transfer per channel for high definition multimedia interface 2.0 (HDMI) receiver and 5.4 Gb/s per channel for DisplayPort (DP) receiver designs. Fabricated in a 28 nm UTBB-FDSOI technology, the 0.06 mm^2 CTLE consumes 30 mW and achieves up to 28 dB of tunable peaking.

The entire receiver channel occupies 0.21 mm^2, consumes 55 mW and achieves an energy efficiency of 9.2 pJ/bit at 6.0 Gb/s, which is better than recently published works. A detailed comparison with recent publications for HDMI and DP is presented. This design achieves a jitter tolerance of 0.7 UI up to 10 MHz for HDMI, and 0.42 UI up to 100 MHz for DP, which is better than their respective specifications.

For the design of a power-optimized transmitter, it is proposed to reuse power from the receiver signal current. In an open drain transmitter, signaling is achieved by pulling current from one of the two receiver termination impedances. It is proposed to re-architect the open drain transmitter to harvest power of the receiver signal current. This receiver signal current is re-used to run the digital, analog and custom digital signal circuits of the transmitter. Harvested signal current is used to create a supply voltage which is regulated by a shunt regulator. There is no local power supply needed at the transmitter side, and no extra power is taken from the receiver apart from whatever power comes out of it during standard signaling. Using the proposed power harvesting technique, the design of a zero power HDMI transmitter capable of 4.95 Gb/s data rate, i.e. 1.65 Gb/s per channel is presented.

At high data rates, the power demanded by the transmitter circuit increases and cannot be met by the harvested signal power. The balance power requirement is met by augmenting the harvested supply with the local transmitter supply. The generated power supply is maintained stable despite being supported by two sources - the harvested current from receiver signal and the local transmitter supply. The architecture to manage two different supply sources, achieving a very high energy efficiency of 0.9 pJ/bit at 18.0 Gb/s transmission is presented. The HDMI2.0 transmitter was designed in 28nm UTBB-FDSOI technology. The power consumption from the local supply is adapted to the data rate. As the data rate reduces, the power consumption of the transmitter from local transmitter supply drops to zero.

सार

हाई स्पीड लिंक, विशेष रूप से मल्टीमीडिया इंटरफेस जैसे हाई डेफिनिशन मल्टीमीडिया इंटरफेस 2.0 (एच. डी. एम. आई.) और डिस्प्लेपोर्ट 1.2 ए (डी.पी.) के डिजाइन में प्रमुख चुनौतियों में से एक यह है कि उच्च डेटा दरों को मौजूदा केबलों पर चलाने की आवश्यकता है, जो कम बैंडविड्थ हैं और कम लागत वाली हैं। बैटरी संचालित प्रणालियों में ऐसे मल्टीमीडिया इंटरफेस के उपयोग ने बिजली की खपत में कमी की मांग की है।

यह शोध कार्य उच्च डेटा दर और कम बिजली उपभोग करने वाले ट्रांसमीटर और रिसीवर डिजाइन को लक्षित करने वाले वास्तुकला और सर्किट स्तर में सुधार का प्रस्ताव करता है। इन प्रस्तावों को 28 एन एम अल्ट्राथिन बॉडी और दफन ऑक्साइड (यू. टी. बी. बी.) में इंस्यूलेटर (ए. फ. डी. एस. ओ. आई.) प्रौद्योगिकी पर पूरी तरह से बनाया गया है। ऊर्जा दक्षता में सुधार पर जोर देने वाले विस्तृत माप परिणाम प्रस्तुत किए जाते हैं।

रिसीवर डिजाइन के लिए, एक बहु मंच निरंतर समय रैखिक एक नियंत्रणीय हस्तांतरण समारोह के साथ तुल्यकारक (सीटीएलई) डिजाइन प्रस्तावित है। ब्याज की पूरी आवृत्ति सीमा, डी.सी. से रोल-ऑफ आवृत्ति हासिल करने के लिए छह क्षेत्रों में बांटा गया है। प्रत्येक क्षेत्र में CTLE का स्थानांतरण कार्य स्वतंत्र रूप से नियंत्रित और अनुकूलित किया जाता है। ट्रांसफर फ्यूशन को संबंधित आवृत्ति क्षेत्रों में चैनल ट्रांसफर फ़ंक्शन के विपरीत होने के लिए ट्यून किया गया है। रेल-टू-रेल आउटपुट प्रदान करने के लिए सीएमओएस बफर के बाद रैखिक एम्पलीफायरों का पालन किया जाता है। ये कम पावर स्लाइसर, घड़ी डेटा रिकवरी (सीडीआर) सर्किट, और इस प्रकार कम पावर रिसीवर डिज़ाइन के डिजाइन की ओर ले जाते हैं। सीटीएलई स्थानांतरण समारोह को अनुकूलित करने के लिए एक डिजिटल अनुकूलन योजना भी प्रस्तावित है।

उच्च परिभाषा मल्टीमीडिया इंटरफ़ेस 2.0 (एचडीएमआई) रिसीवर और डिस्प्लेपोर्ट (डी.पी.) रिसीवर डिज़ाइन के लिए प्रति चैनल 5.4 जीबी / एस के लिए प्रति चैनल 6.0 जीबी / एस डाटा ट्रांसफर के लिए तुल्यकारक का उपयोग किया जाता है। 28 एन एम यू.टी.बी.बी.-एफ.डी.एस.ओ.आई. प्रौद्योगिकी में फैब्रिकेटेड, 0.06 मिमी सीटीएलई 30 मिली वाट का उपभोग करता है और ट्यूनेबल पीकिंग के 28 डीबी तक पहुंचता है।

पूरा रिसीवर चैनल 0.21 मिमी 2 पर कब्जा करता है, 55 मिली वाट का उपभोग करता है।
यह 6.0 जीबी / एस डेटा दर पर 9.2 पीजे / बिट की ऊर्जा दक्षता प्राप्त करता है। यह हाल ही में प्रकाशित कार्यों से बेहतर है। एचडीएमआई और डीपी के लिए हालिया प्रकाशनों के साथ एक विस्तृत तुलना प्रस्तुत की गई है। यह डिज़ाइन एचडीएमआई के लिए 10 मेगाहर्ट्ज तक 0.7 यू.आई. की जिटर सहिष्णुता और डीपी के लिए 0.42 यू.आई. तक 100 मेगाहर्ट्ज तक पहुंचता है। यह प्रदर्शन उनके संबंधित विनिर्देशों से बेहतर है।

एक पावर अनुकूलित ट्रांसमीटर के डिजाइन के लिए, रिसीवर सिग्नल वर्तमान से बिजली का पुनः उपयोग करने का प्रस्ताव है। एक खुले नाली ट्रांसमीटर में, दो रिसीवर समाप्ति रिसिटर में से एक से वर्तमान खींचकर संकेत प्राप्त किया जाता है। रिसीवर सिग्नल वर्तमान की फसल शक्ति के लिए खुले नाली ट्रांसमीटर को पुनः आर्किटेक्ट करने का प्रस्ताव है। यह रिसीवर सिग्नल वर्तमान ट्रांसमीटर के डिजिटल, एनालॉग और कस्टम डिजिटल सिग्नल सर्किट चलाने के लिए फिर से उपयोग किया जाता है। फसल का संकेत वर्तमान आपूर्ति आपूर्ति वोल्टेज बनाने के लिए किया जाता है जिसे एक शंट नियामक द्वारा नियंत्रित किया जाता है। ट्रांसमीटर पक्ष में कोई स्थानीय बिजली की आपूर्ति की आवश्यकता नहीं है। रिसीवर से मानक सिग्नलिंग के दौरान जो भी बिजली निकलती है, उसके अलावा कोई अतिरिक्त शक्ति नहीं ली जाती है। प्रस्तावित बिजली कटाई तकनीक का उपयोग करते हुए, एक शून्य पावर एचडीएमआई ट्रांसमीटर का डिजाइन 4.95 जीबी / एस डेटा दर में सक्षम है, यानि 1.65 जीबी / एस प्रति चैनल प्रस्तुत किया जाता है।

एक पावर ऑप्टिमाइज्ड ट्रांसमीटर के डिजाइन के लिए, रिसीवर सिग्नल से बिजली का पुनः उपयोग करने का प्रस्ताव है उच्च डेटा दरों पर, ट्रांसमीटर सर्किट द्वारा मांग की गई बिजली बढ़ जाती है और कटाई सिग्नल

पावर द्वारा नहीं मिल सकती है। स्थानीय ट्रांसमीटर आपूर्ति के साथ कटाई की आपूर्ति को बढ़ाकर शेष बिजली की आवश्यकता को पूरा किया जाता है। उत्पन्न स्रोतों को दो स्रोतों द्वारा समर्थित होने के बावजूद स्थिर बनाए रखा जाता है - रिसीवर सिग्नल और स्थानीय ट्रांसमीटर आपूर्ति से कटा हुआ प्रवाह। दो अलग-अलग आपूर्ति स्रोतों का प्रबंधन करने के लिए वास्तुकला, 18.0 जीबी / एस संचरण पर 0.9 पीजे / बिट की उच्च ऊर्जा दक्षता प्राप्त करने के लिए प्रस्तुत किया जाता है। एचडीएमआई 2.0 ट्रांसमीटर 28 एनएम यूटीबीबी-एफडीएसओआई प्रौद्योगिकी में डिजाइन किया गया था। स्थानीय आपूर्ति से बिजली की खपत डेटा दर के लिए अनुकूलित किया जाता है। चूंकि डेटा दर कम हो जाती है, स्थानीय ट्रांसमीटर आपूर्ति से ट्रांसमीटर की बिजली खपत शून्य हो जाती है।

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List of Abbreviations

ADC Analog-to-Digital Converters

BER Bit Error Rate

CDR Clock Data Recovery

CTLE Continuous-Time Linear Equalizers

DAC Digital to Analog Converter

DFE Decision Feedback Equalizers

DP DisplayPort (version 1.2a)

EA Error Amplifier

FDSOI Fully Depleted Silicon On Insulator

FIFO First In First Out

FIR Finite Impulse Response

HDMI High Definition Multimedia Interface

HPF High Pass Filter

ISI Inter-Symbol Interference

LMS Least Mean Squares (Algorithm)

PBGA Plastic Ball Grid Array (Package)

PCB Printed Circuit Board

PISO Parallel-In Serial-Out

PoR Power-on-Reset

PRBS Pseudo-Random Bit Sequence

PVT Process Voltage and Temperature

RMS Root Mean Square

Rx Receiver

RX Receiver

SDR Signal-to-Distortion Ratio

SLVS Scalable Low-Voltage Signaling

SNR Signal-to-Noise Ratio

SOC System-on-Chips

TMDS Transition Minimized Differential Signaling

Tx Transmitter

TX Transmitter

UHDTV Ultra-High-Definition Television

UI Unit Interval

USB Universal Serial Bus

UTBB Ultra-Thin Body and Buried Oxide

VESA Video Electronics Standards Association

VGA Variable Gain Amplifier

ZF Zero-Forcing (Algorithm)