

# **ACCURATE LOSS MODELLING FOR ACTIVE THERMAL CONTROL OF SiC CONVERTERS**

**DEBI PRASAD NAYAK**



**DEPARTMENT OF ELECTRICAL ENGINEERING  
INDIAN INSTITUTE OF TECHNOLOGY DELHI  
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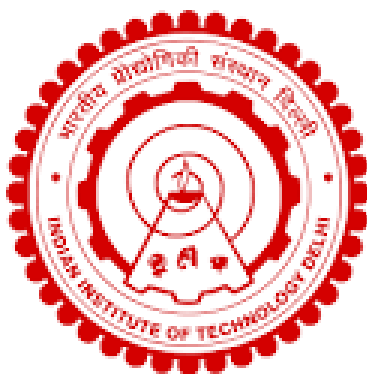
by

**DEBI PRASAD NAYAK**

DEPARTMENT OF ELECTRICAL ENGINEERING

Submitted

In fulfillment of the requirement of the Doctor of Philosophy  
to the



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## Dedication

*This thesis is dedicated to my parents  
Mr. Sukumar Nayak & Mrs. Sujata Nayak.*



# Thesis Certificate

This is to certify that the thesis titled "**ACCURATE LOSS MODELLING FOR ACTIVE THERMAL CONTROL OF SIC CONVERTERS**", submitted by **Debi Prasad Nayak, 2018EEZ8130**, to the Indian Institute of Technology, Delhi, for the award of the degree of **Doctor of Philosophy**, is a bonafide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Sumit Pramanick  
Associate Professor,  
Dept. of Electrical Engineering,  
Indian Institute of Technology, Delhi, 110 016.

Place: New Delhi, India.

Date: May 19, 2025.

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Debi Prasad Nayak

# Abstract

Index Terms: SiC MOSFET, SBD, double-pulse test, half-bridge, parasitic inductance, parasitic capacitance, reverse recovery, switching loss, junction temperature, analytical loss model, calorimetric measurement, on-state voltage measurement, active thermal control, inverter-based resource.

SILICON carbide MOSFETs are increasingly being accepted in the power electronics sector because of their exceptional physical and electrical properties, allowing them to function at higher switching frequencies. The increased switching transition rate and higher switching frequency of the SiC MOSFETs result in a greater influence of the circuit's parasitic elements on the switching profiles, leading to a considerable impact on the switching losses. Hence, precisely estimating the switching losses continues to be a challenging task. Further, loss estimation often aims to find the safe operating limit for power semiconductor devices as it remains the major design limitation; therefore, this also necessitates a simple yet accurate thermal model to estimate the junction temperature.

Therefore, this thesis begins with the motivation for modelling the switching loss of the SiC MOSFETs. Two often employed bridge leg configurations in power electronics are the Diode-MOSFET and MOSFET-MOSFET structures. This thesis primarily focuses on the latter arrangement to develop a loss model based on datasheet parameters, aiming to estimate temperature-dependent switching losses resulting from the reverse recovery charge of the anti-parallel body diode in SiC MOSFETs. In addition, the developed model considers the parasitic components' effects, allowing for a comprehensive knowledge of the switching characteristics of the SiC MOSFETs in various operating conditions. Subsequently, the accuracy of the proposed loss model has been verified by comparing its result with the state-of-the-art double pulse test and calorimetric test results.

In terms of junction temperature estimation, direct measurement is not practical, and indirect non-invasive methods such as temperature-sensitive electrical parameters-based measurement techniques require substantial effort in building and calibrating the sensing circuits. Therefore, an electro-thermal model has been de-

veloped, where an RC network-based thermal model has been implemented, which takes the power loss data from the developed loss model and iteratively returns the junction temperature. The effectiveness of the proposed method has been demonstrated by comparing its results with the conventional and on-state drain-source voltage measurement-based TSEP estimation techniques on a 10kW three-phase interleaved boost converter.

Subsequently, the opportunity to increase the kVA limit of a power electronic converter without breaching the safe operating limit of the junction temperature through the active thermal control technique has been explored. Wherein the applicability of the earlier discussed electro-thermal model for active thermal control is also shown. In the presented active thermal control approach, a discontinuous pulse width modulation strategy, which controls the bus clamp angle according to the virtual junction temperature feedback for increasing the kVA limit of the grid-connected inverter-based resources, is discussed. The impact of a system-level current controller for the kVA increment has also been briefed. Additionally, the effect of DPWM on switching losses  $P_{sw}$  is shown by establishing an analytical relationship between the bus clamp angle with respect to switching loss.

In conclusion, the main contribution of the thesis regarding temperature-dependent loss modelling, junction temperature estimation, and control through active thermal control techniques for SiC converters is summarised, and a brief outlook on possible future research work is discussed.

## संक्षेप

सूचकांक शर्तें: सिलिकॉन कार्बाइड मोसफेट, शॉटकी बैरियर डायोड, डबल-पल्स परीक्षण, अर्ध-ब्रिज लेग, पैरासिटिक प्रेरकत्व, पैरासिटिक धारिता, रिवर्स रिकवरी, स्विचिंग ऊर्जा क्षय, जंक्शन तापमान, विश्लेषणात्मक हानि मॉडल, कैलोरीमेट्रिक माप, ऑन-स्टेट वोल्टेज मापन सक्रिय थर्मल नियंत्रण, इन्वर्टर-आधारित संसाधन।

सिलिकॉन कार्बाइड मोसफेट को उनके असाधारण भौतिक और विद्युत गुणों के कारण पावर इलेक्ट्रॉनिक्स क्षेत्र में तेजी से स्वीकार किया जा रहा है, जिससे उन्हें उच्च स्विचिंग आवृत्तियों पर कार्य करने की अनुमति मिलती है। सिलिकॉन कार्बाइड मोसफेट की बढ़ी हुई स्विचिंग परिवर्तन दर और उच्च स्विचिंग आवृत्ति के परिणामस्वरूप स्विचिंग प्रोफाइल पर सर्किट के पैरासिटिक तत्वों का अधिक प्रभाव पड़ता है, जिससे स्विचिंग ऊर्जा क्षय पर काफी प्रभाव पड़ता है। इसलिए, स्विचिंग ऊर्जा क्षय का सटीक अनुमान लगाना एक चुनौतीपूर्ण कार्य बना हुआ है। इसके अलावा, ऊर्जा क्षय अनुमान का उद्देश्य अक्सर पावर सेमीकंडक्टर उपकरणों के लिए सुरक्षित संचालन सीमा का पता लगाना होता है क्योंकि यह प्रमुख डिज़ाइन सीमा बनी हुई है; इसलिए, जंक्शन तापमान का अनुमान लगाने के लिए एक सरल लेकिन सटीक थर्मल मॉडल की भी आवश्यकता होती है।

इसलिए, यह शोध प्रबन्ध सिलिकॉन कार्बाइड मोसफेट के स्विचिंग ऊर्जा क्षय के मॉडलिंग की प्रेरणा से शुरू होती है। पावर इलेक्ट्रॉनिक्स में दो अक्सर इस्तेमाल किए जाने वाले ब्रिज लेग कॉन्फिगरेशन डायोड-मोसफेट और मोसफेट-मोसफेट संरचना हैं। यह शोध प्रबन्ध मुख्य रूप से डेटाशीट मापदंडों के आधार पर, मोसफेट-मोसफेट संरचनाएँ के ऊपर एक सटीक स्विचिंग ऊर्जा क्षय मॉडल विकसित करने पर केंद्रित है, जिसका उद्देश्य सिलिकॉन कार्बाइड मोसफेट में एंटी-पैरेलल बॉडी डायोड के रिवर्स रिकवरी चार्ज से उत्पन्न तापमान-निर्भर स्विचिंग ऊर्जा क्षय का अनुमान लगाना है। इसके अलावा, विकसित मॉडल वैद्युत पैरासिटिक घटकों के प्रभावों पर विचार करता है, जिससे विभिन्न सकारक स्थितियों में सिलिकॉन कार्बाइड मोसफेट की स्विचिंग विशेषताओं के बारे में व्यापक ज्ञान प्राप्त होता है। इसके बाद, प्रस्तावित ऊर्जा क्षय मॉडल की सटीकता को अत्याधुनिक डबल पल्स टेस्ट और कैलोरीमेट्रिक परीक्षण परिणामों के साथ तुलना करके मान्य किया गया है।

जंक्शन तापमान अनुमान के संदर्भ में, प्रत्यक्ष माप उपयोगी नहीं है, और तापमान-आश्रित विद्युत मापदंडों-आधारित माप तकनीको जैसे अप्रत्यक्ष अनवासीता तरीको को सेंसिंग सर्किट बनाने और कैलिब्रेट करने में पर्याप्त प्रयास की आवश्यकता होती है। इसलिए, एक इलेक्ट्रो-थर्मल मॉडल विकसित किया गया है, जहां एक आर-सी नेटवर्क-आधारित थर्मल मॉडल लागू किया गया है, जो विकसित ऊर्जा क्षय मॉडल से वैद्युत ऊर्जा क्षय डेटा लेता है और जंक्शन तापमान को पुनरावृत्त रूप से लौटाता है। प्रस्तावित विधि की प्रभावशीलता को १० किलोवाट तीन-चरण इंटरलीव्ड बूस्ट कनवर्टर पर पारंपरिक और ऑन-स्टेट ड्रेन-सोर्स वोल्टेज माप-आधारित टीएसईपी अनुमान तकनीको के साथ इसके परिणामों की तुलना करके प्रदर्शित किया गया है।

इसके बाद, सक्रिय थर्मल नियंत्रण तकनीक के माध्यम से जंक्शन तापमान की सुरक्षित परिचालन सीमा का उल्लंघन किए बिना एक पावर इलेक्ट्रॉनिक कन्वर्टर की किलोवोल्टऐम्पियर सीमा को बढ़ाने का अवसर तलाशा गया है। जिसमें सक्रिय थर्मल नियंत्रण के लिए पहले चर्चा किए गए इलेक्ट्रो-थर्मल मॉडल की प्रयोज्यता भी दिखाई गई है। प्रस्तुत सक्रिय थर्मल नियंत्रण दृष्टिकोण में, एक डिस्कन्टीन्यूस पल्स विड्थ मॉड्यूलेशन रणनीति, जो ग्रिड-कनेक्टेड इन्वर्टर-आधारित संसाधनों की किलोवोल्टऐम्पियर सीमा को बढ़ाने के लिए कल्पित जंक्शन तापमान प्रतिक्रिया के अनुसार बस-क्लैप कोण को नियंत्रित करती है, पर चर्चा की गई है। किलोवोल्ट ऐम्पियर वृद्धि के लिए सिस्टम-स्तरीय विद्युत प्रवाह नियंत्रक के प्रभाव को भी संक्षिप्त रूप से बताया गया है। इसके अतिरिक्त, स्विचिंग ऊर्जा क्षय पर डिस्कन्टीन्यूस पल्स विड्थ मॉड्यूलेशन के प्रभाव को स्विचिंग ऊर्जा क्षय के संबंध में बस क्लैप कोण के बीच एक विश्लेषणात्मक संबंध स्थापित करके दिखाया गया है।

निष्कर्ष में, तापमान पर निर्भर ऊर्जा क्षय मॉडलिंग, जंक्शन तापमान आकलन, और सिलिकॉन कार्बाइड कन्वर्टर के लिए सक्रिय थर्मल नियंत्रण तकनीको के माध्यम से नियंत्रण के संबंध में यह शोध प्रबन्ध के मुख्य योगदान को संक्षेप में प्रस्तुत किया गया है, और संभावित भविष्य के शोध कार्य पर एक संक्षिप्त दृष्टिकोण पर चर्चा की गई है।

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# Acronyms

|        |                                                   |
|--------|---------------------------------------------------|
| AC     | Alternating Current                               |
| AGD    | Active Gate Driving                               |
| ATC    | Active Thermal Control                            |
| CHB    | Cascaded H-Bridge                                 |
| CT     | Calorimetric Test                                 |
| DC     | Direct Current                                    |
| DPT    | Double Pulse Test                                 |
| DPWM   | Discontinuous Pulse Width Modulation              |
| DUT    | Device Under Test                                 |
| EV     | Electric Vehicles                                 |
| EMC    | Electromagnetic Compatability                     |
| EMF    | Electromotive Force                               |
| EMI    | Electromagnetic Interference                      |
| ESL    | Equivalent Series Inductance                      |
| ESR    | Equivalent Series Resistance                      |
| FEA    | Finite Element Analysis                           |
| FEM    | Finite Element Method                             |
| GaN    | Gallium Nitride                                   |
| IBR    | Inverter Based Resources                          |
| IGBT   | Insulated Gate Bipolar Transistor                 |
| IITD   | Indian Institute of Technology, Delhi             |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| NPC    | Neutral Point Clamped                             |
| OVMC   | On-State Voltage Measurement Circuit              |
| PCB    | Printed Circuit Board                             |
| PEC    | Power Electronic Converter                        |
| PF     | Power Factor                                      |
| PV     | Photovoltaic                                      |
| PWM    | Pulse Width Modulation                            |
| RMS    | Root Mean Square                                  |
| SBD    | Schottky Barrier Diode                            |
| Si     | Silicon                                           |

---

|       |                                             |
|-------|---------------------------------------------|
| SiC   | Silicon Carbide                             |
| SOA   | Safe Operating Area                         |
| SOH   | State of Health                             |
| SPWM  | Sine Pulse Width Modulation                 |
| SVPWM | Space Vector Pulse Width Modulation         |
| TCT   | Transient Calorimetric Test                 |
| TEC   | Thermo Electric Cooling                     |
| TIM   | Thermal Interface Material                  |
| TSEP  | Temperature Sensitive Electrical Parameters |
| VSI   | Voltage Source Inverter                     |
| VSC   | Voltage Source Converter                    |
| WBG   | Wide Band Gap                               |

## Notation

|                       |                                            |
|-----------------------|--------------------------------------------|
| $\alpha$              | Clamp angle                                |
| $\phi$                | Phase angle                                |
| $\rho$                | Density                                    |
| $\kappa$              | Thermal conductivity                       |
| $\tau_c$              | Charge carrier life time                   |
| $\tau_{rr}$           | Time constant of decay fall                |
| $\Delta I_{Ln}$       | Inductor ripple current                    |
| $\Delta T_j$          | Thermal cycling                            |
| $dI_d/dt$             | Rate of rise of drain current              |
| $dV_{ds}/dt, dV_d/dt$ | Rate of rise of drain-source voltage       |
| $dV_{gs}/dt$          | Rate of rise of gate-source voltage        |
| $c_p$                 | Specific heat capacity                     |
| $C_{ak}$              | Parasitic capacitance across SiC SBD       |
| $C_{ds}$              | Drain-source capacitance                   |
| $C_{gd}$              | Gate-drain capacitance                     |
| $C_{gs}$              | Gate-source capacitance                    |
| $C_{iss}$             | Input capacitance                          |
| $C_j$                 | Parasitic capacitance across body diode    |
| $C_l$                 | Parasitic capacitance of the load          |
| $C_{oss}$             | Output capacitance                         |
| $C_{out}$             | Filter capacitance                         |
| $C_{rss}$             | Reverse transfer capacitance               |
| $E_j$                 | Stored energy in the parasitic capacitance |
| $E_{off}$             | Turn-off energy loss                       |
| $E_{on}$              | Turn-on energy loss                        |
| $E_{rr}$              | Reverse recovery loss                      |
| $E_{sw}$              | Switching energy loss                      |
| $E_{tot}$             | Total energy loss                          |
| $f_{sw}$              | Switching frequency                        |
| $g_m$                 | Trans conductance                          |
| $i_d$                 | Direct axis current                        |
| $i_{ph}$              | Phase current                              |
| $i_q$                 | Quadrature axis current                    |
| $I_d$                 | Drain current                              |
| $I_g$                 | Peak gate current                          |
| $I_{in}$              | Input current                              |
| $I_{lk}$              | Diode leakage current                      |
| $I_{load}$            | Load current                               |
| $I_m$                 | Peak phase current                         |

---

|                  |                                                               |
|------------------|---------------------------------------------------------------|
| $I_{rr}$         | Reverse recovery current                                      |
| $I_{rr}^*$       | Actual reverse recovery current                               |
| $i_{ch}, I_{ch}$ | MOSFET channel current                                        |
| $I_C, I_{cj}(t)$ | Parasitic output capacitance displacement current             |
| $k_f$            | Multiplication factor                                         |
| $L_b$            | DC bus parasitic inductance                                   |
| $L_d$            | Drain lead inductance                                         |
| $L_n$            | Inductive filter per phase                                    |
| $L_s$            | Source lead inductance                                        |
| $L_p, L_{bus}$   | $L_b + L_d + L_s$                                             |
| $m_{abc}$        | Modulating signal                                             |
| $P$              | Real power                                                    |
| $P_o$            | Output power                                                  |
| $P_{cond}$       | Conduction loss                                               |
| $P_{loss}$       | Power loss                                                    |
| $P_{sw}$         | Switching loss                                                |
| $Q$              | Reactive power                                                |
| $Q_{rr}$         | Total reverse recovery charge including the capacitive charge |
| $Q_{rr}^*$       | Actual reverse recovery charge                                |
| $Q_{cj}, Q_c$    | Capacitive charge                                             |
| $Q_1, Q_2$       | Top and bottom device in a half-bridge                        |
| $R_b$            | DC bus parasitic resistance                                   |
| $R_{ds,on}$      | On-state drain-source resistance                              |
| $R_{ds,25}^o$    | On-state drain-source resistance at 25°C                      |
| $R_{DS}$         | On-state drain-source resistance                              |
| $R_g$            | Gate resistance                                               |
| $R_{jc}$         | Junction to case thermal resistance                           |
| $t_{db}$         | Dead-band or dead-time                                        |
| $t_{d,on}$       | Turn-on delay time                                            |
| $t_{d,off}$      | Turn-off delay time                                           |
| $T_c$            | Case temperature                                              |
| $T_j$            | Junction temperature                                          |
| $T_m$            | Drift region transit time                                     |
| $T_{hs}, T_s$    | Heatsink temperature                                          |
| $T_{amb}, T_a$   | Ambient temperature                                           |
| $V_{dc}$         | DC bus voltage                                                |
| $V_{ds}$         | Drain-source voltage                                          |
| $V_{fd}$         | Diode forward voltage drop                                    |
| $V_{off}$        | Offset voltage                                                |
| $V_{th}$         | Gate threshold voltage                                        |
| $V_{ds,m}$       | Sensed on-state drain-source voltage                          |
| $V_{ds,on}$      | On-state drain-source voltage                                 |
| $V_{g,pl}$       | Gate plateau voltage                                          |
| $V_{EE}, V_{cc}$ | Negative and positive gate voltage                            |

---

|                   |                                              |
|-------------------|----------------------------------------------|
| $V_{in}, V_{out}$ | Input and output voltage                     |
| $Z_{th,jc}$       | Junction to case transient thermal impedance |