SPINTRONICS-BASED NEUROMORPHIC COMPUTING: NEW DEVICES AND ARCHITECTURES

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By

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Dedicated to

My parents and siblings

CERTIFICATE

This is to certify that the thesis titled **Spintronics-Based Neuromorphic Computing: New Devices and Architectures**, being submitted by Ms. **Upasana Sahu** for the award of the degree of Doctor of Philosophy in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of original research work carried out by her under our supervision and guidance. The results presented in this thesis have not been submitted for the award of any other degree or diploma. We consider her research work substantial enough for the award of the doctorate degree.

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ABSTRACT

This thesis presents the study, design, and implementation of neural networks using spintronic devices. The first part of this thesis focuses on the spiking neural network, a novel neural-network architecture which is inspired by brain. Spiking Neural Network (SNN) has been shown to consume very low power for an inference task, i.e., forward computation on the test data with a pre-trained model. However, training of such SNN has remained a challenge. In this thesis, Spike-Time-Dependent-Plasticity-based (STDP) learning has been used to train the SNN through implementation on an analog hardware using spintronic devices (on-chip learning).

Here, I design and simulate the synapses and neurons in the analog hardware using a combination of ferromagnetic-metal-heavy-metal-based spintronic devices and transistor-based electronic circuits. The spintronic devices have been modeled through micromagnetics and the circuits through SPICE, with the spintronic-device models incorporated inside SPICE as Verilog A modules. Two different modes have been used for the training/ learning: completely unsupervised learning and partially supervised learning (both STDP-enabled but with different level of control over spiking of the output-stage neurons or post-neurons). High classification accuracy is obtained on the popular Fisher's Iris data set of flowers, for both modes of learning.

Next, the SNN is trained on the MNIST data set of handwritten digits. The architecture used by me has less number of network layers that used previously for MNIST classification. Finally, the time and total energy consumed in the designed synapse circuits, to enable the learning, have been reported.

In the later part of the thesis, a ferrimagnetic domain-wall synapse device has been proposed as an alternative to a ferromagnetic domain-wall synapse device for faster and more

energy-efficient on-chip learning on a crossbar-array-based analog-hardware neural network, which uses such synapse devices.Using micromagnetics, domain-wall motion has been modeled for a Co-Gd-bilayer-based device, in which ferrimagnetic-domain-wall motion has been reported experimentally earlier. Then, this domain-wall-based spintronic device model has been incorporated, as a Verilog A module, in the SPICE design of a crossbar-array-based fully connected neural network (FCNN), for each synapse in the crossbar array. It is shown that for the same duration of current pulses needed to move the domain wall and update the synaptic weight for on-chip learning, total energy consumption in the synapses for on-chip learning is five times (5X) lower in the ferrimagnetic-synapse-based FCNN compared to the ferromagnetic-synapse-based FCNN. Similarly, for the same amount of energy consumed for learning, time taken for on-chip learning is five times (5X) lower for the the ferrimagnetic-synapse-based FCNN compared to the ferromagnetic-synapse-based FCNN. Both these results are a consequence of faster domain-wall motion in the ferrimagnetic device compared to the ferromagnetic device.

KEYWORDS: Spiking neural network, on-chip learning, spike time dependent plasticity (STDP), spintronics, spin-orbit torque, ferromagnetic domain-wall device, ferrimagnetic domain-wall device

सार

यह थीसिस स्पिंट्रोनिक उपकरणों का उपयोग करके तंत्रिका नेटवर्क के अध्ययन, डिजाइन और कार्यान्वयन को प्रस्तुत करती है। इस थीसिस का पहला भाग स्पाइकिंग न्यूरल नेटवर्क पर केंद्रित है, एक उपन्यास न्यूरल-नेटवर्क आर्किटेक्चर जो मस्तिष्क से प्रेरित है। स्पाइकिंग न्यूरल नेटवर्क (एसएनएन) को एक अनुमान कार्य के लिए बहुत कम बिजली की खपत करने के लिए दिखाया गया है, यानी, पूर्व-प्रशिक्षित मॉडल के साथ परीक्षण डेटा पर आगे की गणना। हालांकि, ऐसे एसएनएन का प्रशिक्षण एक चुनौती बना हुआ है। इस थीसिस में, स्पाइक-टाइम-डिपेंडेंट प्लास्टिसिटी-आधारित (एसटीडीपी) लर्निंग का उपयोग एसएनएन को स्पिंट्रोनिक डिवाइस (ऑन-चिप लर्निंग) का उपयोग करके एनालॉग हार्डवेयर पर कार्यान्वयन के माध्यम से प्रशिक्षित करने के लिए किया गया है।

यहां, मैं फेरोमैग्नेटिक-मेटल-हैवी-मेटल-आधारित स्पिंट्रोनिक उपकरणों और ट्रांजिस्टर-आधारित इलेक्ट्रॉनिक सर्किट के संयोजन का उपयोग करके एनालॉग हार्डवेयर में सिनेप्स और न्यूरॉन्स को डिजाइन और अनुकरण करता हूं। स्पिंट्रोनिक उपकरणों को माइक्रोमैग्नेटिक्स और स्पाइस के माध्यम से सर्किट के माध्यम से तैयार किया गया है, जिसमें स्पाइस के अंदर वेरिलोग ए मॉड्यूल के रूप में शामिल स्पिंट्रोनिक-डिवाइस मॉडल शामिल हैं। प्रशिक्षण/सीखने के लिए दो अलग-अलग तरीकों का उपयोग किया गया है: पूरी तरह से अनुपयोगी शिक्षण और आंशिक रूप से पर्यवेक्षित शिक्षण (दोनों एसटीडीपी-सक्षम लेकिन आउटपुट-स्टेज न्यूरॉन्स या पोस्ट-न्यूरॉन्स के स्पाइकिंग पर नियंत्रण के विभिन्न स्तर के साथ)। सीखने के दोनों तरीकों के लिए लोकप्रिय फिशर के आइरिस डेटा सेट पर उच्च वर्गीकरण सटीकता प्राप्त की जाती है।

इसके बाद,एसएनएन को हस्तलिखित अंकों के एम.एन.आई.एस.टी डेटा सेट पर प्रशिक्षित किया जाता है। मेरे द्वारा उपयोग किए गए आर्किटेक्चर में नेटवर्क परतों की संख्या कम है जो पहले एम.एन.आई.एस.टी वर्गीकरण के लिए उपयोग की जाती थी। अंत में, सीखने को सक्षम करने के लिए डिज़ाइन किए गए सिनैप्स सर्किट में खपत समय और कुल ऊर्जा की सूचना दी गई है।

थीसिस के बाद के हिस्से में, एक क्रॉसबार-सरणी-आधारित एनालॉग-हार्डवेयर पर तेज़ और अधिक ऊर्जा-कुशल ऑन-चिप सीखने के लिए एक फेरोमैग्नेटिक डोमेन-वॉल सिनैप्स डिवाइस के विकल्प के रूप में एक फेरिमैग्नेटिक डोमेन-वॉल सिनैप्स डिवाइस प्रस्तावित किया गया है। तंत्रिका नेटवर्क, जो ऐसे सिनैप्स उपकरणों का उपयोग करता है। माइक्रोमैग्नेटिक्स का उपयोग करते हुए, डोमेन-वॉल मोशन को सह-जीडी-बिलेयर-आधारित डिवाइस के लिए तैयार किया गया है, जिसमें फेरिमैग्नेटिक-डोमेन-वॉल मोशन को प्रयोगात्मक रूप से पहले बताया गया है। फिर, इस डोमेन-दीवार-आधारित स्पिंट्रोनिक डिवाइस मॉडल को क्रॉसबार सरणी में प्रत्येक सिंक के लिए, एक क्रॉसबार-सरणी-आधारित पूरी तरह से जुड़े तंत्रिका नेटवर्क (एफसीएनएन) के स्पाइस डिज़ाइन में वेरिलोग ए मॉड्यूल के रूप में शामिल किया गया है। यह दिखाया गया है कि डोमेन दीवार को स्थानांतरित करने और ऑन-चिप सीखने के लिए सिनैप्टिक वजन को अद्यतन करने के लिए आवश्यक वर्तमान दालों की समान अवधि के लिए,ऑन-चिप सीखने के लिए सिनेप्स में कुल ऊर्जा खपत फेरिमैग्नेटिक में पांच गुना कम है- फेरोमैग्नेटिक-सिनैप्स-आधारित एफसीएनएन की तुलना में सिनैप्स-आधारित एफसीएनएन। इसी तरह, सीखने

के लिए खपत की गई ऊर्जा की समान मात्रा के लिए, ऑन-चिप सीखने में लगने वाला समय फेरोमैग्नेटिक-सिनैप्स-आधारित एफसीएनएन की तुलना में फेरिमैग्नेटिक-सिनैप्स-आधारित एफसीएनएन के लिए पांच गुना कम है। ये दोनों परिणाम फेरोमैग्नेटिक डिवाइस की तुलना में फेरिमैग्नेटिक डिवाइस में तेज डोमेन-वॉल मोशन का परिणाम हैं।

Papers related to the thesis

1. Upasana Sahu, Aadit Pandey, Kushaagra Goyal, and Debanjan Bhowmik. "Spike time dependent plasticity (STDP) enabled learning in spiking neural networks using domain wall based synapses and neurons." *AIP Advances* 9, no. 12 (2019): 125339.

2. Upasana Sahu, Kushaagra Goyal, Utkarsh Saxena, Tanmay Chavan, Udayan Ganguly, and Debanjan Bhowmik. "Skyrmionic implementation of Spike Time Dependent Plasticity (STDP) enabled Spiking Neural Network (SNN) under supervised learning scheme." *In 2018 4th IEEE International Conference on Emerging Electronics (ICEE)*, pp. 1-6. IEEE, 2018.

3. Upasana Sahu, Kushaagra Goyal, and Debanjan Bhowmik. "Training of a Spiking Neural Network on spintronics based analog hardware for handwritten digit recognition." in *In 2020 5th IEEE International Conference on Emerging Electronics (ICEE)*, 2020.

4. Upasana Sahu , Naveen Sisodia, Janak Sharda, Pranaba Kishor Muduli, Debanjan Bhowmik, "Ferrimagnetic Synapse Devices for Fast and Energy-Efficient On-Chip Learning on An Analog-Hardware Neural Network." IEEE Transactions on Electron Devices 69, no. 4 (2022): 1713–1720

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ABBREVIATIONS

AMR	Anisotropic Magneto-Resistance
ALU	Arithmetic and Logic Unit
AI	Artificial Intelligence
CoFe	Cobalt Iron
CMOS	Complement Metal Oxide Semiconductor
DW	Domain Wall
DRAM	Dynamic Random Access Memory
DMI	Dzyaloshinskii Moriya Interaction
FM	Ferromagnet
FCNN	Fully Connected Neural Network
GMR	Giant Magneto-resistance
HDD	Hard Disk Drive
HM	Heavy Metal
HH	Hodgkin-Huxley
IF	Integrate-and-Fire
LLG	Landau-Lifshitz-Gilbert
LIF	Leaky Integrate Fire
ML	Machine Learning
MgO	Magnesium Oxide
MRAM	Magnetic Random Access Memory
MTJ	Magnetic Tunnel Junction
MOS	Metal Oxide Semiconductor
MNIST	Modified National Institute of Standards and Technology

NN	Neural Network
PMA	Perpendicular Magnetic Anisotropy
PCM	Phase Change Memory
Pt	Platinum
PDK	Process Design Kit
RBF	Radial Basis Functions
RAM	Random Access Memory
RRAM	Resistive Memory
SNN	Spiking Neural Network
STDP	Spike Time Dependent Plasticity
SOT	Spin Orbit Torque
STT	Spin Transfer Torque
SSD	Solid State Drive
SRAM	Static Random Access Memory
TMR	Tunneling Magneto-Resistance Ratio
WTA	Winner Takes All

NOTATION

α	Damping ratio
A	Exchange correlation constant
Δw	Change in weight of the synapse
ΔG	Change in conductance
Δt	Difference between t_{post} and t_{pre}
e	Electronic charge
E_L	Resting potential of neuron
G_L	Membrane conductance
G_{max}	Maximum conductance of the MTJ
G_{min}	Minimum conductance of the MTJ
h	Planck's constant
J_s	Spin current density
J_c	Charge current density
K	Perpendicular Magnetic Anisotropy (PMA) constant
Ms	Saturation magnetization
m_{Co}	Magnetic moment of Co
m_{Gd}	Magnetic moment of Gd
$m_{Co}^{T=0}$	Magnetic moment of the Co layer at 0 K
$m_{Gd}^{T=0}$	Magnetic moment of the Gd layer at 0 K.
θ_{SH}	Spin hall angle
t_{pre}	Time when the pre-neuron spikes
T_{Co}^{c}	Curie temperature of Co
T_{Gd}^{c}	Curie temperature of Gd
t_{post}	Time when the post-neuron spikes
τ	Time constant for the synapse
μ_0	Permeability of vacuum
γ	Gyro-magnetic ratio
Γ	Proportionality constant of synapse
V_{th}	Threshold potential of neuron
V_{sg}	Source-gate voltage of Transistor.
ξ_{Co}	Exponential parameter describing the temperature dependence for the Co layer
ξ_{Gd}	Exponential parameter describing the temperature dependence for the Gd layer