

SOME STUDIES ON BIPOLAR SYNCHRONIZATION SCHEMES

NAND KUMAR

Thesis submitted to the
Indian Institute of Technology, Delhi
for the award of the degree of

DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, DELHI
NEW DELHI - 110016

NOVEMBER, 1988

(Errors like straw on the surface flow,
One who is in search of truth must dive below)

Dedicated

to

Shri Narayan Prasad (father)

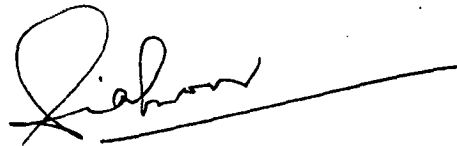
and

Shri Anilesh Kumar (brother)

who always have been the source of inspiration
during my entire academic career.

CERTIFICATE

This is to certify that the thesis entitled, "Some Studies on Bipolar Synchronization Schemes", being submitted by Shri Nand Kumar for the award of the degree of Doctor of Philosophy to the Indian Institute of Technology, Delhi, is a record of the original bonafide research work carried out by him under my guidance and supervision. The results contained in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.



(Prof. S.I. Ahson)

Department of Electrical Engineering
Indian Institute of Technology
New Delhi-110016

श्री नन्द कुमार (D)EIL



ACKNOWLEDGEMENT

It deems to be an order of privilege for me to have worked under the erudite guidance of Dr. S.I. Ahson, Professor of the Electrical Engineering Department, Indian Institute of Technology, Delhi. I express my deep sense of gratitude to Prof. Ahson for his able guidance, keen interest, helpful suggestions and fruitful discussions throughout the entire period of research in this field. I also extend my sincere thanks to my caretaker supervisor Dr. S. S. Jamuar, Asst. Professor of the Electrical Engineering Department, who had helped me in various ways in my life and in my studies when Prof. Ahson was abroad.

I express my profound gratefulness to Dr.(Mrs.) Kum Kum Garg of Roorkee University for her assistance in shaping my ideas in the field of Petri nets. I am also thankful to Prof. N. Viswanadham and Dr. Y. Narahari (I.I.Sc. Bangalore) and other authors from abroad for extending their help in many ways.

The moral support extended by my senior officers like Shri K. Ramanathan (Director), Dr.(Mrs.) N. Chopra (System Supervisor), Dr. P.K. Gupta, Shri S.R. Prabhas and Shri P.D. Ubale from Central Electricity Authority, New Delhi can also not to be forgotten. Special thanks are due to Shri V.C. Jain, System Supervisor, Computer Services Directorate, CEA and Shri R.C. Thakur, Microprocessor Application Programme (MAP), I.I.T. Delhi for fruitful discussions for different topics of the thesis.

At last, but not the least, I am also thankful to the faculty and staff of Elect. Engg. Dept., Computer Science and Engg. Dept., and Computer Services Centre of IIT Delhi, for their help in my studies. I express my thanks to Shri S.K. Shrivastava, Deputy Director, CWC for the pains taken by him in the proof reading of the final draft. Thanks are also due to Shri. A.P. Sharma (CEA) for the art work and Shri Fateh Singh

(IIT Delhi), Shri B. Shrivastava (CWC) and M/s Eagle Computer Centre (New Delhi) for their immense help in the excellent typing of this thesis.

In the end, I want to express my sincere thanks to my wife (Mrs. Chanda Rani), my son (Master Sunny) and my daughter (Miss Snigdha) for bearing with me in the many odd hours during the period of this research work.

Nand Kumar

IIT DELHI .

(NAND KUMAR)

ABSTRACT

The aim of the research work reported in this thesis is to provide additional insight into the theory of bipolar synchronization schemes (bp schemes), and to show (i) its application in **modelling** of distributed processing systems, (ii) **Logical analysis** of the scheme under study, and (iii) its usefulness in **performance evaluation** of systems.

The theory of bp schemes is based on Petri nets and is oriented towards synthesis of well behaved systems. We critically examine the synthesis rules proposed by Genrich and Thiagarajan and extend them to accommodate the 'interface nodes' for modelling interaction with the environment. We propose 'communication modules' and show how to construct these modules using our synthesis rules. We represent semaphore, mutual exclusion and resource guardian constructs using our communication modules. Some of these constructs are employed to model the dining philosophers problem and the Ballistic Missile Defence (BMD) system.

The notion of 'well behavedness' is the key issue in the theory of bp schemes. We propose new techniques for verification of well behavedness using 'net transformation' and 'reachability graph'. The latter is also used to detect 'deadlock' in bp schemes. Our "arc numbering system" is a new method to partition a bp scheme into its V-components which is useful in consistent data allocation of bp schemes. We also consider "fairness" in bp schemes.

Besides modelling application and logical analysis, we extend the applicability of bp schemes to performance evaluation. We provide a new interpretation to bp schemes by associating the notion of 'time' and 'branching probability' with the choices made between alternative

courses of actions. The concept of Moment Generating Function (MGF) of the probability distribution function associated with bp schemes is exploited to derive useful performance indices like mean and variance. The quantitative results presented in the thesis also include an integral approach towards analysis of large and complex bp schemes using decomposition and reduction techniques. We consider a typical Flexible Manufacturing System (FMS) for performance analysis.

Further research work to reinforce the results and ideas given in the thesis is suggested. The thesis also includes comprehensive reviews on Petri nets and bipolar synchronization schemes.

TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENT	i
ABSTRACT	iii
CHAPTER 1 INTRODUCTION	
1.1 MOTIVATION	1
1.2 SCOPE OF THE THESIS	2
1.3 THESIS ORGANIZATION	4
CHAPTER 2 REVIEW OF PETRI NETS AND BP SCHEMES	
2.1 INTRODUCTION	7
2.2 CONDITION/EVENT SYSTEMS	8
2.2.1 Condition/Event-net	9
2.2.2 Condition/Event System	10
2.2.3 Liveness and Case Graphs	11
2.3 PLACE/TRANSITION NETS	13
2.3.1 Petri Nets	13
2.3.2 Pure Petri net	16
2.3.3 Properties and Analysis Techniques of Petri nets	16
2.3.3.1 Reachability	17
2.3.3.2 Coverability	17
2.3.3.3 Boundedness	17
2.3.3.4 Safeness (or safety)	17
2.3.3.5 Liveness	18

2.3.4 Analysis Techniques	18
2.3.4.1 Reachability Tree	18
2.3.4.2 Linear Algebraic Technique	19
2.3.5 Validation of Properties of Petri net based models	19
2.3.5.1 S-invariant	20
2.3.5.2 T-invariant	20
2.4 STATE MACHINES AND MARKED GRAPHS	20
2.4.1 State Machines	21
2.4.2 Marked Graphs	21
2.5 FREE CHOICE NETS	23
2.6 PREDICATE/TRANSITION NETS	24
2.7 TIMED AND STOCHASTIC PETRI NETS	26
2.8 BIPOLAR SYNCHRONIZATION SCHEMES	28
2.8.1 Evolution of Bp Schemes	28
2.8.2 An Informal View	29
2.8.3 Formal Model	30
2.8.4 Well Behaved Bp Schemes	34
2.8.5 Synthesis Procedure	35
2.8.5.1 Transformation Rules	37
2.8.5.2 Well Formed Bp Schemes	41
2.8.5.3 Reduction Rules	41
2.8.6 Interpreted Bp Schemes	45
2.9 CONCLUSION	47

CHAPTER 3 MODELLING APPLICATIONS OF BP SCHEMES

3.1	INTRODUCTION	48
3.2	DISTRIBUTED SYSTEMS	49
3.2.1	Computer Communication Protocol	50
3.2.2	A Concurrent Addition Problem	52
3.3	SYNTHESIS RULE FOR INTERFACE NODES	52
3.4	COMMUNICATION AND SYNCHRONIZATION IN DISTRIBUTED SYSTEMS	58
3.4.1	Communication and Synchronization	58
3.4.2	Communication Modules	60
3.4.2.1	Bp Scheme Models for Communication Modules	61
3.4.2.2	Synthesis of Communication Modules	64
3.4.2.3	Interconnection of Communication Modules	64
3.5	BP SCHEME MODELS FOR SYNCHRONIZATION PROBLEM	71
3.5.1	Model for Mutual Exclusion	71
3.5.2	Bp Scheme for Dining Philosophers Problem	74
3.5.2.1	Resource Guardian	74
3.5.2.2	Dining Philosophers Problem	76
3.6	BP SCHEME MODEL FOR BMD SYSTEM	80
3.7	CONCLUSION	82

CHAPTER 4 ANALYTICAL TECHNIQUES FOR BP SCHEMES

4.1	INTRODUCTION	84
4.2	VERIFICATION OF WELL BEHAVEDNESS: CONVENTIONAL METHODS	85
4.2.1	Application of Reduction Rules	86
4.2.1.1	A Fresh Look on Synthesis and Reduction Rules	86
4.2.1.2	New sets of Synthesis and Reduction Rules	92
4.2.1.3	Verification based on Reduction Rules	92
4.2.2	Verification using FC Representation of Bp Schemes	92
4.3	NEW METHODS FOR THE VERIFICATION OF WELL BEHAVEDNESS	94
4.3.1	Verification Based on CE Representation	94
4.3.1.1	Condition/Event Systems - Revisited	95
4.3.1.2	Transformation of Bp Scheme into CE Systems	97
4.3.1.3	Primitives for Arc Transformation	97
4.3.1.4	Primitives for V- Node Transformation	99
4.3.1.5	Primitives for &- Node Transformation	103
4.3.1.6	Discussion	106
4.3.1.7	Theorem for Well Behavedness of Bp Scheme	107

4.3.1.8	Application of BP-CE Transformation	109
4.3.1.9	Discussion	113
4.4	VERIFICATION BASED ON REACHABILITY GRAPH OF BP SCHEMES	116
4.4.1	Basic Concepts	116
4.4.1.1	Marking and Control States	116
4.4.1.2	Reachability and Reachability Graphs	117
4.4.2	Algorithm for Enumeration of Control States	117
4.4.3	Illustrative Examples	120
4.4.4	Discussion	123
4.5	DECOMPOSITION OF BP SCHEMES FOR DATA ALLOCATION	127
4.5.1	Allocation of Variables and V-components	127
4.5.2	Decomposition of Bp Scheme into V-Components	127
4.5.3	Method for Decomposing Bp Schemes into V-components	130
4.5.4	Arc Numbering System	131
4.5.5	Steps for Arc-Numbering	135
4.5.6	Decomposition Procedure	141
4.5.7	Examples	142
4.5.8	Arc Numbering System and Well Behavedness	147
4.5.9	Application of V-Components for Data Allocation	149
4.5.10	Discussion	149

4.6	FAIRNESS IN BP SCHEMES	152
4.7	WELL BEHAVED BP SCHEMES AND TRANSITION SYSTEMS	156
4.8	CONCLUSION	158
CHAPTER 5	PERFORMANCE EVALUATION USING BP SCHEMES	
5.1	INTRODUCTION	160
5.2	PERFORMANCE EVALUATION	161
5.3	A NEW INTERPRETATION TO BP SCHEMES	162
5.3.1	Time	162
5.3.2	Branching Probability	162
5.3.3	Moment Generating Function	163
5.3.4	Parameters Associated with each Arc of a Bp Scheme	163
5.3.5	Further Assumptions	164
5.3.6	Discussion	166
5.4	BP SCHEMES AS A PERFORMANCE MODELLING TOOL	166
5.4.1	Bp Schemes with V- Nodes	166
5.4.2	Basic Series System	169
5.4.3	Basic Parallel System	169
5.4.4	Basic Loop System	170
5.4.5	Procedure for Analysing Bp Schemes (with V-Nodes)	172
5.4.6	Application of Bp Schemes with V-Nodes	172
5.5	BP SCHEMES WITH V- AND &- NODES	173
5.5.1	V-node Sub-scheme	173

5.5.2	&-node Sub-scheme	175
5.5.3	Reduction Procedure	175
5.5.4	Further Reduction of Bp Schemes with V- and &-Nodes	178
5.5.4.1	Arc Reduction	178
5.5.4.2	Node Reduction	178
5.5.4.3	(X) -Reduction	180
5.5.4.4	&-diamond Reduction	182
5.5.5	General Algorithm for Analysis	182
5.6	PERFORMANCE ANALYSIS OF FMS	185
5.7	CONCLUSION	188
CHAPTER 6 CONCLUSION		
6.1	INTRODUCTION	190
6.2	SUMMARY AND CONCLUSION	190
6.3	SUGGESTION FOR FUTURE WORK	193
REFERENCES		195
APPENDIX A		
A.1	MOMENT GENERATING FUNCTION	205
A.2	APPLICATION OF BP SCHEMES FOR PERFORMANCE ANALYSIS	208
BIO-DATA		217