MODELLING OF NANOSCALE TUNNELLING FIELD EFFECT TRANSISTORS

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DEPERTMENT OF ELECTRICAL ENGINEERING

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MODELLING OF NANOSCALE TUNNELLING FIELD EFFECT TRANSISTORS

by

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Certificate

This is to certify that the thesis entitled **Modelling of nanoscale Tunnelling Field Effect Transistors** being submitted by **Mr. RAJAT VISHNOI** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, **Indian Institute of Technology Delhi**, is a record of bonafide work done by him under my supervision and guidance. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any degree or diploma.

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Dedicated

to

Mahatma Gandhi,
The Father of the Nation

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Rajat Vishnoi

Abstract

In the quest of increasing the density and the speed of integrated circuits (IC), MOSFETs have been extensively scaled over the past decade. As the size of the MOSFETs are scaled downwards, sub-threshold leakage current and leakage power in the ICs is increasing. With continued scaling, we have now reached a point where further miniaturization of the MOSFET is facing major challenges. Due to the thermal limit of 60 mV/decade on the sub-threshold slope (SS), conventional MOSFETs at sub-20 nm channel lengths suffer from high OFF-state leakage currents. They also suffer from numerous other short channel effects. Hence, as an alternative to the MOSFETs, TFETs have been widely studied. TFETs, due to a built-in tunneling barrier exhibit SS below 60 mV/decade, low off state leakage currents and diminished short channel effects. Therefore, TFETs are promising candidates for low power CMOS applications.

As TFETs are becoming popular, developing analytical models for predicting their current characteristics becomes important. In addition to predicting the drain current of the device, analytical models provide us insights into the functioning of the device. They also provide a starting point for developing industry standard compact models. Analytical modelling of TFETs is an emerging field, hence it is important to develop new and accurate analytical models for TFETs, using various mathematical techniques. Also, it is required to extend the existing modelling techniques for popular TFET architectures. Modelling the effects of non-idealities on the drain current of a TFET is also an important aspect.

In this work, a drain current model has been developed for a dual material gate (DMG) TFET by using a pseudo-2D solution to the Poisson's equation and the Kane's model for band-to-band tunneling. A DMG TFET provides an improved ON-state current, sub-threshold slope and drain saturation voltage over a conventional planar TFET.

Following an approach similar to the one followed for the DMG TFET, in this work, an analytical model has been developed for gate all around nanowire (GAA) TFET. It involves solving the 2D

Poisson's equation in the cylindrical coordinates and then using the Kane's model for band-to-band tunneling. A GAA structure due to an enhanced gate control provides an improved SS and short channel effects over a conventional planar TFET. It also provides an enhanced ON current due to the device geometry.

In this work, the effect of hot carriers has also been studied on the drain current of a TFET. Due to the presence of a high electric field at the source-channel junction, TFETs are more prone to hot carrier effects than the MOSFETs. Hence, in this work the effect of the presence of hot carrier induced localized charges on the threshold voltage of a TFET has been modelled and studied.

The approach used to develop the drain current models for a TFET in the initial part of this work lacks in accuracy in the sub-threshold region. Hence, in this work, for the first time an approach has been developed to model the drain current in a TFET, which is compact and analytical, and is accurate for the entire range of the gate voltages. Such a unified model is infinitely differentiable at each point in the output characteristics, which makes this model more suitable for analogue circuit simulation.

Finally, in this work, the effect of lateral doping profile variation on the drain current of a TFET is studied and modelled. It has been shown for the first time that, how the phenomena of band gap narrowing plays an important role in determining the drain current of a TFET when it has a non-abrupt lateral doping profile.

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Acronyms

SS	Sub-threshold slope
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DIBL	Drain Induced Barrier Lowering
CMOS	Complementary Metal Oxide Semiconductor
TFET	Tunnel Field Effect Transistor
DMG	Dual Material Gate
GAA	Gate All Around
SOI	Silicon on Insulator
$\hbar$	Plank's constant
m	Mass of electron
E_g	Band gap
T_{ox}	Gate oxide thickness
T_{Si}	Thickness of the silicon film

Φ	Gate metal work function
q	Electron charge
ε_{Si}	Permittivity of silicon
ε_{ox}	Permittivity of silicon dioxide
I_d	Drain current
G_{btb}	Tunneling generation rate
I_{ON}	ON-state current
I_{OFF}	OFF-state current
SMG	Single Material Gate
L_T	Shortest tunneling length
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
SS_{AVG}	Average sub-threshold slope
V_T	Threshold voltage of the TFET
TCAD	Technology Computer Aided Design

SCE	Short Channel Effects
HCE	Hot carrier effects
V_{FB}	Flat-band voltage
t_{inv}	Thickness of the inversion layer