CIRCUITS AND SYSTEMS FOR SUB-MICRO WATT ENERGY HARVESTING

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by

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To my beloved family members

Shri Venkateswara Rao, Shri Ramamohan Rao, Shrimati Krishna Kumari, and my teachers

Certificate

This is to certify that the thesis entitled **"Circuits and Systems for Sub-micro Watt Energy Harvesting"**, being submitted by **Mr. Ch Gajendranath Chaudhury** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

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Abstract

Deployment of wireless sensor networks require periodic battery replacement of all the sensor nodes. If possible, with energy harvesting from ambient sources, battery replacement will not be needed, and the maintenance cost of a wireless sensor network, or a body-area network, may be reduced significantly. Ambient sources for energy harvesting include ambient sound or vibrations, indoor light and RF radiation. The available power in ambient RF sources, in ambient vibrations, and in ambient light is only as large as 2 μW for a 1 square-cm transducer, and typically the voltage output of the transducer is very small. Most integrated circuits require more than 1 V supply voltage for reliable operation, and therefore there is a need for high performance DC-DC converters for voltage boosting. In this thesis, circuits and systems for sub-μW energy harvesting are discussed. For available input-power levels below 1 μW, voltage boosting is achieved by operating all circuits in the sub-threshold region, and by switching the DC-DC converter at tens of Hz, thereby reducing switching losses. Further explored the possibility of energizing the DC-DC inductor for an optimum duration, such that switching and resistive losses are minimized.

A modular power management system that can harvest energy from three sources simultaneously, with available power levels of 25 nW to 100 μW, with one inductor is proposed. The DC-DC converter is clocked with energize and dump pulses, and the pulse-widths are generated for constant peak inductor current and for no reversal, without current sensing. A comparator is used to reach the open-circuit-voltage-based maximum power point, and train an oscillator to mimic the comparator output. The oscillator frequency is tuned

through a successive-approximation algorithm within 11 comparator cycles. The 180 nm chip has a maximum efficiency of 87% at an input available power of 20 μW (input voltage of 0.6 V), and has an output voltage of 1.5 V.

To achieve ultra low power operation, ultra low power reference circuits are proposed. The proposed programmable voltage reference circuit uses two transistors with different threshold voltages for its core operation. The voltage reference is programmable in steps of 90 mV and consumes 80 pA. As a derivative of the voltage reference, a 0.3 nA current reference circuit is demonstrated. The difference of threshold voltages is used to generate a complementary-to-absolute temperature (CTAT) voltage. With an on-chip poly-resistor, and a 50 pA 6.5 Hz unity-gain bandwidth operational amplifier, the CTAT voltage is converted to a reference current. The current reference exhibits a variation of 518 ppm/$^\circ$C from -10 $^\circ$C to 80 $^\circ$C, consumes 1.6 nW, and occupies 0.164 mm^2 in a 180 nm process. As an application of the voltage reference circuit a temperature compensated under-voltage lock-out (UVLO) circuit is demonstrated. The designed UVLO circuit consumes 200 pA at 1.1 V. The measured low-to-high trip-point and high-to-low trip-point are 1.28 V and 1.12 V with variations of 208 ppm/$^\circ$C and 200 ppm/$^\circ$C respectively over a temperature range from -40 $^\circ$C to 75 $^\circ$C. The trip points are programmable from 1.1 V to 1.4 V in steps of 90 mV. The UVLO circuit uses 0.0055 mm^2 in a 180 nm CMOS process. With the help of a reference capacitor, and our voltage and current reference circuit techniques, a 30-minute timer was developed with a measured variation of 148 ppm/$^\circ$C over 70 $^\circ$C.

A novel CMOS ultra-low power (ULP) fractional band gap based voltage reference

(FBGR) is proposed. FBGR is achieved by subtracting a fraction of BJT CTAT from MOS CTAT. No operation amplifiers are used to generate the PTAT current and CTAT voltage subtraction. Simulation results shows that this fractional BGR circuit can generate a 260 mV voltage, having temperature coefficient (TC) of the voltage is 10 ppm/$^{\circ}$C, power consumption of 2 nW at 27 $^{\circ}$C temperature. FBGR has a line regulation of 20 ppm/V and power supply rejection of 65 dB at 100 Hz. Another bandgap regulator circuit, generating 1.18 V and driving the load of 1 nA to 30 mA is proposed. 1.18 V reference has TC of 30 ppm/$^{\circ}$C.

Voltage regulators are required in many integrated circuits to meet the current demands of the load, and at the same time provide a constant output voltage, which increases the complexity in their design. In this thesis, a three transistor voltage regulator based on a two transistor voltage reference is proposed. The regulator output voltage has a temperature coefficient of 50ppm/$^{\circ}$C over a load variation of 2 nA to 20 μA. The DC PSR obtained for the circuit was close to -43 dB with the maximum output noise spectral density equal to 3 $\mu V/\sqrt{Hz}$.

Table of Contents

List of Figures

List of Tables