HOT CARRIER RELIABILITY CHARACTERIZATION OF ADVANCED CMOS DEVICES

ANSHUL GUPTA

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

JULY 2020

HOT CARRIER RELIABILITY CHARACTERIZATION OF ADVANCED CMOS DEVICES

by

ANSHUL GUPTA

Department of Electrical Engineering

Submitted

In fulfillment of the requirements of the degree of Doctor of Philosophy

to the

INDIAN INSTITUTE OF TECHNOLOGY DELHI

JULY 2020

Certificate

This is to certify that the thesis entitled ***"Hot Carrier Reliability Characterization of Advanced CMOS Devices"***, being submitted by **Anshul Gupta** to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering and is a record of the original bonafide research work carried out by him. The results presented in the thesis have not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

I certify that he has pursued the prescribed course of research.

Prof. Abhisek Dixit
Associate Professor,
(Supervisor of Student)
Department of Electrical Engineering
Indian Institute of Technology Delhi
Hauz Khas, New Delhi – 110016

Acknowledgements

This thesis would not have been possible without the kind efforts of my well-wishers. Firstly, I would like to express my sincere gratitude to my Ph.D. supervisor Prof. Abhisek Dixit for his support and guidance during the course of my study. His vast exposure in the semiconductor field, immense knowledge, and motivation always enhanced my research-abilities throughout the course of learning from him. He has always helped me with technical discussions, and also improved scientific writing of this thesis.

Apart from my Ph.D. supervisor, I would like to acknowledge the inputs provided by my progress review committee members: Prof. Shouri Chatterjee, Prof. Madhusudan Singh and Prof. Smruti Ranjan Sarangi. I would like to thank them for their utmost guidance and encouragement.

Inputs from our collaborators have helped us in establishing the relevance of current work with present indutrial trends. This would have not been possible without the useful insights provided by them. I thank Reinaldo Vega and Terence B.Hook at IBM Research Group, Albany, USA for providing us with the cutting-edge hardware. Also Fernando Guarin from Global Foundries and H. S. Jatana from Semi-Conductor Laboratory, Chandigarh, India for their valuable inputs.

I express my thankfulness to the Department of Science and Technology, Govt. of India, for the instrumentation setup for the Device and Wafer Level Characterization laboratory, through SERB, under grant SB/S3/EECE/037/2014 and through TSG, under grant DST/TSG/AMT/2015/339 (General). Also I would thank the Visvesvaraya Ph.D. Scheme of Ministry of Electronics and Information Technology, Government of India, which is being implemented by Digital India Corporation.

I would like to give special thanks to Prof. Shree Prakash Tiwari from IIT Jodhpur for motivating and providing me the useful guidance. I thank my fellow labmates for creating and maintaining enthusiastic environment of the lab, and for all the beutiful memories we have had in the last four years. Thanks to Anil, Ramendra, Aarti, Sumreti, Kritika, Chandan, Chanchal and Manoj, who have been there to support me for my Ph.D. thesis.

A very special thanks to my dear friends Saurabh, Raj, Vivek who have supported me during this journey. In the end, I express my deep heartfelt gratitude to my respected parents, Smt. Veena Gupta and Shri Vijay Gupta for their blessings and supporting me. Special thanks to my beloved wife Charu for coming into my life, and always support me both professionally

and personally in the moments when there was no one to answer my queries. I am also thankful to my in-laws for having faith in me. Also great thanks to my brother Hitesh for being my support system. Thank you Bauji and Mumma for showering your heavenly blessings.

Anshul Gupta

Abstract

The current semiconductor industry is driven by continuous device scaling in order to keep up with Moore's law. Unfortunately, this has resulted in increased electric fields and operating temperature with more and more devices placed on a single chip. Such outcomes are giving rise to various reliability challenges which pose a threat to accurate operation for the integrated circuits. One such reliability concern is hot-carrier degradation (HCD) that affects the transistor parameters and consequently, functionality of various analog and digital circuits severely. The time-evolution of HCD in MOSFETs has traditionally been studied to predict device performance during its lifetime. HCD curve follows power-law with the time-exponent of degradation being an important measure. This variation in time power-law exponent for different stress bias combinations or over different stress time intervals can be used to identify the major degrading mechanism during HCD.

HCD studies involving accelerated testing renders inaccuracy when employed on advanced MOS devices such as silicon-on-insulator (SOI)-FETs. The use of continuous DC supply as stress voltage results in device-heating or self-heating (SH). This local temperature build-up within the device is known to enhance hot-carrier injection (HCI) in the gate dielectric of the device. Also, the use of a fixed DC stress voltage is overly pessimistic as it is seldom encountered in a real circuit operation. In general, the effective duty cycle of the voltages/currents applied to any device during a circuit operation will always be less than 100%. This demand for a revision in conventional stress set-up with the use of DC stress input being replaced by pulse or AC stress waveforms.

Stress-induced performance drifts have become common in RF circuits as well. Often during the circuit operation, the constituent transistors are exposed to high voltage, high current regimes thereby, making them vulnerable to HCD. Therefore, device technology qualification in terms of its DC as well as RF parameters is required. Moreover, understanding the device performance under RF operating conditions has also become critical. Therefore, formulating the methodologies and techniques such that the device is stressed under a realistic random logic circuit atmosphere with input bias chosen as per the targeted DC or RF application is necessary.

सार

वर्तमान अर्धचालक उद्योग निरंतर डिवाइस स्केलिंग द्वारा संचालित है मूर के नियम को बनाए रखने के लिए दुर्भाग्य से, यह हुआ है अधिक से अधिक उपकरणों के साथ बिजली के क्षेत्रों और ऑपरेटिंग तापमान में वृद्धि एक चिप पर रखा गया। इस तरह के परिणाम विभिन्न विश्वसनीयता को जन्म दे रहे हैं चुनौतियां जो एकीकृत के लिए सटीक संचालन के लिए खतरा पैदा करती हैं सर्किट। इस तरह की विश्वसनीयता की चिंता गर्म वाहक क्षरण (HCD) है ट्रांजिस्टर मापदंडों को प्रभावित करता है और फलस्वरूप, विभिन्न की कार्यक्षमता एनालॉग और डिजिटल सर्किट गंभीर रूप से। MOSFETs में HCD का समय-विकास पारंपरिक रूप से अपने जीवनकाल के दौरान डिवाइस के प्रदर्शन की भविष्यवाणी करने के लिए अध्ययन किया गया है। HCD वक्र गिरावट के समय-प्रतिपादक के साथ शक्ति-कानून का पालन करता है एक महत्वपूर्ण उपाय है। इसके लिए समय शक्ति-कानून के प्रतिपादक में भिन्नता विभिन्न तनाव पूर्वाग्रह संयोजन या विभिन्न तनाव समय अंतराल पर कर सकते हैं एचसीडी के दौरान प्रमुख अपमानजनक तंत्र की पहचान करने के लिए उपयोग किया जाता है।

HCD अध्ययनों में त्वरित परीक्षण शामिल है जब नियोजित करने में अशुद्धि होती है सिलिकॉन-ऑन-इन्सुलेटर (SOI)-FETs जैसे उन्नत MOS उपकरणों पर। तनाव-वोल्टेज के रूप में निरंतर डीसी आपूर्ति का उपयोग डिवाइस-हीटिंग में परिणाम करता है या स्व-हीटिंग (एसएच)। डिवाइस के भीतर इस स्थानीय तापमान का निर्माण होता है डिवाइस के गेट ढांकता हुआ में गर्म-वाहक इंजेक्शन (HCI) को बढ़ाने के लिए जाना जाता है। इसके अलावा, एक निश्चित डीसी तनाव वोल्टेज का उपयोग अत्यधिक निराशावादी है जैसा कि यह है शायद ही कभी एक असली सर्किट ऑपरेशन में सामना करना पड़ा। सामान्य तौर पर, प्रभावी कर्तव्य सर्किट ऑपरेशन के दौरान किसी भी उपकरण पर लागू वोल्टेज / धाराओं का चक्र हमेशा 100% से कम रहेगा। यह पारंपरिक में संशोधन की मांग करता है पल्स द्वारा प्रतिस्थापित डीसी तनाव इनपुट के उपयोग के साथ तनाव सेट-अप या एसी तनाव तरंग।

आरएफ सर्किट में तनाव-प्रेरित प्रदर्शन बदलाव आम हो गए हैं भी। अक्सर सर्किट ऑपरेशन के दौरान, घटक ट्रांजिस्टर होते हैं उच्च वोल्टेज, उच्च वर्तमान व्यवस्थाओं से अवगत कराया, जिससे वे कमजोर हो गए से HCD इसलिए, अपने डीसी के संदर्भ में डिवाइस प्रौद्योगिकी योग्यता साथ ही साथ आरएफ मापदंडों की आवश्यकता है। इसके अलावा, डिवाइस को समझना आरएफ ऑपरेटिंग शर्तों के तहत प्रदर्शन भी महत्वपूर्ण हो गया है। इसलिए, इस तरह के तरीके और तकनीक तैयार करना कि डिवाइस है इनपुट पूर्वाग्रह के साथ एक यथार्थवादी यादृच्छिक तर्क सर्किट वातावरण के तहत जोर दिया लक्षित डीसी या आरएफ आवेदन के अनुसार चुना जाना आवश्यक है।

Contents

List of Figures

List of Tables

List of Abbreviations

Abbreviation	Description
BTI	**B**ias **T**emperature **I**nstability
CHE	**C**hannel-**H**ot **E**lectron
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CV	**C**apacitance-**V**oltage
DAHC	**D**rain-**A**valanche **H**ot **C**arrier
DCIV	**D**irect-**C**urrent **C**urrent **V**oltage
DUT	**D**evice **U**nder **T**est
EEDF	**E**lectron **E**nergy **D**istribution **F**unction
EES	**E**lectron-**E**lectron **S**cattering
EOT	**E**ffective **O**xide **T**hickness
FDSOI	**F**ully **D**epleted **S**ilicon-**o**n-**I**nsulator
FinFET	**F**in **F**ield-**E**ffect **T**ransistor
FOMs	**F**igures-**o**f-**M**erit
GSG	**G**round-**S**ignal-**G**round
GUI	**G**raphical **U**ser **I**nterface
HC	**H**ot-**C**arrier
HCD	**H**ot-**C**arrier **D**egradation
HCI	**H**ot-**C**arrier **I**njection
HCS	**H**ot-**C**arrier **S**tress
ISS	**I**mpedance **S**tandard **S**ubstrates
I/O	**I**nput **O**utput
IV	**C**urrent **V**oltage
LDD	**L**ightly **D**oped **D**rain
LEM	**L**ucky **E**lectron **M**odel
LSL	**L**ower **S**pecification **L**imit
LTL	**L**ower **T**olerance **L**imit
MFCMU	**M**ulti-**F**requency **C**apacitance **M**easurement **U**nit
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
MPSMU	**M**edium **P**ower **S**ource **M**easure **U**nit
MuGFETs	**M**ultiple **G**ate **F**ield-**E**ffect **T**ransistors
NBTI	**N**egative **B**ias **T**emperature **I**nstability

NMOS	**N**egative-channel **MOS**
NWFET	**N**anowire **F**ield-**E**ffect **T**ransistor
PMOS	**P**ositive-channel **MOS**
RSU	**R**emote-**S**ense & **S**witch **U**nit
SCE	**S**hort-**C**hannel **E**ffect
SCL	**S**emiconductor **L**aboratory
SH	**S**elf-**H**eating
SHE	**S**elf-**H**eating **E**ffect
SMS	**S**tress-**M**easure-**S**tress
SMU	**S**ource-**M**easure-**U**nit
SOI	**S**ilicon-**o**n-**I**nsulator
SOLT	**S**hort-**O**pen-**L**oad-**T**hru
S/D	**S**ource/**D**rain
TDDB	**T**ime **D**ependent **D**ielectric **B**reakdown
TEM	**T**ransmission **E**lectron **M**icroscopy
USL	**U**pper **S**pecification **L**imit
UTL	**U**pper **T**olerance **L**imit
VNA	**V**ector **N**etwork **A**nalyzer
WGFMU	**W**aveform **G**enerator/**F**ast **M**easurement **U**nit

List of Symbols

Symbol	Description
N_{ot}	Bulk-Oxide Traps
I_{CP}	Charge Pumping Current
A_i	Current Gain
f_T	Cut off frequency
W	Device Width
C_{dd}	Drain Capacitance
I_{ds}	Drain Current
V_{ds}	Drain Voltage
W_{fin}	Effective Total Channel Width of the FinFET
W_{eff}	Effective Total Channel Width of the MOSFET
I_{stack}	Effective Stack Current
t	Effective Stress Time
τ_f	Falling Delay
H_{fin}	Fin Height
D_{fin}	Fin Width
V_{FB}	Flat-Band Voltage
C_{gg}	Gate Capacitance
I_{gate}	Gate Current
Lg	Gate Length
R_g	Gate Resistance
V_{gs}	Gate Voltage
N_{it}	Interface Traps
T_L	Lattice Temperature
$I_{d,lin}$	Linear Drain Current
$V_{ds,lin}$	Linear Drain Voltage
$V_{TH,lin}$	Linear Threshold Voltage
$G_{m,lin}$	Linear transconductance
f_{max}	Maximum Operating Frequency
N_{fin}	Number of Fins
N_f	Number of Gate Fingers

I_{OFF}	OFF-current
I_{ON}	On Drain Current
G_{ds}	Output Conductance
$I_{d,sat}$	Saturation Drain Current
$V_{ds,sat}$	Saturation Drain Voltage
$V_{TH,sat}$	Saturation Threshold Voltage
$V_{ds,stress}$	Stress applied at Drain terminal
$V_{gs,stress}$	Stress applied at Gate terminal
V_{stress}	Stress Voltage
I_{sub}	Substrate Current
SS	Subthreshold Slope
SS_{lin}	Subthreshold Slope in Linear Region
V_{dd}	Supply Voltage
R_{th}	Thermal Resistance
I_{TH}	Threshold Current
V_{TH}	Threshold Voltage
n	Time Exponent of Hot-carrier Degradation
G_m	Transconductance
$\|U\|$	Unilateral Power Gain
A_v	Voltage Gain