

**HOT CARRIER RELIABILITY
CHARACTERIZATION OF ADVANCED CMOS
DEVICES**

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**DEPARTMENT OF ELECTRICAL ENGINEERING
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DEVICES**

by

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Department of Electrical Engineering

Submitted

*In fulfillment of the requirements of the degree of Doctor of Philosophy
to the*



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Certificate

This is to certify that the thesis entitled “*Hot Carrier Reliability Characterization of Advanced CMOS Devices*”, being submitted by **Anshul Gupta** to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering and is a record of the original bonafide research work carried out by him. The results presented in the thesis have not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

I certify that he has pursued the prescribed course of research.

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Abstract

The current semiconductor industry is driven by continuous device scaling in order to keep up with Moore's law. Unfortunately, this has resulted in increased electric fields and operating temperature with more and more devices placed on a single chip. Such outcomes are giving rise to various reliability challenges which pose a threat to accurate operation for the integrated circuits. One such reliability concern is hot-carrier degradation (HCD) that affects the transistor parameters and consequently, functionality of various analog and digital circuits severely. The time-evolution of HCD in MOSFETs has traditionally been studied to predict device performance during its lifetime. HCD curve follows power-law with the time-exponent of degradation being an important measure. This variation in time power-law exponent for different stress bias combinations or over different stress time intervals can be used to identify the major degrading mechanism during HCD.

HCD studies involving accelerated testing renders inaccuracy when employed on advanced MOS devices such as silicon-on-insulator (SOI)-FETs. The use of continuous DC supply as stress voltage results in device-heating or self-heating (SH). This local temperature build-up within the device is known to enhance hot-carrier injection (HCI) in the gate dielectric of the device. Also, the use of a fixed DC stress voltage is overly pessimistic as it is seldom encountered in a real circuit operation. In general, the effective duty cycle of the voltages/currents applied to any device during a circuit operation will always be less than 100%. This demand for a revision in conventional stress set-up with the use of DC stress input being replaced by pulse or AC stress waveforms.

Stress-induced performance drifts have become common in RF circuits as well. Often during the circuit operation, the constituent transistors are exposed to high voltage, high current regimes thereby, making them vulnerable to HCD. Therefore, device technology qualification in terms of its DC as well as RF parameters is required. Moreover, understanding the device performance under RF operating conditions has also become critical. Therefore, formulating the methodologies and techniques such that the device is stressed under a realistic random logic circuit atmosphere with input bias chosen as per the targeted DC or RF application is necessary.

सार

वर्तमान अर्धचालक उद्योग निरंतर डिवाइस स्केलिंग द्वारा संचालित है मूर के नियम को बनाए रखने के लिए दुर्भाग्य से, यह हुआ है अधिक से अधिक उपकरणों के साथ बिजली के क्षेत्रों और ऑपरेटिंग तापमान में वृद्धि एक चिप पर रखा गया। इस तरह के परिणाम विभिन्न विश्वसनीयता को जन्म दे रहे हैं चुनौतियां जो एकीकृत के लिए सटीक संचालन के लिए खतरा पैदा करती हैं सर्किट। इस तरह की विश्वसनीयता की चिंता गर्म वाहक क्षरण (HCD) है ट्रांजिस्टर मापदंडों को प्रभावित करता है और फलस्वरूप, विभिन्न की कार्यक्षमता एनालॉग और डिजिटल सर्किट गंभीर रूप से। MOSFETs में HCD का समय-विकास पारंपरिक रूप से अपने जीवनकाल के दौरान डिवाइस के प्रदर्शन की भविष्यवाणी करने के लिए अध्ययन किया गया है। HCD वक्र गिरावट के समय-प्रतिपादक के साथ शक्ति-कानून का पालन करता है एक महत्वपूर्ण उपाय है। इसके लिए समय शक्ति-कानून के प्रतिपादक में भिन्नता विभिन्न तनाव पूर्वाग्रह संयोजन या विभिन्न तनाव समय अंतराल पर कर सकते हैं एचसीडी के दौरान प्रमुख अपमानजनक तंत्र की पहचान करने के लिए उपयोग किया जाता है।

HCD अध्ययनों में त्वरित परीक्षण शामिल है जब नियोजित करने में अशुद्धि होती है सिलिकॉन-ऑन-इन्सुलेटर (SOI)-FETs जैसे उन्नत MOS उपकरणों पर। तनाव-वोल्टेज के रूप में निरंतर डीसी आपूर्ति का उपयोग डिवाइस-हीटिंग में परिणाम करता है या स्व-हीटिंग (एसएच)। डिवाइस के भीतर इस स्थानीय तापमान का निर्माण होता है डिवाइस के गेट ढांकता हुआ में गर्म-वाहक इंजेक्शन (HCI) को बढ़ाने के लिए जाना जाता है। इसके अलावा, एक निश्चित डीसी तनाव वोल्टेज का उपयोग अत्यधिक निराशावादी है जैसा कि यह है शायद ही कभी एक असली सर्किट ऑपरेशन में सामना करना पड़ा। सामान्य तौर पर, प्रभावी कर्तव्य सर्किट ऑपरेशन के दौरान किसी भी उपकरण पर लागू वोल्टेज / धाराओं का चक्र हमेशा 100% से कम रहेगा। यह पारंपरिक में संशोधन की मांग करता है पल्स द्वारा प्रतिस्थापित डीसी तनाव इनपुट के उपयोग के साथ तनाव सेट-अप या एसी तनाव तरंग।

आरएफ सर्किट में तनाव-प्रेरित प्रदर्शन बदलाव आम हो गए हैं भी। अक्सर सर्किट ऑपरेशन के दौरान, घटक ट्रांजिस्टर होते हैं उच्च वोल्टेज, उच्च वर्तमान व्यवस्थाओं से अवगत कराया, जिससे वे कमजोर हो गए से HCD इसलिए, अपने डीसी के संदर्भ में डिवाइस प्रौद्योगिकी योग्यता साथ ही साथ आरएफ मापदंडों की आवश्यकता है। इसके अलावा, डिवाइस को समझना आरएफ ऑपरेटिंग शर्तों के तहत प्रदर्शन भी महत्वपूर्ण हो गया है। इसलिए, इस तरह के तरीके और तकनीक तैयार करना कि डिवाइस है इनपुट पूर्वाग्रह के साथ एक यथार्थवादी यादृच्छिक तर्क सर्किट वातावरण के तहत जोर दिया लक्षित डीसी या आरएफ आवेदन के अनुसार चुना जाना आवश्यक है।

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List of Abbreviations

Abbreviation	Description
BTI	Bias Temperature Instability
CHE	Channel-Hot Electron
CMOS	Complementary Metal-Oxide-Semiconductor
CV	Capacitance-Voltage
DAHC	Drain-Avalanche Hot Carrier
DCIV	Direct-Current Current Voltage
DUT	Device Under Test
EEDF	Electron Energy Distribution Function
EES	Electron-Electron Scattering
EOT	Effective Oxide Thickness
FDSOI	Fully Depleted Silicon-on-Insulator
FinFET	Fin Field-Effect Transistor
FOMs	Figures-of-Merit
GSG	Ground-Signal-Ground
GUI	Graphical User Interface
HC	Hot-Carrier
HCD	Hot-Carrier Degradation
HCI	Hot-Carrier Injection
HCS	Hot-Carrier Stress
ISS	Impedance Standard Substrates
I/O	Input Output
IV	Current Voltage
LDD	Lightly Doped Drain
LEM	Lucky Electron Model
LSL	Lower Specification Limit
LTL	Lower Tolerance Limit
MFCMU	Multi-Frequency Capacitance Measurement Unit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPSMU	Medium Power Source Measure Unit
MuGFETs	Multiple Gate Field-Effect Transistors
NBTI	Negative Bias Temperature Instability

NMOS	Negative-channel MOS
NWFET	Nanowire Field-Effect Transistor
PMOS	Positive-channel MOS
RSU	Remote-Sense & Switch Unit
SCE	Short-Channel Effect
SCL	Semiconductor Laboratory
SH	Self-Heating
SHE	Self-Heating Effect
SMS	Stress-Measure-Stress
SMU	Source-Measure-Unit
SOI	Silicon-on-Insulator
SOLT	Short-Open-Load-Thru
S/D	Source/Drain
TDDDB	Time Dependent Dielectric Breakdown
TEM	Transmission Electron Microscopy
USL	Upper Specification Limit
UTL	Upper Tolerance Limit
VNA	Vector Network Analyzer
WGFMU	Waveform Generator/Fast Measurement Unit

List of Symbols

Symbol	Description
N_{ot}	Bulk-Oxide Traps
I_{CP}	Charge Pumping Current
A_i	Current Gain
f_T	Cut off frequency
W	Device Width
C_{dd}	Drain Capacitance
I_{ds}	Drain Current
V_{ds}	Drain Voltage
W_{fin}	Effective Total Channel Width of the FinFET
W_{eff}	Effective Total Channel Width of the MOSFET
I_{stack}	Effective Stack Current
t	Effective Stress Time
τ_f	Falling Delay
H_{fin}	Fin Height
D_{fin}	Fin Width
V_{FB}	Flat-Band Voltage
C_{gg}	Gate Capacitance
I_{gate}	Gate Current
L_g	Gate Length
R_g	Gate Resistance
V_{gs}	Gate Voltage
N_{it}	Interface Traps
T_L	Lattice Temperature
$I_{d,lin}$	Linear Drain Current
$V_{ds,lin}$	Linear Drain Voltage
$V_{TH,lin}$	Linear Threshold Voltage
$G_{m,lin}$	Linear transconductance
f_{max}	Maximum Operating Frequency
N_{fin}	Number of Fins
N_f	Number of Gate Fingers

I_{OFF}	OFF-current
I_{ON}	On Drain Current
G_{ds}	Output Conductance
$I_{d,sat}$	Saturation Drain Current
$V_{ds,sat}$	Saturation Drain Voltage
$V_{TH,sat}$	Saturation Threshold Voltage
$V_{ds,stress}$	Stress applied at Drain terminal
$V_{gs,stress}$	Stress applied at Gate terminal
V_{stress}	Stress Voltage
I_{sub}	Substrate Current
SS	Subthreshold Slope
SS_{lin}	Subthreshold Slope in Linear Region
V_{dd}	Supply Voltage
R_{th}	Thermal Resistance
I_{TH}	Threshold Current
V_{TH}	Threshold Voltage
n	Time Exponent of Hot-carrier Degradation
G_m	Transconductance
$ U $	Unilateral Power Gain
A_v	Voltage Gain