STUDIES IN ANALOG VLSI IMPLEMENTATION OF NEURAL NETWORKS

by

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CERTIFICATE

This is to certify that the dissertation titled "Studies In Analog VLSI Implementation Of Neural Networks", which is being submitted by Mr. Kaushik Saha to the Indian Institute of Technology, Delhi, is a record of the bona fide research work carried out by him under our guidance and supervision.

It is our opinion that this dissertation has reached a standard meeting the requirements of all regulations relating to the award of the degree of Doctor of Philosophy. The results contained in it have not been submitted in part or in full to any other university or institute for the award of any degree or diploma.

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" Those who loved me,
Lit His divine lamp in my temple,
In His Divinity do I feel their affection,
To them, my salutations. "
- Rabindranath Tagore

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ABSTRACT

Artificial neural networks (a.n.n.) constitute a novel parallel computing paradigm. They find application in diverse areas where computers based on the von Neumann model prove to be inadequate, e.g. pattern recognition, combinatorial optimisation and many others. As the strength of a.n.n. lies in the massively parallel architecture of highly interconnected (through *synapses*) computing nodes (*neurons*), they pose special problems to the designer attempting to realise them using VLSI (very large scale integration) integrated circuits (IC).

The work in this thesis focuses on the issues involved in realising a multi-layer, feed-forward perceptron type a.n.n. as a VLSI device. Existing literature has been reviewed with the aim of selecting a suitable synapse and neuron design. Analog circuits, realisable using CMOS technology, were found to be more suitable in many ways, though digital techniques are also highly popular and have their own merits. The circuit selected uses two MOS transistors in the linear region of operation for synaptic multiplication. The sum of the synaptic products is calculated using the natural summing of currents incident on a node, and hence, this circuit belongs to the family of current-mode analog computing circuits. The circuit exhibits high speed of operation and high noise immunity, besides being compact.

The large thermal dissipation associated with the circuit is its main disadvantage. This is on account of the low resistivity shown by MOS transistors while operating in the linear region.This may be overcome by increasing the size of the synaptic devices, thereby losing the advantage of compactness. A tentative floor-plan and routing strategy for the a.n.n. chip to be designed with the neurons under study has been proposed. A design procedure has been developed to enable computation of the minimum device size which satisfies the constraints

synapses to a single neuron. An algorithm to partition a trained, extensively connected a.n.n. into distinct unconnected blocks has been developed. The algorithm, which uses the training data and the connectivity matrix as inputs, attempts the partitioning with as little degradation in the performance of the system as possible.

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