

**INVESTIGATION OF CMOS SCALING EFFECTS
ON HOT-CARRIER RELIABILITY THROUGH
ON-WAFER DEVICE CHARACTERIZATION**

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INVESTIGATION OF CMOS SCALING EFFECTS ON HOT-CARRIER RELIABILITY THROUGH ON-WAFER DEVICE CHARACTERIZATION

by

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Submitted

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Certificate

This is to certify that the thesis entitled "*Investigation of CMOS Scaling Effects on Hot-Carrier Reliability through on-wafer Device Characterization*", being submitted by **Charu Gupta** to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering and is a record of the original bonafide research work carried out by her. The results presented in the thesis have not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

I certify that she has pursued the prescribed course of research.

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"In everyone's life, at some time, our inner fire goes out. It is then burst into flame by an encounter with another human being. We should all be thankful for those people who rekindle the inner spirit."

Albert Schweitzer

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It is rightly said, *"Alone we can do so little; together we can do so much."*

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Octavio Paz (1990). "Búsqueda Del Presente", Harcourt

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Abstract

Performance degradation due to early device-aging has been a critical concern for semiconductor industry. High electric fields within the device channel lead to several reliability concerns hindering further downscaling at advanced technology nodes. Hot-carrier degradation (HCD) is one such dominant aging mechanism in present-day integrated circuits. For a device under hot-carrier stress (HCS), threshold voltage (V_{TH}) gradually changes over time which can affect the speed of the encompassing circuit leading to operation failure. Several factors including external operating conditions like temperature, nature of applied stress bias (asynchronous/synchronous pulse, DC, RF), and frequency of operation etc. affect the performance of a circuit due to HCD. In addition, V_{TH} variations may occur in a device due to increased process variability at nanoscale dimensions as well. Therefore, a thorough understanding of these issues is needed to ensure required device lifetime and accurate functionality.

This work addresses HCD aging from two major perspectives; first, accurate age monitoring and identification of dominant degrading mechanisms. In order to implement guard-bands for failure-prevention, critical biases affecting device performance at different technology nodes are determined. However, issues peculiar to device geometries, such as increase in series resistance in narrow fins, increased local device-temperature due to dense layouts, change in V_{TH} at narrow dimensions etc. may change the effective stress bias reaching the channel. Thus, the geometrical implications of HCD are studied to determine most degrading bias combinations. The second perspective deals with the effect of device scaling on HCD. Conservative performance metrics, such as ON-current, V_{TH} or subthreshold slope are studied along with OFF-state leakage current and drain-induced barrier lowering, for holistic analysis of device performance in different operation regimes. Moreover, dynamic workload i.e. pulsed asynchronous stress is used for optimizing guard-band, which is otherwise too strict if based on DC stress conditions. Also, RF metrics are investigated using S-parameters showing that the mechanisms affecting DC and RF device performance are necessarily the same.

सार

अर्ली डिवाइस-एजिंग के कारण प्रदर्शन में गिरावट अर्धचालक उद्योग के लिए एक महत्वपूर्ण चिंता का विषय रहा है। डिवाइस चैनल के भीतर उच्च विद्युत क्षेत्र कई विश्वसनीयता चिंताओं का कारण बनते हैं, जो उन्नत प्रौद्योगिकी नोड्स में और गिरावट लाते हैं। वर्तमान समय के एकीकृत परिपथों में हॉट-कैरियर डिग्रेडेशन (HCD) एक ऐसा प्रमुख उम्र बढ़ने वाला तंत्र है। गर्म-वाहक तनाव (HCS) के तहत एक उपकरण के लिए, थ्रेशोल्ड वोल्टेज (V_{TH}) धीरे-धीरे समय के साथ बढ़ता है जो ऑपरेशन विफलता के लिए अग्रणी सर्किट की गति को प्रभावित कर सकता है। तापमान के बाहरी संचालन की स्थिति, लागू तनाव पूर्वाग्रह की प्रकृति (अतुल्यकालिक / तुल्यकालिक पल्स, डीसी, आरएफ) और ऑपरेशन की आवृत्ति आदि सहित कई कारक HCD के कारण एक सर्किट के प्रदर्शन को प्रभावित करते हैं। इसके अलावा, V_{TH} भिन्नता डिवाइस में नैनोस्केल आयामों पर प्रक्रिया परिवर्तनशीलता के कारण भी हो सकती है। इसलिए, आवश्यक डिवाइस जीवनकाल और सटीक कार्यक्षमता सुनिश्चित करने के लिए इन मुद्दों की गहन समझ आवश्यक है।

यह कार्य दो प्रमुख दृष्टिकोणों से HCD को संबोधित करता है; सबसे पहले, सटीक उम्र की निगरानी और प्रमुख विफलता तंत्र की पहचान। विफलता-रोकथाम के लिए गार्ड-बैंड को लागू करने के लिए, विभिन्न प्रौद्योगिकी नोड्स पर डिवाइस के प्रदर्शन को प्रभावित करने वाले महत्वपूर्ण पूर्वाग्रह निर्धारित किए जाते हैं। हालाँकि, डिवाइस ज्यामिति के लिए अजीबोगरीब मुद्दे, जैसे संकीर्ण पंखों में श्रृंखला प्रतिरोध में वृद्धि, घने लेआउट के कारण स्थानीय डिवाइस-तापमान में वृद्धि, V_{TH} में संकीर्ण आयामों में परिवर्तन आदि प्रभावी तनाव पूर्वाग्रह को चैनल तक पहुंचा सकते हैं। । इस प्रकार, HCD के ज्यामितीय निहितार्थों का अध्ययन सबसे अधिक विफलता पूर्वाग्रह संयोजनों को निर्धारित करने के लिए किया जाता है। दूसरा दृष्टिकोण HCD पर डिवाइस स्केलिंग के प्रभाव से संबंधित है। अलग-अलग ऑपरेशन अपराधों में डिवाइस के प्रदर्शन के समग्र विश्लेषण के लिए ऑफ-करेंट, लीकेज करंट और ड्रेन-इंस्पायर्ड बैरियर लोअरिंग के साथ कंजर्वेटिव परफॉर्मेंस मेट्रिक्स, जैसे ओएन-करेंट, V_{TH} या सबथ्रेशोल्ड ढलान का अध्ययन किया जाता है। इसके अलावा, डायनेमिक वर्कलोड यानी स्पंदित अतुल्यकालिक तनाव का उपयोग गार्ड-बैंड के अनुकूलन के लिए किया जाता है, जो कि डीसी तनाव की स्थिति के आधार पर अन्यथा बहुत सख्त है। इसके अलावा, आरएफ मेट्रिक्स की जांच एस-मापदंडों का उपयोग करके की जाती है जो दिखाते हैं कि डीसी और आरएफ डिवाइस के प्रदर्शन को प्रभावित करने वाले तंत्र जरूरी समान हैं।

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List of Abbreviations

Abbreviation	Description
BEOL	Back-End-of-Life
BTI	Bias Temperature Instability
CLM	Channel Length Modulation
IV	Current Voltage
DUT	Device-under-Test
DG-DC	Double-Gate Double-Channel
DIBL	Drain-Induced Barrier Lowering
FET	Field-Effect Transistor
FinFET	Fin Field-Effect Transistor
GAA	Gate-All-Around
GIDL	Gate-Induced Drain Leakage
GUI	Graphical User Interface
GSG	Ground-Signal-Ground
HEMT	High-Electron-Mobility Transistor
HDD	Highly-Doped Drain
HC	Hot-Carrier
HCD	Hot-Carrier Degradation
HCI	Hot-Carrier Injection
HCS	Hot-Carrier Stress
ISS	Impedance Standard Substrate
ISL	Insertion Layer
ILD0	Interlayer Dielectric level Zero
LDD	Lightly-Doped Drain
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MSE	Minimum least Squared Error
MIS	Metal-Insulator-Semiconductor
MFCMU	Multi-Frequency Capacitance Measurement Unit
NW	Nanowire
NWFET	Nanowire Field-Effect Transistor
NBTI	Negative Bias Temperature Instability
NMOS	Negative-channel MOS

PBTI	Positive Bias Temperature Instability
PMOS	Positive-channel MOS
QS-CV	Quasi Static-Capacitance Voltage
RTA	Rapid Thermal Annealing
RSU	Remote-Sense & Switch Unit
RMG	Replacement-Metal Gate
SH	Self-Heating
SHE	Self-Heating Effect
SDA	Semiconductor Device Analyzer
SPA	Semiconductor Parametric Analyzer
SCE	Short-Channel Effect
SOLT	Short-Open-Load-Through
SIT	Sidewall Image Transfer
SOI	Silicon-on-Insulator
SG-SC	Single-Gate Single-Channel
SG-DC	Single-Gate Double-Channel
S/D	Source/Drain
SMU	Source-Measure-Unit
TCAD	Technology Computer-aided Design
TDDb	Time Dependent Dielectric Breakdown
TTF	Time to Failure
VNA	Vector Network Analyzer
WGFMU	Waveform Generator/Fast Measurement Unit
2-DEG	2-D Electron Gas

List of Symbols

Symbol	Description
N_{ot}	Bulk-Oxide Trapping
v	Carrier Velocity
k	Change in $V_{TH,sat}$ to Change in $V_{TH,lin}$
R_{ch}	Channel Resistance
τ_c	Characteristic Capture Time
τ_e	Characteristic Emission Time
E_c	Conduction Band
E_{cr}	Critical Electric Field
I_{ds}	Drain Current
R_D	Drain Resistance
V_{dg}	Drain to Gate Voltage
V_{ds}	Drain Voltage
μ_{eff}	Effective Mobility
EOT	Effective Oxide Thickness
t	Effective Stress Time
W_{fin}	Effective Total Channel Width of the FinFET
W_{NW}	Effective Total Channel Width of the NWFET
$W_{effective}$	Effective Width
E	Electric Field
E_g	Energy Band Gap
D_{fin}	Fin Thickness
FP	Fin/Nanowire Pitch
f	Frequency of AC Stress Signal
I_{gate}	Gate Current
$I_{g,Leak}$	Gate Leakage Current
L_g	Gate Length
V_{gs}	Gate Voltage
I_{GIDL}	GIDL current
N_{it}	Interface state generation
$I_{d,lin}$	Linear Drain Current

$V_{ds,lin}$	Linear Drain Voltage
f_{max}	Maximum Operating Frequency
d_{NW}	Nanowire Width
N_{fin}	Number of Fins
N_{finger}	Number of Gate Fingers
N_{NW}	Number of Parallel Nanowires
I_{OFF}	OFF-current
I_{ON}	ON-current
g_{ds}	Output Conductance
$V_{OverDrive}$	Overdrive Voltage
H_{fin}	Physical Height of FinFET
H_{NW}	Physical Height of NWFET
$V_{ds,sat}$	Pinch-off/Saturation Drain Voltage
R_S	Source Resistance
R_{SD}	Source-Drain Resistance
V_{stress}	Stress Voltage
$V_{ds,stress}$	Stress Voltage at Drain
$V_{gs,stress}$	Stress Voltage at Gate
I_{subth}	Subthreshold Current
SS	Subthreshold Slope
V_{DD}	Supply Voltage
A	Technology-Dependent Constant of Hot-Carrier Degradation
I_{TH}	Threshold Current
V_{TH}	Threshold Voltage
$V_{TH,lin}$	Threshold Voltage in Linear Regime
$V_{TH,sat}$	Threshold Voltage in Saturation Regime
T_{delay}	Time Delay
n	Time Exponent of Hot-Carrier Degradation
I_{Leak}	Total Leakage Current
R_{total}	Total MOSFET Resistance
G_m	Transconductance
f_t	Transistor Cut-off Frequency
E_v	Valence Band
v_{sat}	Velocity Saturation