DESIGN AND SIMULATION OF TRENCH GATE POWER MOSFETs FOR SWITCHING AND RF APPLICATIONS

By

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Certificate

This is to certify that the thesis entitled "**Design and Simulation of Trench Gate Power MOSFETs for Switching and RF Applications**" being submitted by **Raghvendra Sahai Saxena** for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology, Delhi, is a record of bonafied work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

Date: 11-Oct-2010
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Abstract

The devices that allow us to control the flow of electrical energy in to the systems are of utmost importance. These devices are called power devices. In the present age of limited energy resources, efficient and effective handling of the energy is required. To make the electrical control easy and energy efficient, we need to have efficient power devices. In the medium to low voltage applications, a trench gate power MOSFET is the most efficient device than other devices as it provides the lowest ON resistance than any other MOS device. However, the need of efficiency is even more and requires further improvements in its basic structure. The main objective of the thesis is to discuss the technological limitations in the trench gate MOSFET performance and a few methods to overcome some of these deficiencies. The recent improvements in the semiconductor device technology have led to a new era of nanoscale CMOS devices to boost the performance of VLSI / ULSI circuits. The same technology may also be used to improve the performance of power devices, similar to what was done for initial development of power MOSFETs in 1970's.

The major performance parameters of power MOSFETs are ON state performance parameters: R_{ON} and transconductance, OFF state performance parameter: breakdown voltage (V_{BD}) and switching performance parameters: total gate charge (Q_G) and gate-to-drain charge (Q_{GD}). In this thesis, we concentrate on the improvements of parameters, R_{ON}, V_{BD}, transconductance and gate charges. We have used some of the nanoscale device technologies in trench gate power MOSFET to improve its performance. This includes the following:

- Use of strained Si channel for enhancing the carrier mobility in order to reduce the channel resistance of the device in ON state.
- Use of multiple gates for performance enhancement.
- Use of gate stack with different materials for work function engineering.
- Use of gate oxide engineering for performance enhancement.

To demonstrate the performance improvement over the conventional device structure, we have also created the equivalent conventional device structures in ATLAS and performed numerical simulations of the proposed devices with respect to their equivalent conventional devices. We found that it gives quantifiable bench-marks of improvements in drive current, on state resistance, peak transconductance, switching delays and breakdown voltage as compared to the conventional trench gate MOSFET device. The simulation based demonstration of improvements in the performance is expected to provide the incentive for experimental verification.

Contents

1. Introduction 1

1.1 Motivation 1

1.2 MOSFETs in Power Applications 2

1.3 The Trench Gate Power MOSFET 3

1.4 Objectives and Overview of the Thesis 5

2 A Brief Review on Trench Gate Power MOSFET 7

2.1 Evolution of Trench Gate Power MOSFET 7

2.2 Structural Advances and Innovations 10

2.2.1 Trench Optimization 10

2.2.2 Body / Channel Profile Engineering 12

2.2.3 Drift Region Engineering 14

2.2.3.1 Floating Islands 14

2.2.3.2 Super Junction and RESURF 15

2.2.4 Use of Metal Substrates 19

2.3 Advances in Fabrication Technology 21

2.3.1 Trench Etching Technology 22

2.3.2 Self-Aligned Fabrication Process 24

2.3.3 Other Technological Innovations 26

2.4 Characterization Techniques and Reliability 27

2.4.1 Device and Process Characterization 27

2.4.1.1 Gate Charge 28

2.4.1.2 Carrier Mobility Extraction 31

2.4.1.3 Energy Capability Estimation 31

2.4.1.4 Process Control and Monitoring 32

2.4.2 Reliability Estimation and Assurance 34

3 Strained Silicon Channel Trench Gate Power MOSFET 37

3.1 Introduction 37

3.2 Device Structure and Proposed Fabrication Process 38

3.3 Results and Discussion 42

3.3.1 Effect of Energy Band Modifications 44

3.3.2 Current Voltage Characteristics 47

3.3.3 Gate Charge and Switching Delays 51

3.3.4 Breakdown 53

3.4 Dual Gate SCT MOSFET 54

3.5 Conclusions 58

4 Dual Material Gate Trench Power MOSFET 59

4.1 Introduction 59

4.2 Device Structure and Proposed Fabrication Process 62

4.3 Results and Discussion 64

4.4 Conclusions 72

5 Stepped Oxide Hetero Material Gate Trench Power MOSFET 73

5.1 Introduction 73

5.2 Device Structure and Proposed Fabrication Process 75

5.3 Results and Discussion 78

5.3.1 Current Voltage Characteristics 80

5.3.2 Gate Charge and Switching Delays 82

5.3.3 Drain Breakdown Voltage 85

5.4 Conclusions 87

6 Buried Drift Region Oxide in Trench Gate Power MOSFET 89

6.1 Introduction 89

6.2 Device Structure and Proposed Fabrication Process 90

6.3 Results and Discussion 93

6.3.1 Electric Field Distribution 95

6.3.2 Current Voltage Characteristics 95

6.3.3 Improved Breakdown Performance 96

6.3.4 Heat Dissipation 98

6.3.5 Effect of L_{Gap} Variation and Misalignment 99

6.4 Conclusions 100

7 Conclusions 101

Bibliography 103

Appendix A: Creation of Device Structures in DEVEDIT 115

Appendix B: Input Decks for Simulations in ATLAS 131