REALIZATION OF SYNTHESIZED RTL STRUCTURES ON LUT ASED FPGAs

By

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DOCTOR OF PHILOSOPHY

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I N D I A

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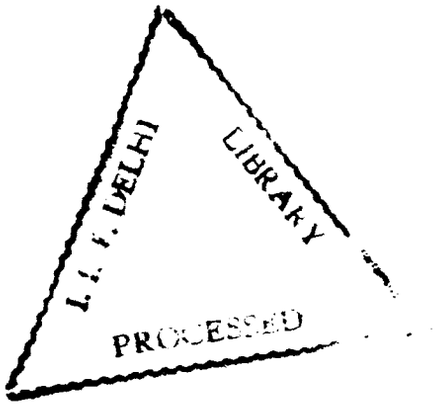
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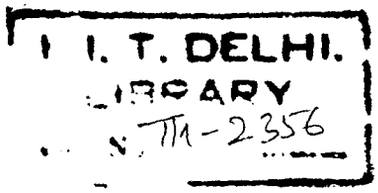
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CERTIFICATE

This is to certify that the thesis entitled *Realization of Synthesized RTL Structures on LUT based FPGAs*, being submitted by A. R. Naseer to the Indian Institute of Technology, Delhi, for the award of Degree of Doctor of Philosophy, is a bonafide research work carried out by him under our supervision and guidance. The results obtained in this thesis have not been submitted to any other university or Institute for the award of any other degree or diploma.

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Dedicated

to

my parents

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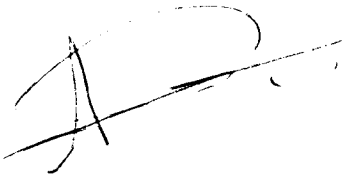

A. R. Naseer

Abstract

The Field Programmable Gate Arrays(FPGAs) provide a new approach to Application Specific Integrated Circuit(ASIC) implementation that features both large scale integration and user programmability. Short turnaround time and low manufacturing cost have made FPGA technology popular for rapid system prototyping and low to medium-volume production. The increase in complexity of FPGAs in recent years have made it possible to implement data path oriented designs on FPGAs.

Technology Mapping problem involves transforming a technology independent network into technology dependent circuits. For FPGAs, a technology dependent circuit is a collection of interconnected CLBs. This thesis addresses the problem of mapping synthesized RTL structures onto LUT based FPGAs. The key distinctive feature of our thesis is a novel approach to perform this mapping by utilizing the iterative nature of the data path components.

The RTL components are generic in nature and because of their large size, they cannot be directly mapped onto a single Configurable Logic Block(CLB). Hence a RTL component is viewed as an array of cells or slices where cell is a single-bit of a component that is iterated to form a component and slice is an array of contiguous cells of a component. The slice width is not decided a-priori, rather it is decided dynamically during the technology mapping process. For a node in the network, we define a cone rooted at that node (termed apex) as a subgraph consisting of that node and its predecessors such that any path connecting a node in the subgraph and the apex node lies entirely in the subgraph. Closely connected slices of different modules are considered together and mapped onto one or more logic blocks. Both cost-optimal and delay-minimal mappings are supported. The objective in cost-optimal mapping is to cover a given data path network with minimum number of CLBs. Similarly in delay minimal mapping the objective is to reduce the number of CLB levels in the paths corresponding to the combinational logic between the primary inputs/register outputs and register inputs/primary outputs. The mapping techniques result in a significant

reduction in CLB count and CLB levels in the critical path over manufacturer's proprietary tools and is much faster than these tools.

In this research, we also address the problem of decomposition of a function into two or more parts to be mapped onto a CLB. We propose a decomposition technique which belongs to the class of functional decomposition techniques, but is faster than these exhaustive methods. Observing that in data path designs almost all the logic encountered is completely specified, our method uses only onset of the function in contrast to exhaustive methods which require onset as well as offset. As decomposition process is compute intensive, to speed up this, we present a fast heuristic which eliminates a large number of trial partitions of the input variable set. Comparison of our decomposition approach with Roth-Karp method for some of the Logic synthesis benchmarks demonstrates the efficiency of our approach.

We also present an efficient technique for selecting an optimal clock period especially in the context of allocation of multi-cycle operators for FPGA targeted designs. In general for any technology like FPGA, where interconnection delays are significant, clock period selected ignoring the interconnection delays cannot guarantee performance. The task of selecting an optimal clock period is handled as a post technology mapping task with interconnection delays back-annotated onto the RTL structure after place and route. Experimental results on RTL structures generated from High level synthesis benchmarks show both the utility as well as the efficiency of our approach.

The data path technology mapper is integrated to a high level synthesis system and it forms a backend to the data path synthesizer. Starting from a behavioral description language and a global time constraint, RTL data path is generated automatically. This forms the input to our data path technology mapper. The output of the data path technology mapper is a CLB map of the design which can be directly placed and routed using manufacturer's layout tools.

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