

PIEZORESISTIVE SENSING AND RELIABILITY ANALYSIS OF GATE-ALL-AROUND JUNCTIONLESS TRANSISTOR

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INDIAN INSTITUTE OF TECHNOLOGY DELHI

May 2025

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PIEZORESISTIVE SENSING AND RELIABILITY ANALYSIS OF GATE-ALL-AROUND JUNCTIONLESS TRANSISTOR

by

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Centre for Applied Research in Electronics

Submitted

in fulfilment of the requirements of the degree of

DOCTOR OF PHILOSOPHY

to the



INDIAN INSTITUTE OF TECHNOLOGY DELHI

May 2025

DEDICATED TO

Papa Ji, Maa, Bhaiya, Bhabhi, Didi, Jiju, and all the teachers and professors whom I came across at different stages of my career and life have been instrumental in my development. Some motivated me, some inspired me, and many assisted in shaping the process flow of my life, often challenging me with the sharp stick of "truth", which has enabled my growth into the person I am today.

CERTIFICATE

This is to certify that the thesis entitled, “**PIEZORESISTIVE SENSING AND RELIABILITY ANALYSIS OF GATE-ALL-AROUND JUNCTIONLESS TRANSISTOR**” being submitted by **Mr. NITISH KUMAR** to the Indian Institute of Technology Delhi for the award of the degree of **Doctor of Philosophy** in the Centre for Applied Research in Electronics, is a record of the original, bona fide research work carried out by him under our guidance and supervision.

In our opinion, the thesis has reached the standard of fulfilling the requirement of all the regulations related to the award of the degree. The results contained in this thesis have not been submitted, in part or in full, to any other University or Institute for the award of any degree or diploma to the best of our knowledge.

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Acknowledgements

I would like to express my heartfelt gratitude to everyone who supported me during my thesis journey, whether directly or indirectly. Acknowledging this support is challenging, much like recognizing every neuron and synapse that contributed to this work. Even if I were to list everyone who influenced this thesis and the past three and a half years of my life, it would still feel incomplete.

First and foremost, I would like to thank my supervisors, **Prof. Pushpapraj Singh** and **Prof. Ankur Gupta**, from the bottom of my heart for their invaluable guidance, encouragement, and unwavering support throughout my thesis research journey. I would also like to express my gratitude for encouraging me to pursue my own ideas, which allowed me to work independently and implement my thoughts freely, ultimately optimizing the research budget. In addition to their academic guidance, I wish to express my admiration for my supervisors on a personal level. **Prof. Pushpapraj Singh** embodies the qualities of a classical researcher and demonstrates exceptional enthusiasm as an all-rounder cricketer, showcasing his abilities as an inspiring team leader. Meanwhile, **Prof. Ankur Gupta** possesses a remarkable gift for organizing insightful and informative presentations on research projects, all while maintaining a calm and approachable demeanor. Together, they represent the ideal supervisors a student could hope for. Lastly, their diverse strengths not only enrich my approach to research and my academic experience but also serve as a profound source of inspiration.

I would like to extend my sincere gratitude to my research committee members, **Prof. Monika Aggarwal**, **Prof. Abhisek Dixit**, and **Prof. Samaresh Das**, for their thoughtful feedback and unwavering encouragement. Your diverse perspectives have challenged me to think critically and have significantly deepened my understanding of the subject matter.

I would also like to express my gratitude to **Prof. Subhas Chandra Mukhopadhyay**, for his assistance in helping me achieve the AIRS Fellow 2023, which allowed me to visit Macquarie University Sydney, Australia. My sincere gratitude is extended to my mentors, **Prof. Francky Catthoor**, **Dr. Dwaipayan Biswas**, **Dr. Venkateswarlu Sankatali**, **Dr. Subrat Mishra**, and the **Thermal & Mechanical Characterization Team** at IMEC and KU Leuven, Belgium, for granting me the esteemed

opportunity to serve as a Visiting Researcher and International Scholar. Their unwavering support throughout my exposure to System-on-Chip (SoC) thermal reliability analysis and their invaluable suggestions have been instrumental in my academic development. I am also grateful to my friend **Dr. Yukai Chen** for discussing both technical and non-technical team challenges and for sharing ideas for their resolution with me.

At the CARE Microelectronics Group, I extend my heartfelt thanks to everyone, especially those who contributed significantly to this research. Thank you to **Dr. Pragyey Kumar Kaushik, Dr. Sushil Kumar, Dr. Vaibhav Rana, Dr. Aakanksha Mishra, and Dr. Shraddha Pali** for sharing your knowledge whenever I found myself stuck in my thinking. I appreciate the company of former and current researchers, especially including the above members **Dr. Dhairya Singh Arya, Dr. Manu Garg, Mr. Mujeeb Yousuf, Dr. Akhil K. Ramesh, Dr. Sumit Sharma, and Mr. Vikash Sharma**. They have made valuable contributions to this work through discussions and suggestions. A special thanks to my best friends, **Ms. Himanshi Awasthi** and **Mr. Khanjan Joshi**, for every moment of sharing and their unwavering emotional support. I also want to thank my friend **Ms. Mudra Chavda** for sharing in my joyful celebrations and for having lunches and dinners together. I am also eternally grateful to my M.Tech supervisors, **Dr. Vaibhav Purwar** and **Dr. Abhinav Gupta**, for their support in helping me reach the esteemed platform of CARE, IIT Delhi. I was also fortunate to have the opportunity to mentor several M.Tech and PhD students. I also wish to acknowledge all the travel grants that have helped me connect with the research community beyond India: the ITS-SERB Grant, RSTA (IITD), RETA (IITD), IEEE SENSORS Travel Grant, and IMEC (Belgium). I would also like to thank all the resource personnel at IIT Delhi for their administrative support. I extend my special thanks to the Office staff (**Mr. Sameer Hansda**) for their polite and helpful nature.

Most importantly, my long tenure as a graduate student would not have been possible without the support and patience of my **loving family**. I would like to express my deepest gratitude to my extraordinary family for instilling the value of education in me, especially my **father (Mr. Brijesh Prasad Gupta), mother (Mrs. Sugandhi Devi), elder brother (Mr. Satish Kumar), and sister-in-law (Mrs. Bebi Kumari)**. Their love and support have encouraged me to persevere throughout this endeavor. I must say that because of them, a farmer's son has become a specialist in device development and reliability co-optimization.

NITISH KUMAR

Abstract

Junctionless nanowire (JL-NW) gate-all-around (GAA) field-effect transistors (FETs) are widely investigated as reliable switching solutions for computing technologies (both memory and logic) and as highly sensitive piezoresistive sensing elements in the subthreshold regime. They offer high ON/OFF switching ratios, very low OFF-state leakage currents, and relatively better performance under harsh environmental conditions. Despite the advantages, electro-thermal and electro-mechanical reliability are significant concerns in computing electronics applications, particularly regarding thermal and mechanical stress (MS) reliability and performance. The self-heating effect necessitates optimization for better thermal management in ON-state transistors, requiring control over process variation effects on device thermal conductivity through careful optimization of fabrication processes and device characteristics. Moreover, the 3D integration and packaging of chips introduce tensile and compressive MS that can impact device performance and leakage reliability. This MS ultimately influences the switching threshold and is closely related to the device's characteristics. The induced MS also contributes to piezoresistive behavior. Therefore, the proposed devices are investigated not only as piezoresistive sensing elements but also for their reliability in terms of sensing resolution. This thesis aims to address critical issues related to thermal management, MS effects, and piezoresistive sensing applications, particularly in light of scaling limitations.

This thesis is organized into three major themes, outlined as follows. The first half discusses the development of a compact thermal conductivity model to capture the effects of process variation in analyzing the thermal implications and reliability of long-channel devices and advanced-node junctionless devices. The proposed model is easy to implement in any finite element method (FEM) simulator and calculates the thermal conductivity of each region or layer, considering the effects of temperature, thickness, doping concentration, and type of doping. Using this model, the electro-thermal behavior is mapped onto a long-channel experimental device with the Sentaurus TCAD simulator. Furthermore, the electro-thermal behavior is analyzed in advanced nodes and co-optimized for improved thermal reliability. Additionally, the thermal reliability of junctionless devices is examined in terms of hot carrier injection (HCI) lifetime and bias temperature instability (BTI) lifetime degradation, specifically in relation to the maximum lattice temperature ($T_{L,max}$) and the gap

variation between two nanowires. The comparative study for electro-thermal performance analysis of junctionless and inversion mode nanowire GAA FETs is also presented in advanced technology nodes by considering nonlocal effects.

Next, as one-fourth of the thesis, the gate-induced drain leakage (GIDL) current, HCI, and variation of the electrical parameters to analyze the performance are investigated with the uniaxial tensile MS from a few MPa to GPa levels. GIDL is observed to increase exponentially, while some hot electrons are trapped in the gate oxide, leading to a nearly linear increase in HCI and gate leakage current with the induced MS. The ON-state current, carrier mobility, threshold voltage, and subthreshold swing are directly proportional to the induced MS due to the reduced energy band gap and intervalley scattering effect. The reduced subthreshold swing shows low power consumption and better switching ability in advanced CMOS technologies. Thus, this study demonstrates the importance of MS engineering for performance improvement in CMOS technology and highlights the importance of MS in device reliability. In addition, the change of drain current shows highly piezoresistive sensing ability in nanoelectromechanical sensor applications.

Thus, last as one-fourth of the thesis, a tunable piezoresistive pressure sensor is designed and developed using JL-NW FETs integrated into a circular diaphragm. The measured results show that the piezoresistive sensitivity is improved in the subthreshold regime (depletion regime) compared to the ON-state condition (partial depletion regime). This improvement is achieved by reducing the channel conductivity with a low gate bias below the threshold voltage. Additionally, LFN is measured to estimate the MDS and SNR. These measurements indicate that the JL-NW GAA FET offers higher resolution and better performance as a sensing element compared to the inversion mode NW GAA FET in advanced technology nodes. Furthermore, the limitations of the scaling factor on piezoresistive sensitivity are analyzed and co-optimized by considering the design of uniform MS on the multi-nanosheet channels in advanced nodes. These results show better sensing resolution, it is also much easier to integrate with advanced CMOS technologies.

In the three parts of this thesis, the co-optimization solutions for thermal and mechanical reliability, along with piezoresistive sensitivity derived from the research presented, could lead to enhanced electro-thermal and electro-mechanical reliability of junctionless devices. This improvement impacts their performance as piezoresistive sensing elements in advanced electronics applications.

सार

जंक्शनलेस नैनोवायर (जेएल-एनडब्ल्यू) गेट-ऑल-अराउंड (जीएए) फील्ड-इफेक्ट ट्रांजिस्टर (एफईटी) की कंप्यूटिंग प्रौद्योगिकियों (मेमोरी और लॉजिक दोनों) के लिए विश्वसनीय स्विचिंग समाधान और सबथ्रेशोल्ड शासन में अत्यधिक संवेदनशील पीज़ोरेसिस्टिव सेंसिंग तत्वों के रूप में व्यापक रूप से जांच किया गया है। ये उच्च चालू/बंद स्विचिंग अनुपात, बहुत कम ऑफ-स्टेट रिसाव धाराएं, और कठोर पर्यावरणीय परिस्थितियों में अपेक्षाकृत बेहतर प्रदर्शन प्रदान करते हैं। इसके बावजूद, इलेक्ट्रो-थर्मल और इलेक्ट्रो-मैकेनिकल विश्वसनीयता कंप्यूटिंग इलेक्ट्रॉनिक्स अनुप्रयोगों में महत्वपूर्ण चिंताये हैं, खासकर थर्मल और मैकेनिकल तनाव (एमएस) विश्वसनीयता और प्रदर्शन के संबंध में। स्व-हीटिंग प्रभाव को ऑन-स्टेट ट्रांजिस्टर में बेहतर थर्मल प्रबंधन के लिए अनुकूलन की आवश्यकता होती है, जिसके लिए निर्माण प्रक्रियाओं और डिवाइस विशेषताओं के सावधानीपूर्वक अनुकूलन के माध्यम से डिवाइस थर्मल चालकता पर प्रक्रिया भिन्नता प्रभावों पर नियंत्रण की आवश्यकता होती है। इसके अलावा, चिप का 3डी एकीकरण और पैकेजिंग तन्म और संपीडित एमएस पेश करता है, जो डिवाइस के प्रदर्शन और रिसाव विश्वसनीयता को प्रभावित कर सकता है। यह एमएस अंततः स्विचिंग थ्रेशोल्ड को प्रभावित करता है जो की डिवाइस की विशेषताओं से संबंधित है। प्रेरित एमएस पीज़ोरेसिस्टिव व्यवहार में भी योगदान देता है। इसलिए, प्रस्तावित उपकरणों की जांच न केवल पीज़ोरेसिस्टिव सेंसिंग तत्वों के रूप में की गई है, बल्कि सेंसिंग रिज़ॉल्यूशन के संदर्भ में उनकी विश्वसनीयता की भी जांच की गई है। इस थीसिस का मुख उद्देश्य थर्मल प्रबंधन, एमएस प्रभाव, और पीज़ोरेसिस्टिव सेंसिंग अनुप्रयोगों से संबंधित महत्वपूर्ण मुद्दों को संबोधित करना है, विशेष रूप से स्केलिंग सीमाओं पे प्रकाश डालते हुए।

इस थीसिस को तीन प्रमुख विषयों में व्यवस्थित किया गया है, जिनकी रूपरेखा इस प्रकार है। पहले भाग में लंबे-चैनल उपकरणों और उन्नत-नोड जंक्शन रहित उपकरणों के थर्मल निहितार्थ और विश्वसनीयता का विश्लेषण करने में प्रक्रिया भिन्नता के प्रभावों को पकड़ने के लिए एक कॉम्पैक्ट थर्मल चालकता मॉडल की विकास पर चर्चा की गई है। प्रस्तावित मॉडल किसी भी परिमित तत्व विधि (एफईएम) सिम्युलेटर में लागू करना आसान है और तापमान, मोटाई, डोपिंग एकाग्रता, और डोपिंग के प्रकार के प्रभावों पर विचार करते हुए प्रत्येक क्षेत्र या परत की थर्मल चालकता की गणना की जा सकती है। इस मॉडल का उपयोग करके, इलेक्ट्रो-थर्मल व्यवहार को सेंटोरस टीसीएडी सिम्युलेटर के साथ एक लंबे चैनल प्रयोगात्मक डिवाइस पर मैप किया गया है। इसके अलावा, इलेक्ट्रो-थर्मल व्यवहार का उन्नत नोड्स में विश्लेषण किया गया है और बेहतर थर्मल विश्वसनीयता के लिए सह-अनुकूलित की गई है। इसके अतिरिक्त, जंक्शन रहित उपकरणों की थर्मल विश्वसनीयता की जांच गर्म वाहक इंजेक्शन (एचसीआई) जीवनकाल और पूर्वाग्रह तापमान अस्थिरता (बीटीआई) जीवनकाल गिरावट के संदर्भ में की गई है, विशेष रूप से अधिकतम जाली तापमान (टीएल, अधिकतम) और दो नैनोवायरों के बीच अंतर भिन्नता के संबंध में। जंक्शन रहित और व्युत्क्रम मोड नैनोवायर

जीएफ एफईटी के इलेक्ट्रो-थर्मल प्रदर्शन विश्लेषण के लिए तुलनात्मक अध्ययन भी गैर-स्थानीय प्रभावों पर विचार करके उन्नत प्रौद्योगिकी नोड्स में प्रस्तुत किया गया है।

इसके बाद, थीसिस के एक-चौथाई भाग में, गेट-प्रेरित नाली रिसाव (जीआईडीएल) वर्तमान, एचसीआई, और प्रदर्शन का विश्लेषण करने के लिए विद्युत मापदंडों की भिन्नता की जांच कुछ एमपीए से जीपीए स्तरों तक एकअक्षीय तन्यता एमएस के साथ की गई है। जीआईडीएल में तेजी से वृद्धि देखी गई है, जबकि कुछ गर्म इलेक्ट्रॉन गेट ऑक्साइड में फंस जाते हैं, जिससे प्रेरित एमएस के साथ एचसीआई और गेट लीकेज करंट में लगभग रैखिक वृद्धि होती है। कम ऊर्जा बैंड गैप और इंटरवलली स्कैटरिंग प्रभाव के कारण ऑन-स्टेट करंट, कैरियर मोबिलिटी, थ्रेशोल्ड वोल्टेज, और सबथ्रेशोल्ड स्विंग प्रेरित एमएस के सीधे आनुपातिक हैं। कम सबथ्रेशोल्ड स्विंग उन्नत सीएमओएस प्रौद्योगिकियों में कम बिजली की खपत और बेहतर स्विचिंग क्षमता को दर्शाता है। इस प्रकार, यह अध्ययन सीएमओएस प्रौद्योगिकी में प्रदर्शन सुधार के लिए एमएस इंजीनियरिंग के महत्व को प्रदर्शित करता है और डिवाइस विश्वसनीयता में एमएस के महत्व पर प्रकाश डालता है। इसके अलावा, ड्रेन करंट का परिवर्तन नैनोइलेक्ट्रोमैकेनिकल सेंसर अनुप्रयोगों में अत्यधिक पीज़ोरेसिस्टिव सेंसिंग क्षमता को दर्शाता है।

इस प्रकार, थीसिस के अंतिम एक-चौथाई भाग में, एक ट्यून करने योग्य पीज़ोरेसिस्टिव प्रेशर सेंसर को एक गोलाकार डायफ्राम में एकीकृत जेएल-एनडब्ल्यू एफईटी का उपयोग करके डिजाइन और विकसित किया गया है। मापे गए परिणामों से पता चलता है कि ऑन-स्टेट स्थिति (आंशिक कमी शासन) की तुलना में सबथ्रेशोल्ड शासन (कमी शासन) में पीज़ोरेसिस्टिव संवेदनशीलता में सुधार हुआ है। यह सुधार थ्रेशोल्ड वोल्टेज के नीचे कम गेट पूर्वाग्रह के साथ चैनल चालकता को कम करके प्राप्त किया जाता है। इसके अतिरिक्त, एमडीएस और एसएनआर का अनुमान लगाने के लिए एलएफएन को मापा गया है। इन मापों से संकेत मिलता है कि जेएल-एनडब्ल्यू जीएफ एफईटी उन्नत प्रौद्योगिकी नोड्स में व्युत्क्रम मोड एनडब्ल्यू जीएफ एफईटी की तुलना में एक सेंसिंग तत्व के रूप में उच्च रिज़ॉल्यूशन और बेहतर प्रदर्शन प्रदान करता है। इसके अलावा, उन्नत नोड्स में मल्टी-नैनोशीट चैनलों पर समान एमएस के डिजाइन पर विचार करके पीज़ोरेसिस्टिव संवेदनशीलता पर स्केलिंग कारक की सीमाओं का विश्लेषण और सह-अनुकूलित की गई है। ये परिणाम बेहतर सेंसिंग रिज़ॉल्यूशन दिखाते हैं, उन्नत सीएमओएस प्रौद्योगिकियों के साथ एकीकृत करना भी बहुत आसान है।

इस थीसिस के तीन भागों में अध्ययन ये दर्शाता है की, थर्मल और मैकेनिकल विश्वसनीयता के लिए सह-अनुकूलन समाधान, प्रस्तुत शोध से प्राप्त पीज़ोरेसिस्टिव संवेदनशीलता के साथ, जंक्शन रहित उपकरणों की इलेक्ट्रो-थर्मल और इलेक्ट्रो-मैकेनिकल विश्वसनीयता को बढ़ाया जा सकता है। यह सुधार उन्नत इलेक्ट्रॉनिक्स अनुप्रयोगों में पीज़ोरेसिस्टिव सेंसिंग तत्वों के रूप में उनके प्रदर्शन को प्रभावित करता है।

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List of Abbreviations

CMOS	Complementary Metal-Oxide-Semiconductor
NW	Nanowire
GAA	Gate-All-Around
MOS	Metal-Oxide-Semiconductor
FETs	Field-Effect-Transistors
IRDS	International Roadmap for Devices and Systems
HCI	Hot-carrier injection
BTI	Bias Temperature Instability
BOX	Buried-Oxide
SHEs	Self-Heating Effects
ICs	Integrated-Circuits
F2F	Face-to-Face
BS-PDN	Backside-Power Delivery Network
MoL	Memory-on-Logic
SoCs	System-on-Chips
FEOL	Front-End-Of-Line
PDN	Power Delivery Network
BPR	Buried Power Rail
n-TSV	Nano-Through-Silicon-Vias
GPa	Gigapascals
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MuG	Muti-Gate
DIBL	Drain-Induced Barrier Lowering
SCEs	Short-Channel Effects

JL-NW	Junctionless Nanowire
JL	Junctionless
IM	Inversion Mode
AM	Accumulation Mode
CPU	Central Processing Unit
DD	Drift-Diffusion
KE	Kinetic Energy
MPa	Megapascals
TCAD	Technology Computer-Aided Design
DC	Direct Current
FoMs	Figure-of-Merits
NEMS	Nanoelectromechanical System
LFN	Low-Frequency Noise
MDS	Minimum Detectable Strain
SNR	Signal-to-Noise Ratio
FEM	Finite Element Method
SOI	Silicon-on-Insulator
MFP	Mean Free Path
SS	Subthreshold Slope
JL-MNW	Junctionless Multi-Nanowire
BEOL	Back-End-Of-Line
LPCVD	Low-Pressure Chemical Vapor Deposition
HD	Hydrodynamic
SRH	Shockley-Read-Hall
QC	Quantum Confinement
BTE	Boltzmann Transport Equation
RT	Rise Time

FT	Fall Time
OT	OFF Time
PT	Pulse Time
GHz	Gigahertz
MS	Mechanical Stress
GIDL	Gate-Induced Drain Leakage
BTBT	Band-to-Band Tunneling
HC	Hot-Carrier
UV	Ultraviolet
DRIE	Deep Reactive Ion Etching
BHF	Buffered Hydrofluoric Acid
CVD	Chemical Vapor Disposition
W	Weight
CC	Constant Current
SD	Second Derivative
MF	Multiplication Factor
TaN	Tantalum Nitride
Al	Aluminum
MEMS	Microelectromechanical System
SEM	Scanning Electron Microscope
D2D	Device-to-Device
GF	Gauge Factor
NS	Nanosheet

