

IMPACT IONIZATION BASED TRANSISTORS: DESIGN, SIMULATIONS AND APPLICATIONS

AVINASH LAHGERE



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IMPACT IONIZATION BASED TRANSISTORS: DESIGN, SIMULATIONS AND APPLICATIONS

by

AVINASH LAHGERE

Department of Electrical Engineering

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Dedicated

to

*Dadi ji, Mommy, Papa, brothers, sister, my wife and all the teachers whom I came
across at different stages during the last 27 years of my life.*

Certificate

This is to certify that the thesis entitled **Impact Ionization Based Transistors: Design, Simulations and Applications** being submitted by **Mr. AVINASH LAHGERE** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, **Indian Institute of Technology Delhi**, is a record of bonafide work done by him under my supervision and guidance. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

To the best of my knowledge, the matter embodied in this thesis has not been submitted to any other University or Institute for the award of any degree or diploma.

Date:

Place: New Delhi

Dr. Mamidala Jagadesh Kumar

Professor

Department of Electrical Engineering

Indian Institute of Technology Delhi

New Delhi - 110016, INDIA

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Abstract

As the dimensions of the conventional metal oxide semiconductor field effect transistors (MOSFETs) are aggressively scaling down, the conventional MOSFETs have obtained amazing packaging density onto the same silicon wafer. However, the scaling of the conventional MOSFETs has reached its physical limits in particularly due to the subthreshold swing (SS), which is difficult to scale down below 60 mV/decade at room temperature. Thus, the static power consumption in integrated circuits (ICs) is progressively increasing with conventional MOSFET scaling.

The impact ionization metal oxide semiconductor (I-MOS) transistors have captivated immense attention due to its capability to overcome the physical constraints of the conventional MOSFET. I-MOS works on the principle of modulation of channel length or modulation of avalanche effect and shows very steep SS of the order of ~ 4 to 5 mV/decade. However, I-MOS has two major shortcomings: (i) higher supply voltage and (ii) poor gate oxide reliability due to hot carrier injection, which needs to be addressed for its commercialization.

Recently, the Bipolar I-MOS has been reported in the literature, which has symmetric doping in the source and the drain regions, unlike the conventional I-MOS. The Bipolar I-MOS has the ability to overcome the aforementioned challenges of the conventional I-MOS, which exhibits avalanche breakdown voltage of the order of ~ 2.85 V and better reliability in comparison to the conventional I-MOS. However, the breakdown voltage of the Bipolar I-MOS can be further reduced for memory applications. In addition, the presence of the snapback in the output characteristics of the Bipolar I-MOS can be explored for realizing 1-transistor (1-T) capacitorless DRAM. Therefore, this dissertation is focused on reducing the breakdown voltage of the Bipolar I-MOS and its application for realizing 1-T capacitorless DRAM.

The first device that is proposed is the charge plasma N-P-N impact ionization MOS (I-MOS). The proposed device is made on lightly doped P-type silicon film using the charge plasma concept. The proposed device does not have metallurgical junctions and needs no chemical doping for creating the source and the drain regions. Therefore, the proposed device combines the benefits of

the Bipolar I-MOS (low avalanche breakdown voltage and immunity towards the hot carrier injection) and a junctionless field effect transistor (JLFET) (low thermal budget process). The proposed charge plasma N-P-N I-MOS exhibits excellent electrical characteristics such as a low avalanche breakdown voltage compared to the conventional Bipolar I-MOS, which is due to the enhanced current gain mechanism. Moreover, the proposed device also obviates the need for complex ion-implantation and annealing or thermal diffusion processes, which makes the device fabrication simpler.

The second device that is demonstrated is a bandgap-engineered silicon-germanium bipolar I-MOS. The silicon-germanium Bipolar I-MOS employs a low-bandgap material $\text{Si}_{0.6}\text{Ge}_{0.4}$ in the channel region by keeping the source and the drain semiconductor material as silicon in comparison to the conventional Bipolar I-MOS. The use of low-bandgap material $\text{Si}_{0.6}\text{Ge}_{0.4}$ in existing conventional Bipolar I-MOS results in a lower breakdown voltage due to higher impact ionization rate. Moreover, the same device is extended for realizing a 1-T capacitorless DRAM. In a silicon-germanium Bipolar I-MOS based 1-T capacitorless DRAM, the 1-state current level is triggered by the excess hole charge generated into the body due to impact ionization.

The third and the final device that is investigated is a 1-T capacitorless DRAM using laterally bandgap engineered Si-Si:C heterostructure Bipolar I-MOS. The proposed device features a high-K gate dielectric, a metal gate, and an epitaxially grown $\text{Si}_{0.99}\text{C}_{0.01}$ source/drain regions. The lattice-mismatch between the Si:C source/drain and the Si channel results in strain effect, hence, the proposed 1-T capacitorless DRAM memory cell exhibit enhanced memory characteristics, particularly, the sensing margin, and the retention time.

The work presented in this thesis demonstrates the possible potential of Bipolar I-MOS in different applications where the steep subthreshold slope is an essential requirement.

सार

पारंपरिक metal oxide semiconductor ट्रांजिस्टर (MOSFETs) के आयाम आक्रामक रूप से स्केल कर रहे हैं, पारंपरिक MOSFET ने उसी सिलिकॉन वेफर पर अद्भुत पैकेजिंग घनत्व प्राप्त किया है। हालांकि, परंपरागत MOSFET का स्केलिंग विशेष रूप से सबथ्रेशोल्ड स्विंग (SS) के कारण अपनी शारीरिक सीमा तक पहुंच गया है, जो कमरे के तापमान पर 60 mV/decade से नीचे स्केल करना मुश्किल है। इस प्रकार, एकीकृत सर्किट (IC) में स्थिर बिजली खपत पारंपरिक MOSFET स्केलिंग के साथ क्रमिक रूप से बढ़ रही है।

Impact ionization metal ऑक्साइड सेमीकंडक्टर (I-MOS) ट्रांजिस्टर ने पारंपरिक MOSFET की शारीरिक बाधाओं को दूर करने की अपनी क्षमता के कारण अत्यधिक ध्यान आकर्षित किया है। आई-एमओएस चैनल मॉडुलन या breakdown voltage प्रभाव के मॉड्यूलेशन के सिद्धांत पर काम करता है और ~ 4 से 5 mV/decade के आदेश के बहुत तेज एसएस दिखाता है। हालांकि, I-MOS में दो प्रमुख कमियां हैं: (i) उच्च आपूर्ति वोल्टेज और (ii) गर्म वाहक इंजेक्शन के कारण खराब गेट ऑक्साइड विश्वसनीयता, जिसे इसके व्यावसायीकरण के लिए संबोधित करने की आवश्यकता है।

हाल ही में, साहित्य में Bipolar I-MOS की सूचना मिली है, जिसमें सममित डोपिंग है, source और drain क्षेत्रों में परंपरागत आई-एमओएसकी उपरोक्त चुनौतियों को दूर करने की क्षमता, जो प्रदर्शित करता है ~ 2.85 V के आदेश का हिमस्खलन टूटने वोल्टेज और तुलना में बेहतर विश्वसनीयता पारंपरिक आई-एमओएस। हालांकि, द्विध्रुवीय आई-एमओएसका ब्रेकडाउन वोल्टेज आगे हो सकता है स्मृति अनुप्रयोगों के लिए कम किया गया। इसके अलावा, आउटपुट में स्नैपबैक की उपस्थिति द्विध्रुवीय आई-एमओएस की विशेषताओं को 1-ट्रांजिस्टर (1-टी) कैपेसिटरलेस को महसूस करने के लिए खोजा जा सकता है DRAM। इसलिए, यह शोध प्रबंध द्विध्रुवीय के ब्रेकडाउन वोल्टेज को कम करने पर केंद्रित है आई-एमओएस और 1-टी कैपेसिटरलेस डीआरएएम को साकार करने के लिए इसका आवेदन।

प्रस्तावित पहला उपकरण charge plasma N-P-N impact ionization MOS (I-MOS) है। प्रस्तावित डिवाइस charge plasma अवधारणा का उपयोग करके हल्के ढंग से डॉप किए गए P-type सिलिकॉन फिल्म पर बनाया गया है। प्रस्तावित डिवाइस में मेटलर्जिकल जंक्शन नहीं हैं और इसके लिए कोई रासायनिक डोपिंग की आवश्यकता नहीं है source और drain क्षेत्रों का निर्माण। इसलिए, प्रस्तावित डिवाइस के लाभ को जोड़ती Bipolar I-MOS (कम breakdown वोल्टेज और hot carrier injection की ओर प्रतिरक्षा) और एक junctionless field effect ट्रांजिस्टर (JLFET) (कम थर्मल बजट प्रक्रिया)। प्रस्तावित चार्ज प्लाज्मा एन-पी-एन आई-एमओएसउत्कृष्ट विद्युत विशेषताओं जैसे कि कम दिखाता है परंपरागत द्विध्रुवीय आई-एमओएसकी तुलना में हिमस्खलन टूटने वोल्टेज, जो कि के कारण है बढ़ाया वर्तमान लाभ तंत्र। इसके अलावा, प्रस्तावित डिवाइस भी आवश्यकता को रोकता है जटिल आयन-इम्प्लान्टेशन और एनीलिंग या थर्मल प्रसार प्रक्रियाएं, जो डिवाइस बनाती हैं निर्माण आसान है।

प्रदर्शित किया गया दूसरा उपकरण एक बैंडगैप-इंजीनियर सिलिकॉन-जर्मेनियम द्विध्रुवीय आईएमओएस है। सिलिकॉन-जर्मेनियम द्विध्रुवीय I-MOS एक कम बैंडगैप सामग्री $\text{Si}_{0.6}\text{Ge}_{0.4}$ को नियोजित करता है सिलिकॉन के रूप में स्रोत और नाली अर्धचालक सामग्री को रखकर चैनल क्षेत्र पारंपरिक द्विध्रुवीय I-MOS की तुलना में कम बैंडगैप सामग्री $\text{Si}_{0.6}\text{Ge}_{0.4}$ में उपयोग करें मौजूदा पारंपरिक द्विध्रुवीय I-MOS के परिणामस्वरूप उच्च प्रभाव के कारण कम ब्रेकडाउन वोल्टेज में परिणाम होता है आयनीकरण दर। इसके अलावा, एक ही डिवाइस को 1-टी कैपेसिटरलेस डीआरएएम को साकार करने के लिए बढ़ाया जाता है। एक सिलिकॉन-जर्मेनियम द्विध्रुवीय आई-एमओएसआधारित 1-टी कैपेसिटरलेस डीआरएएम में, 1-राज्य वर्तमान स्तर प्रभाव आयनीकरण के कारण शरीर में उत्पन्न अतिरिक्त छेद चार्ज से ट्रिगर किया जाता है।

जांच की गई तीसरी और अंतिम डिवाइस बाद में उपयोग करके 1-टी कैपेसिटरलेस डीआरएएम है बैंडगैप इंजीनियर सी-सी: सी हेटेरोस्ट्रक्चर द्विध्रुवीय आई-एमओएस। प्रस्तावित डिवाइस में एक उच्च- के गेट ढांकता हुआ, एक धातु द्वार, और एक epitaxially उगाया $\text{Si}_{0.99}\text{C}_{0.01}$ स्रोत / नाली क्षेत्रों लैटिसमिसमैच सी: सी स्रोत / नाली और सी चैनल के बीच तनाव प्रभाव में परिणाम, इसलिए, प्रस्तावित 1-टी कैपेसिटरलेस डीआरएएम मेमोरी सेल प्रदर्शनी बढ़ाया स्मृति विशेषताओं, विशेष रूप से, संवेदन मार्जिन, और प्रतिधारण समय। इस थीसिस में प्रस्तुत किया गया कार्य द्विध्रुवीय आई-एमओएस की संभावित क्षमता को दर्शाता है विभिन्न अनुप्रयोग जहां खड़ी subthreshold ढलान एक आवश्यक आवश्यकता है।

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