DC TO RF CHARACTERIZATION, MODELING, AND SIMULATION OF MULTIPLE-GATE FETS IN SUB-14NM CMOS TECHNOLOGIES

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JUNE 2019

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by

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Submitted

in fulfilment of the requirements of the degree of Doctor of Philosophy

to the

INDIAN INSTITUTE OF TECHNOLOGY DELHI

JUNE 2019

Certificate

This is to certify that the thesis entitled ***"DC to RF Characterization, Modeling, and Simulation of Multiple-Gate FETs in Sub-14nm CMOS Technologies"***, being submitted by **Ramendra Singh** to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering and is a record of the original bonafide research work carried out by him. The results presented in the thesis have not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

I certify that he has pursued the prescribed course of research.

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Acknowledgements

This thesis would not be possible without the help of many people. Firstly, I would like to express my sincere gratitude to my supervisor Prof. Abhisek Dixit for the continuous support of my Ph.D study and related research. His motivation, and immense knowledge always enhanced my research-abilities throughout the course of learning from him. His guidance helped me in research all the time and writing of this thesis.

Besides my advisor, I express my sincere thank to Prof. Yogesh S. Chauhan, Electrical Department, IIT Kanpur for his sincere advice and encouragement, but also for the hard question which incented me to widen my research from various perspectives.

I would like to thank the rest of my thesis committee: Prof. Madhusudan Singh, Prof. Manan Suri, and Prof. P. R. Panda, for their insightful comments and encouragement.

I would also like to thank our industry collaborator Reinaldo Vega and Terence B. Hook at IBM Research Group, Albany, USA, and Bertrand Parvais at IMEC, Belgium for their valuable and expert comments.

I would like to thank the Department of Information Technology, Govt. of India, for the instrumentation setup for the Device and Wafer Level Characterization laboratory, through SERB , under grant SB/S3/EECE/037/2014, and through TSG, under grant DST/TSG/AMT/2015/339.

I thank my fellow labmates in for creating and maintaining enthusiastic environment in the lab, and for all the fun we have had in the last four years. Thanks to Anil, Kritika, Charu, Anshul, Chandan, Ishita, Manoj, Shivendra and Pritam, who have been there to support me. I would like to acknowledge Anshul and Anil for their technical inputs during the TCAD simulations of the devices. Special acknowledgements to Kritika and Charu for free ranging technical discussions on various topics and also, helped me in research writing.

Last but not the least, I express my deep heartfelt gratitude to my respected parents for their blessings and supporting me spiritually throughout writing this thesis. Special thanks to my beloved wife for coming into my life, and always my support in the moments when there was no one to answer my queries. I am also thankful to my younger brother and sister for their support and understanding. . .

Ramendra Singh

Abstract

Multiple-gate FETs are the device architecture of choice beyond 22 nm node CMOS devices. To suppress the short channel effects below 10nm node, gate-all-around NWFETs, along with some novel structure like inserted-oxide FinFET and negative capacitance based CMOS devices are the promising candidates. This thesis presents DC/RF characterization, simulation, and modeling of these structures. As feature size approaches sub-10nm regime, process variation which is a naturally occurring phenomenon becomes prominent. This causes measurable variance in output characteristics of all circuits and it also degrades the manufacturing yield. In this thesis, DC model parameters of NWFETs are extracted and process variations have been modeled, using the BSIM-CMG model card by performing Monte Carlo simulations. The NWFETs used in this work are designed with vertically stacked nanowires in order to attain the same current density and equivalent layout area efficiency as FinFETs. This significantly surge the process complexity in NWFETs as compared to FinFETs. Inserted-oxide FinFET (iFinFET), which is recently proposed as another multigate transistor, has similar fabrication process flow as FinFETs, yet it achieves better device performance. In this thesis, parasitic capacitance in Inserted-Oxide FinFETs is modeled analytically using conformal mapping techniques.

With continued device scaling, NWFETs may be considered by industry, since it provides the best electrostatic control of the channel due to gate all around geometry. However, self-heating effect in NWFETs is a major concern due to their strong confined geometry. In this thesis, self-heating effect is characterized in NWFETs using small-signal output conductance technique and analog/RF figures of merit of these NWFETs have been investigated. To reduce the power density in the modern processors, the transistors with steeper slope or lower subthreshold swing (SS) are preferred. Ferroelectric based negative capacitance FETs (NC-FETs) are the emerging devices with lower SS (< 60mV/decade). In this thesis, RF performance of NC-FinFET is investigated using BSIM-CMG compact model extracted from DC and RF measured data of 10nm technology node bulk FinFET devices. A globally scalable RF model usable for the low power and high-frequency applications has been reported with detailed model description of NC-FinFET.

सार

22nm नोड CMOS डिवाइस से परे के लिए मल्टीपल गेट FET आर्किटेक्चर पसंदीदा डिवाइस है। 10nm नोड के नीचे लघु चैनल प्रभाव को दबाने के लिए, गेट-ऑल-अराउंड NWFETs के साथ कुछ नवीन संरचना जैसे सम्मिलित-ऑक्साइड FinFET तथा नकारात्मक धारिता पर आधारित CMOS डिवाइस होनहार उम्मीदवार हैं। यह थीसिस इन संरचनाओं के डीसी / आरएफ लक्षण वर्णन, सिमुलेशन और मॉडलिंग प्रस्तुत करता है। जैसे डिवाइस आकृति उप-10nm के पास पहुंचती है, प्रक्रिया भिन्नता जो की स्वाभाविक रूप से होने वाली घटना है प्रमुख हो जाती है। इसकी वजह से सभी सर्किट के आउटपुट विशेषताओं में औसत दर्जे का विचरण तथा विनिर्माण प्राप्ति में कमी आ जाती है। इस थीसिस में, NWFETs के डीसी मॉडल मापदंडों को निकाला गया है और BSIM-CMG मॉडल कार्ड का उपयोग करके मोंटे कार्लो सिमुलेशन प्रदर्शन करके प्रक्रिया भिन्नता को मॉडल किया गया है। FinFETs की तरह वर्तमान घनत्व और समकक्ष लेआउट क्षेत्र दक्षता प्राप्त करने के लिए, इस काम में इस्तेमाल किए गए NWFETs को क्रम में खड़ी स्टैक्ड नैनोवायर के साथ डिज़ाइन किया गया है। इस वजह से FinFETs की तुलना में NWFETs में प्रक्रिया की जटिलता में काफी वृद्धि हुई है। सम्मिलित-ऑक्साइड FinFET (iFinFET), जो हाल ही में प्रस्तावित एक और मल्टीगेट ट्रांजिस्टर के रूप में, FinFETs की तरह समान निर्माण प्रक्रिया प्रवाह है, फिर भी यह बेहतर डिवाइस प्रदर्शन प्राप्त करता है। इस थीसिस में, सम्मिलित-ऑक्साइड FinFET में परजीवी समाई को कंफर्मल मैपिंग तकनीक का उपयोग करके विश्लेषणात्मक रूप से मॉडल किया गया है।

निरंतर डिवाइस स्केलिंग के साथ, NWFET को उद्योग द्वारा माना जा सकता है, क्योंकि ज्यामिति के चारों ओर गेट के कारण यह चैनल का सबसे अच्छा इलेक्ट्रोस्टैटिक नियंत्रण प्रदान करता है। हालांकि, NWFETs में मजबूत सीमित ज्यामिति के कारण, स्वयं-हीटिंग प्रभाव एक प्रमुख चिंता का विषय है। इस थीसिस में, स्वयं-हीटिंग प्रभाव को लघु-संकेत आउटपुट चालन तकनीक का उपयोग करते हुए NWFETs में वर्णन किया गया है और इन NWFETs की योग्यता के लिये एनालॉग/आरएफ आंकड़ों की जांच की गई है। आधुनिक प्रोसेसर में बिजली के घनत्व को कम करने के लिए, एक तीव्र ढलान या निचले सबथ्रेशोल्ड स्विंग (SS) के साथ ट्रांजिस्टर को प्राथमिकता दी जाती है। फेरोइलेक्ट्रिक आधारित नकारात्मक धारिता FET (NC-FETs) कम SS (<60mV / दशक) के साथ उभरते उपकरण हैं। इस थीसिस में, NC-FinFET के RF प्रदर्शन क़ी BSIM-CMG कॉम्पैक्ट मॉडल का उपयोग करके जांच की गयी है जो 10nm प्रौद्योगिकी नोड बल्क FinFET डिवाइस के मापे गए डीसी और आरएफ डेटा से निष्कर्षित है। निम्न शक्ति और उच्च आवृत्ति अनुप्रयोगों के लिए प्रयोग करने योग्य स्केलेबल आरएफ मॉडल को NC-FinFET के विस्तृत मॉडल विवरण के साथ सूचित किया गया है।

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List of Abbreviations

Abbreviation	Description
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
MuGFET	**M**ultiple **G**ate **F**ield **E**ffect **T**ransistor
NWFET	**N**ano **W**ire **F**ield **E**ffect **T**ransistor
GAAFET	**G**ate **A**ll **A**round **F**ield **E**ffect **T**ransistor
NCFET	**N**egative **C**apacitance **F**ield **E**ffect **T**ransistor
TCAD	**T**echnology **C**omputer **A**ided **D**esign
SOI	**S**ilicon **O**n **I**nsulator
RF	**R**adio **F**requency
SOLT	**S**hort **O**pen **L**oad **T**hru
FOM	**F**igure **o**f **M**erit
SHE	**S**elf **H**eating **E**ffect
SPICE	**S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
BSIM	**B**erkeley **S**hort **C**hannel **I**GFET **M**odel
CMG	**C**ommon **M**ultiple **G**ate **D**evices

List of Symbols

Symbol	Description
L_g	Gate Length
V_t	Threshold Voltage
V_{ds}	Drain to Source Voltage
V_{gs}	Gate to Source Voltage
I_{ds}	Drain Current
g_m	Transconductance
g_{ds}	Output Conductance
I_{on}	On Drain Current
I_{off}	Off Drain Current
SS	Subthreshold Swing
A_v	Voltage Gain
A_i	Current Gain
f_T	Cut-off Frequency
f_{max}	Maximum Oscillation Frequency