MODELING AND SIMULATION OF NOVEL MULTI GATE NANOSCALE SOI MOSFETs AND POLYSILICON TFTs

by
Ali Asghar Orouji
Department of Electrical Engineering

Submitted
in fulfillment of the requirements of the degree of Doctor of Philosophy

to the

Indian Institute of Technology Delhi

March, 2006

CERTIFICATE

This is to certify that the thesis entitled **MODELING AND SIMULATION OF NOVEL MULTI GATE NANOSCALE SOI MOSFETs AND POLYSILICON TFTs** being submitted by **Ali Asghar Orouji** to the **Indian Institute of Technology, Delhi**, for the award of the degree of **Doctor of Philosophy** in **Electrical Engineering Department** is a bona fide work carried out by him under my supervision and guidance. The research reports and the results presented in this thesis have not been submitted in parts or in full to any other University or Institute for the award of any other degree or diploma.

Date: 10 July 2006
Place: IIT, Delhi

Dr. M. Jagadesh Kumar
Professor
Department of Electrical Engineering
Indian Institute of Technology
New Delhi - 110016

ACKNOWLEDGEMENTS

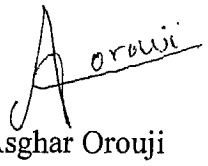
I would like to express my sincere gratitude to my supervisor, Prof. M. Jagadesh Kumar for his generous help through my Ph.D. study at I.I.T. Delhi. Prof. Kumar is an admirable academic professional. He taught me not only his precious knowledge, but his exceptional professionalism. He impressed me very much by his responsibility and strict attitude in training students. I am greatly indebted to him for his continuing encouragement and support without which, it would not have been possible for me to complete this undertaking successfully. Throughout my life I will benefit from the experience and knowledge I gained working with Professor Kumar.

Special thanks are due to Prof. B. Bhaumik, Prof. G. S. Visweswaran, Dr. Tuli for their valuable suggestions and questions during my semester plan presentation.

My special thanks to my friends Anurag, Reddy, Sukhendu and others, who always inspired me and particularly helped me in difficult times.

I wish to record my appreciation for my wife, Mrs. Sousan Zakikhani, for her patience and co-operation through out the research period.

My sincere thanks and acknowledgements are due to all my family members who have constantly encouraged me for completing this project.



Ali Asghar Orouji

ABSTRACT

Silicon-on-insulator (SOI) technology has been receiving a lot of attention owing to its advantages in reduced second-order effects for VLSI applications and has been the forerunner of the CMOS technology in the last decade offering superior CMOS devices with higher speed, higher density and excellent radiation hardness. Many novel device structures have been reported in literature to address the challenge of short-channel effects (SCE) and higher performance for deep submicron VLSI integration. However, most of the proposed structures do not offer simultaneous SCE suppression and improved circuit performance.

To simultaneously suppress SCE and improve device performance, the Electrically Shallow Junction (EJ) structure was proposed. By a careful control of the material work function and length of the side gate materials optimum performance can be attained in a EJ structure. In this thesis, a physics based analytical model of surface potential along the channel in a FD EJ-SOI MOSFET is developed by solving 2-D Poisson's equation. The model is used to investigate the excellent immunity against SCE offered by the EJ structure. Further the model is used to formulate an analytical expression of the threshold voltage, V_{th}. The results clearly demonstrate the scaling potential of EJ SOI devices with a desirable threshold voltage "roll-down" observed with decreasing channel lengths.

Double Gate (DG) MOSFETs using lightly doped ultra thin layers seem to be another very promising option for ultimate scaling of CMOS technology. Excellent short-channel effect immunity, high transconductance and ideal subthreshold factor have been reported by many theoretical and experimental studies on this device. But, the Dg MOSFETs suffer from SCEs yet. Therefore, a new concept and structure that we have called shielded channel DG MOSFET proposed and analyzed for first time. We demonstrate that the proposed device exhibits significantly reduced short channel effects such as drain induced barrier lowering and hot carrier effect. It is expected that the

shielded channel DG MOSFET could be of significant importance in CMOS applications requiring extreme scaling with improved reliability.

In recent years, polycrystalline silicon (poly-Si) thin film transistors (TFTs) have drawn much attention because of their widely application in active matrix liquid crystal displays (AMLCDs). One of the important problems of poly-Si TFTs is large OFF state leakage current. Several device structures have been reported in literature to circumvent the undesirable leakage current in poly-Si TFT devices. We have proposed a new approach and structure that is called Triple Gate TFT for reduction at leakage current of a poly-Si TFT. Numerical simulation studies demonstrate the diminishing of pseudo-subthreshold region and huge leakage current reduction in the proposed structure. Also, with same approach, for the first time we have demonstrated in this work that by applying a multiple-gate concept to the front gate of an asymmetrical double gate poly-Si-TFT, the OFF-state leakage current can be reduced significantly improving the performance of double gate poly-Si TFTs in AMLCD or other applications.

TABLE OF CONTENTS