CURRENT GAIN VARIABILITY AND PHYSICAL MODELING OF NORMAL AND I^2L BIPOLAR TRANSISTORS

by

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ABSTRACT

The yield and performance requirements of the present day integrated circuits demand a tight control of the parameters of individual components. In the case of planar epitaxial bipolar transistors, the current gain is very sensitive to process perturbations and is an important parameter from the viewpoint of process control. It is known from considerations of cost optimisation of integrated circuit fabrication that it is difficult to exercise a very fine control of all process steps. For a selective control, a precise understanding of the dependence of current gain on various process perturbations is required. The present thesis investigates the problem of current gain variability in normal and I^2L bipolar transistors.

The analysis pertains to planar epitaxial transistors of the double-diffused type. Calculations of current gain incorporate effects of heavy doping, mobility variations, built-in fields and surface recombination, with identification of different boundary conditions at the oxide-covered and metal-covered surface regions.

Considering that it is of foremost interest to determine the critical diffusion parameters and the effect of nonuniformities in epitaxial region parameters on current gain, a variability analysis of current gain has been carried out with respect to these parameters. The analysis yields useful results regarding the control of current gain. It is revealed that a change in gain, caused by perturbations in an intermediate process step, can be minimised by modifying the subsequent process schedule. This is a flexible approach to device fabrication.

An interesting feature which has emerged in this study is that a variability analysis can provide information about device design also. Some designs may inherently be more vulnerable to process perturbations. A procedure has been developed to optimise design parameters, e.g., emitter surface concentration and emitter-contact area in normal transistors. A new parameter called 'Risk Factor' has been defined for this purpose. A measure of the quality of device design and an estimate of the expected spread of gain on processed wafers is provided by defining a total variability function of gain.

The considerations of current gain variability have led to the design of a low-variability structure for I^2L with several advantages like high gain, low junction capacitances, reduced charge storage and linear-digital compatibility.

To conduct a variability study for a particular fabrication run, it is required to determine the structure of fabricated devices. New methods are developed in this work to determine the physical parameters of transistors because the existing techniques of physical modeling are not applicable to small area epitaxial transistors where stray and sidewall capacitances have to be identified. Moreover, the existing techniques use breakdown data for the determination of junction depth. It is shown here, by a two-dimensional numerical analysis, that the use of breakdown data for modeling planar epitaxial junctions is subject to error.

In this manner, the present thesis studies the process-dependent variability of current gain with an aim to utilise the information so obtained for better process control and for improving the design of bipolar integrated circuits.

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