EXPLORING REGISTER FILE AND MEMORY ORGANIZATION IN ASIP SYNTHESIS

by

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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Submitted

in fulfillment of the requirement of the degree of Doctor of Philosophy

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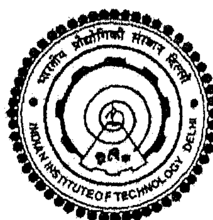

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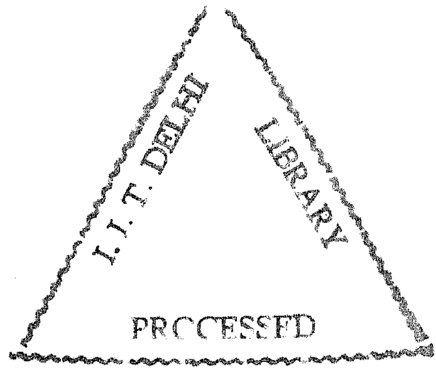

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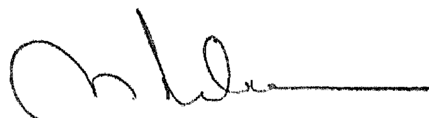
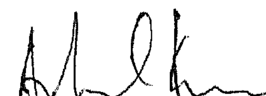
This is to certify that the project titled "**EXPLORING REGISTER FILE AND MEMORY ORGANIZATION IN ASIP SYNTHESIS**", being submitted by **Manoj Kumar Jain**, in partial fulfillment for the award of **Doctor of Philosophy**, is a record of the bonafide work carried out by him under our guidance and supervision at the Department of Computer Science and Engineering, **Indian Institute of Technology Delhi**. Also, the work presented in this project has not been submitted elsewhere, either in part or in full, for the award of any other degree or diploma.



Prof. M. Balakrishnan



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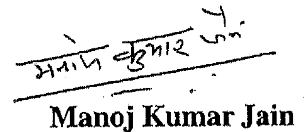

Manoj Kumar Jain

Abstract

An Application Specific Instruction Set Processor (ASIP) is a processor designed for one particular application or for a set of specific applications. An ASIP exploits special characteristics of the given application(s) to meet the desired performance, cost and power requirements. A typical ASIP design flow includes key steps such as application analysis, design space exploration, instruction set generation, code generation for software and hardware synthesis [1]. Performance estimation which drives the design space exploration is usually done by simulation. Such technique needs a retargetable compiler to generate code for different processor configurations to be explored and then simulating the generated code. This process is generally very slow. Further, there is a well known trade off between retargetability and code quality in terms of performance and code size when compared to the hand optimized code. This is because when the design space is large, all possible target specific optimizations can not be performed in that case. Therefore, in our opinion, compiler-simulator based approach is not suitable for an early design space exploration.

In the domain of Application Specific Instruction set Processors (ASIP), this problem can be solved by scheduler based approaches, which are much faster. However, existing scheduler based approaches do not help in exploring storage organization. We demonstrated the importance of including storage organization in design space exploration through a study using a retargetable code generator encc and a standard simulator. We studied the impact of register file size on performance, code size, power and energy consumption [2] for selected benchmarks on ARM7TDMI processor. Results indicated that choice of an appropriate number of registers has a significant impact on performance and energy in many cases.

The major contribution of this thesis is a scheduler based approach to explore register file size, number of register windows and cache memory configurations in an integrated manner. Proposed technique estimates the cycle count for application execution on chosen processor and memory configuration. We consider a parameterized model for processor as well as memory. Performance for different register file sizes are estimated by predicting the number of memory spills and its delay. The technique developed does not require explicit register assignment. We estimate register needs

on unscheduled code using the concept of reuse chains with significant extensions [3]. Cost due to register spills are considered while merging the reuse chains. Proposed technique also considers the global register needs.

For an architecture with register windows, the number of context switches leading to spills are estimated for evaluating the time penalty due to a limited number of register windows. A sequence of function calls and returns during the execution of the application is generated by instrumenting the input application. Number of window spills and restores required for a specific number of windows is computed by stack based analysis of generated trace of function calls and returns. We observe that usually the number of memory locations required to store spilled scalar variables and register windows is small compared to the total number of cache locations. Therefore, the spilling overhead is insensitive to the cache organization. This observation allows us to estimate the two independently. We use sim-cache simulator of simplescalar tool set to know cache misses statistics. Once we know the number of memory misses for a particular cache, based on the block size and delay information we compute the additional schedule overhead due to cache misses.

Performance estimates for a range of register file sizes, register windows and cache memory configurations are generated for selected benchmarks for different processors. The processors include ARM7TDMI, LEON [4] and Trimedia (TM-1000). Experiments showed that our estimates were within 9.6%, 9.7% and 3.3% for these processors respectively, compared to the actual performance results produced by standard tool sets. Further, this technique was nearly 77 times faster compared to simulator based approach.

We have shown utilization of our approach by a case study on LEON processor. We used the addresses of the registers which are decided to be 'spare' by our technique in addressing coprocessor registers. This simplified the coprocessor interface to the LEON processor and saved a number of loads and stores. Work presented here is integrated in an overall ASIP Synthesis Methodology named ASSIST being developed at IIT Delhi.

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