BROADBAND TRANSMIT/RECEIVE FRONT END FUNCTIONAL BLOCKS USING GAN TECHNOLOGY

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by

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CENTRE FOR APPLIED RESEARCH IN ELECTRONICS

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CERTIFICATE

This is to certify that the work reported in this thesis titled "**Broadband Transmit/Receive Front End Functional Blocks Using Gan Technology**" being submitted by **Mr. Ashish Jindal** for the award of the degree of **Doctor of Philosophy** to the Indian Institute of Technology Delhi, New Delhi, India, is a record of original Bonafide research work carried out by him under our guidance and supervision. The results contained in this thesis have not been submitted in part or full, to any other university or institute for the award of any degree or diploma.

We certify that he has pursued the prescribed course of research.

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ASHISH JINDAL

ABSTRACT

This thesis presents the design, development, and full monolithic integration of a
This thesis presents the design, development, and full monolithic integration of a
broadband, high-power, and compact Transmit/Receive (T/R) front-end module using Gallium Nitride (GaN) Monolithic Microwave Integrated Circuit (MMIC) technology. It is motivated by the growing demands of modern radar and electronic warfare (EW) platforms, which increasingly rely on wideband, high-efficiency, and space-constrained phased array architectures. This research addresses key challenges associated not only with the development of individual functional blocks but also with the integration of high-performance Low Noise Amplifiers (LNAs), Power Amplifiers (PAs), and RF single pole double throw (SPDT) switches onto a single MMIC chip.

The dissertation presents novel design methodologies and circuit-level innovations across three critical RF building blocks: LNAs, PAs, and Single Pole Double Throw (SPDT) switches. A key innovation is the introduction of a Rotation-Aligned Interstage Matching (RAIM) technique for wideband LNAs. This approach counters the impedance trajectory mismatch caused by Foster's reactance theorem and the inherent characteristics of HEMTs, enabling optimal conjugate matching between amplifier stages without intermediate 50-ohm terminations. As a result, substantial improvements in noise figure, gain flatness, and return loss are achieved across multi-octave frequency spans.

In the domain of power amplification, an improved Non-Uniform Distributed Power Amplifier (NDPA) topology is proposed and implemented. The design introduces a novel method for determining the characteristic impedance of the drain transmission line, ensuring it remains within a realizable range and can be directly matched to 50 ohms. This approach eliminates the need for bulky output transformers, significantly reducing chip area and insertion loss. To maintain consistent efficiency across all stages, the input drive levels are strategically adjusted, allowing each stage to operate optimally under its specific load conditions. The resulting amplifier achieves output power levels exceeding 10 W with high power-added efficiency, typically around 30%, across the 4–19 GHz frequency range.

For the switching function, a compact and broadband SPDT switch is developed based on an Active Loaded Transmission Line (ALTL) structure, combined with inductive tuning to achieve the desired frequency band and support high power handling. The resulting design demonstrates exceptional performance, with isolation exceeding 50 dB, insertion loss below 0.8 dB, and power handling capabilities above 43 dBm across the 4–20 GHz band. Furthermore, the switch is integrated with an on-chip driver that generates appropriate gate control voltages, thereby eliminating the need for external high-voltage control circuitry. To further enhance power handling, cascading of series devices is employed, enabling the switch to achieve a power handling capability of up to 44.5 dBm with insertion loss below 1 dB over the 1–18 GHz range.

These building blocks are monolithically integrated into a Single-Chip Front-End (SCFE) MMIC, combining the LNA, PA, and SPDT switch into a unified compact architecture. The SCFE achieves broadband operation from 4.5 to 18 GHz, with transmit output power exceeding 9 W, receive-mode noise figure below 3.5 dB, and Tx-Rx isolation surpassing 55 dB. Multiple SCFE prototypes are fabricated and evaluated to address coupling, layout optimization, and electromagnetic isolation challenges, progressively improving overall performance metrics.

The outcomes of this research represent a significant advancement in GaN-based MMIC design, offering practical solutions to the long-standing challenges of wideband impedance matching, high-power integration, and on-chip control compatibility. The presented architectures lay the foundation for the next generation of multifunctional, reconfigurable, and SWaP-optimized RF front ends, with direct applicability in phased-array radars, EW receivers, and high-speed communication platforms. This work contributes not only to the state-of-the-art in MMIC integration but also provides a scalable framework for future developments in frequency-agile and digitally controlled RF systems.

सारांश

यह शोध एक ब्रॉडबैंड, उच्च-शक्ति और कॉम्पैक्ट ट्रांसमिट/रिसीव (T/R) फ्रंट-एंड मॉड्यूल के डिजाइन, विकास और पूर्ण मोनोलिथिक एकीकरण को प्रस्तुत करता है, जिसे गैलियम नाइट्राइड (GaN) मोनोलिथिक माइक्रोवेव इंटीग्रेटेड सर्किट (MMIC) तकनीक का उपयोग करके विकसित किया गया है। इसका उद्देश्य आधुनिक रडार और इलेक्ट्रॉनिक युद्ध (EW) प्लेटफार्मों की बढ़ती आवश्यकताओं को पूरा करना है, जो आज के समय में वाइडबैंड, उच्च दक्षता और सीमित स्थान वाले फेज़्ड एरे आर्किटेक्चर पर आधारित होते हैं। यह शोध केवल व्यक्तिगत कार्यात्मक ब्लॉकों के विकास से संबंधित चुनौतियों को ही नहीं, बल्कि उच्च प्रदर्शन वाले लो नॉइज़ एम्प्लीफायर (LNA), पावर एम्प्लीफायर (PA) और RF सिंगल पोल डबल थ्रो (SPDT) स्विच को एक एकल MMIC चिप पर एकीकृत करने की जटिलताओं को भी संबोधित करता है।

शोध में तीन प्रमुख RF निर्माण खंडों—LNA, PA और SPDT स्विच—के लिए नवीन डिजाइन पद्धतियाँ और सर्किट-स्तरीय नवाचार प्रस्तुत किए गए हैं। एक मुख्य नवाचार है “रोटेशन-अलाइन इंटरस्टेज मैचिंग” (RAIM) तकनीक का प्रस्ताव, जो वाइडबैंड LNA के लिए उपयोग की गई है। यह तकनीक फोस्टर की रिएक्टेंस प्रमेय और HEMT की विशेषताओं के कारण उत्पन्न इम्पीडेंस ट्राजेक्टरी असंतुलन को संबोधित करती है, जिससे बिना मध्यवर्ती 50-ओम टर्मिनेशन के चरणों के बीच इष्टतम कंजुगेट मैचिंग संभव होती है। इसके परिणामस्वरूप नॉइज़ फिगर, गेन फ्लैटनस और रिटर्न लॉस में बहु-ऑक्टेव फ्रिक्वेंसी बैंड में उल्लेखनीय सुधार होता है।

पावर एम्प्लीफायर डोमेन में एक उन्नत “नॉन-यूनिफॉर्म डिस्ट्रीब्यूटेड पावर एम्प्लीफायर” (NDPA) टोपोलॉजी को प्रस्तावित और लागू किया गया है। इसमें ड्रेन ट्रांसमिशन लाइन की विशेष इम्पीडेंस को व्यावहारिक सीमा में बनाए रखने के लिए एक नई विधि प्रस्तुत की गई है, जिससे इसे सीधे 50 ओम से मैच किया जा सकता है और वॉल्यूमदार ट्रांसफॉर्मर की आवश्यकता समाप्त हो जाती है। सभी चरणों में दक्षता बनाए रखने के लिए इनपुट ड्राइव स्तरों को रणनीतिक रूप से समायोजित किया गया है, जिससे प्रत्येक चरण अपने लोड पर इष्टतम रूप से कार्य करता है। यह एम्प्लीफायर 4–19 GHz फ्रीक्वेंसी रेंज में 10 वॉट से अधिक आउटपुट पावर और लगभग 30% पावर-ऐडेड एफिशिएंसी प्राप्त करता है।

स्विचिंग फ़ंक्शन के लिए, एक कॉम्पैक्ट और ब्रॉडबैंड SPDT स्विच विकसित किया गया है, जो "एक्टिव लोडेड ट्रांसमिशन लाइन" (ALTL) संरचना पर आधारित है और इंडक्टिव ट्यूनिंग का उपयोग करता है। यह डिजाइन 4–20 GHz रेंज में 50 dB से अधिक आइसोलेशन, 0.8 dB से कम इंसर्शन लॉस और 43 dBm से अधिक पावर

हैंडलिंग प्रदर्शित करता है। इसमें ऑन-चिप ड्राइवर भी शामिल है जो उपयुक्त गेट कंट्रोल वोल्टेज उत्पन्न करता है, जिससे बाहरी हाई-वोल्टेज नियंत्रण सर्किट की आवश्यकता समाप्त हो जाती है। श्रृंखला में उपकरणों के कैस्केडिंग से पावर हैंडलिंग 44.5 dBm तक पहुंचती है, और 1–18 GHz बैंड में इंसर्शन लॉस 1 dB से कम रहता है।

ये सभी निर्माण खंड एक सिंगल-चिप फ्रंट-एंड (SCFE) MMIC में मोनोलिथिक रूप से एकीकृत किए गए हैं, जो LNA, PA और SPDT स्विच को एक एकीकृत और कॉम्पैक्ट संरचना में समाहित करता है। SCFE 4.5 से 18 GHz तक ब्रॉडबैंड संचालन प्रदान करता है, जिसमें ट्रांसमिट मोड में 9 वॉट से अधिक आउटपुट पावर, रिसीव मोड में 3.5 dB से कम नॉइज़ फिगर और Tx-Rx आइसोलेशन 55 dB से अधिक है। विभिन्न SCFE प्रोटोटाइप तैयार कर परीक्षण किए गए हैं, जिससे कपलिंग, लेआउट ऑप्टिमाइज़ेशन और विद्युतचुंबकीय आइसोलेशन की चुनौतियों को संबोधित किया गया है।

यह शोध GaN-आधारित MMIC डिज़ाइन में एक महत्वपूर्ण प्रगति को दर्शाता है, जो वाइडबैंड इम्पीडेंस मैचिंग, उच्च शक्ति एकीकरण और ऑन-चिप कंट्रोल संगतता की पुरानी चुनौतियों का व्यावहारिक समाधान प्रदान करता है। यह कार्य अगली पीढ़ी के मल्टीफंक्शनल, री-कॉन्फिगर करने योग्य और SWaP-अनुकूल RF फ्रंट-एंड्स के लिए एक आधार प्रदान करता है, जिनका उपयोग फेज्ड एरे रडार, EW रिसीवर और हाई-स्पीड संचार प्लेटफार्मों में किया जा सकता है।

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List of Abbreviations

ADC – Analog to Digital Converter

AESA – Active Electronically Scanned Array

ALTL – Active Loaded Transmission Line

CAD – Computer Aided Design

CPW – Coplanar Waveguide

CW – Continuous Wave

DA – Distributed Amplifier

DAC – Digital to Analog Converter

DC – Direct Current

EM – Electromagnetic

EMI – Electromagnetic Interference

EMC – Electromagnetic Compatibility

EW – Electronic Warfare

GaAs – Gallium Arsenide

GaN – Gallium Nitride

GHz – Giga Hertz

HEMT – High Electron Mobility Transistor

HPA - High Power Amplifier

IC – Integrated Circuit

IL – Insertion Loss

IMD – Intermodulation Distortion

IIP3 – Third-Order Input Intercept Point

LNA – Low Noise Amplifier

LTCC – Low-Temperature Co-fired Ceramic

MDS – Minimum Detectable Signal

MMIC – Monolithic Microwave Integrated Circuit

NDPA – Non-Uniform Distributed Power Amplifier

NF – Noise Figure

PA – Power Amplifier

PAE – Power Added Efficiency

PCB – Printed Circuit Board

$\mathbf{P}_{\mathbf{1}\,dB}$ – 1 dB Compression Point

RF – Radio Frequency

RFIN – RF Input

RFOUT – RF Output

RMS – Root Mean Square

Ropt – Optimum Load Resistance

SCFE – Single-Chip Front-End

SPDT – Single Pole Double Throw

T/R – Transmit/Receive

TRL – Thru-Reflect-Line

TX – Transmit

UWB – Ultra Wide Band

VNA – Vector Network Analyzer

VSWR – Voltage Standing Wave Ratio

Z0 – Characteristic Impedance