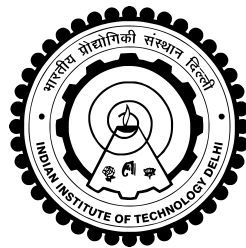


# **REAL TIME COMPRESSIVE SENSING IN CMOS IMAGE SENSORS**

**B. BHUVAN**



**Department of Electrical Engineering  
Indian Institute of Technology Delhi  
June, 2022**



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by

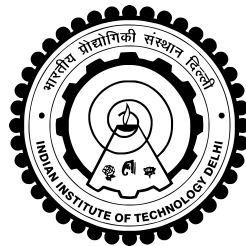
**B. BHUVAN**

Department of Electrical Engineering

Submitted in fulfillment of the requirements  
of the degree of

**Doctor of Philosophy**

to the



**Indian Institute of Technology Delhi**

**June, 2022**

To my parents ...

# Certificate

This is to certify that the thesis entitled “**Real time compressive sensing in CMOS image sensors**”, being submitted by **Mr. B. Bhuvan** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

**Dr. Mukul Sarkar**

Associate Professor,  
Department of Electrical Engineering,  
Indian Institute of Technology Delhi,  
Hauz Khas, New Delhi - 110016,  
INDIA.

**Dr. Shouri Chatterjee**

Professor,  
Department of Electrical Engineering,  
Indian Institute of Technology Delhi,  
Hauz Khas, New Delhi - 110016,  
INDIA.

# Acknowledgements

I would like to express my gratitude to my supervisors Prof. Mukul Sarkar and Prof. Shouri Chatterjee, for their guidance, support, and help throughout this research work. Their inputs on various occasions helped me in deciding the path to be followed both in this research work and in my academic career. Without their continuous infusion of positivity, this journey would not have reached where it is today.

I am thankful to my 'Student research committee,' Prof. G. S. Visweswaran, Prof. Sumantra Dutta Roy, and Prof. Samaresh Das, for all their constructive feedbacks throughout the research work. I am grateful to the Department of Electrical Engineering, IIT Delhi, for providing the required facilities to carry out the work. I also would like to thank the anonymous reviewers whose comments helped a lot in shaping this thesis.

I wish to express my thanks to Dr. Deepak Mishra, Dr. Amandeep Kaur, Ms. Indu Bharti, and Dr. Dawit for the support they provided to me during the worst phase of my Delhi life. I would like to thank Dr. Gajendranath Chowdary, Dr. Amandeep Kaur, and Dr. Roohie for their help during my first IC design. I would like to acknowledge the technical contributions of Rahul Kumar Singh, P. Anand, K. Devadershan, Aditya Singh Pal, Uzma Khan, Neha Priyadarshini, Dr. Chandani Anand. Siddhant Jain and Aakash Vishwakarma at different portions of this work. I would like to thank T. R. Aashish for his support in solving software access related issues. I thank Rohit, Atul, Supriyo, Nithin, Akhlesh, Sanjeev, and Akash for their help at various times.

I would like to thank all my colleagues at the Department of Electronics and Commu-

nication Engineering, National Institute of Technology Calicut (my parent institute), for supporting me to pursue my Ph.D. under Quality Improvement Programme (QIP) scheme. I also thank them for extending their full support even after the QIP leave period. I express my special thanks to Dr. Jaikumar M. G, Dr. Dhanaraj K. J, Dr. Rama Komaragiri, Dr. S. Kumaravel, Dr. A. V. Babu, and Dr. V. Sakthivel for their helping hands at crucial times.

I would like to thank my parents, my wife, and my son for their continuous support and understanding. I also thank my brother and my cousins, who ensured my absence was not felt on several occasions. Finally, I acknowledge all others who helped me directly or indirectly during this research work.

**B. Bhuvan**

# Abstract

CMOS image sensors are widely used in imaging applications ranging from simple photography to scientific measurements. The parallelism followed in image sensors generates an enormous amount of data that makes the storage/processing a challenging task. Image compression techniques ease this task by reducing the amount of data while increasing the power consumption of the processing blocks. However, image compression reduces the power consumption involved in signal transmission. Thus, the image compression introduces a trade-off between the power consumption of the processing and communication blocks of the imager. Hence, image compression schemes that lead to an overall reduction in power consumption are highly desirable.

Transform domain algorithms represent images with fewer coefficients in an alternate domain. However, the increasing spatial resolutions make the circuit-level realizations of these algorithms less energy efficient. The compressive sensing imagers help to reduce circuit-level complexity. However, the quality of the image highly depends on the reconstruction algorithms, which demands extensive training. Feature-based and information-centric compression algorithms exhibit higher energy efficiency compared to the information-theory based compressive sensing algorithms. Besides, the advances in the focal-plane processing support bio-inspired image compression schemes emerging as one of the energy-efficient solutions. However, many of these approaches provide specific information and fail to ensure the complete reconstruction of images in real-time.

The power consumption of an image sensor readout depends on the spatial resolution,

speed, and bit-depth of the sensors. Most of the works focus on reducing the spatial or temporal resolutions to reduce the power consumption, and the compression on the depth of the pixel is considered rarely. In this work, the photon shot noise characteristic of an image sensor is used to achieve bit-depth compression. The photon shot noise-inspired image sensors use increased quantization step sizes at high light conditions to accelerate the data conversion in slope ADCs. Here, an accelerated ramp with uniform counting is proposed to achieve bit-depth compression.

Slope ADCs using accelerated ramps result in slope-dependent nonlinearities in their transfer characteristics. A decelerated-ramp slope ADC ensures unique digital outputs for each analog quantization range, thus ensures nonlinearity reduction. A decelerated-ramp slope ADC designed in a  $0.18 \mu\text{m}$  CMOS process has no missing-decision-levels even with bandwidth-limited comparators. The nonlinearities due to slope-dependent latencies are reduced to less than 0.5 LSB. With reduced nonlinearity, a second-level compression can be applied to the bit-depth compressed outputs.

A two-level image compression using our bit-depth compression followed by Discrete Cosine Transform is proposed. The two-level compression achieves a PSNR of 48.9 dB and an SSIM of 0.99 for a quality factor  $Q=16$ . The resultant PSNR and SSIM are 5.5 dB and 0.0126 higher than the transform domain compression without bit-depth compression for the same quality factor and equal data rate.

Depth-sensing imagers are one of the suitable applications where our bit-depth compression can be used. In depth-sensing imagers, as the object moves closer to the sensor,

the signal and the photon shot noise increase. Hence, the quantization step of the ramp can be increased during the data conversion of the object closer to the sensor. The bit-depth compression supports a higher resolution ADC with fewer bits for its digital representation. The advantages of the proposed bit-depth compression in a depth-sensing application are studied using the measurement results of a time-of-flight sensor fabricated in 0.35  $\mu\text{m}$  AMS OPTO process. In the analysis, a 10-bit (bit-depth compressed) digital representation is assumed for an 11-bit (linear) pixel output. The increased ADC resolution predicts a reduced error in the distance measurement compared to a linear 10-bit readout.

## सार

साधारण फोटोग्राफी से लेकर वैज्ञानिक मापन तक के इमेजिंग अनुप्रयोगों में सीएमओएस इमेज सेंसर का व्यापक रूप से उपयोग किया जाता है। छवि संवेदकों में अनुसरण की जाने वाली समानता बहुत अधिक मात्रा में डेटा उत्पन्न करती है जो भंडारण/प्रसंस्करण को एक चुनौतीपूर्ण कार्य बनाती है। प्रसंस्करण ब्लॉकों की बिजली खपत में वृद्धि करते हुए छवि संपीड़न तकनीक डेटा की मात्रा को कम करके इस कार्य को आसान बनाती है। हालांकि, छवि संपीड़न सिग्नल ट्रांसमिशन में शामिल बिजली की खपत को कम करता है। इस प्रकार, छवि संपीड़न इमेजर के प्रसंस्करण और संचार ब्लॉकों की बिजली खपत के बीच एक व्यापार-बंद का परिचय देता है। इसलिए, छवि संपीड़न योजनाएं जो बिजली की खपत में समग्र रूप से कमी लाती हैं, अत्यधिक वांछनीय हैं।

ट्रांसफॉर्म डोमेन एल्गोरिदम वैकल्पिक डोमेन में कम गुणांक वाली छवियों का प्रतिनिधित्व करते हैं। हालांकि, बढ़ते स्थानिक संकल्प इन एल्गोरिदम के सर्किट-स्तरीय अहसास को कम ऊर्जा कुशल बनाते हैं। कंप्रेसिव सेंसिंग इमेजर सर्किट-स्तरीय जटिलता को कम करने में मदद करते हैं। हालांकि, छवि की गुणवत्ता अत्यधिक पुनर्निर्माण एल्गोरिदम पर निर्भर करती है, जिसके लिए व्यापक प्रशिक्षण की आवश्यकता होती है। फ्रीचर-आधारित और सूचना-केंद्रित संपीड़न एल्गोरिदम, सूचना-सिद्धांत आधारित कंप्रेसिव सेंसिंग एल्गोरिदम की तुलना में उच्च ऊर्जा दक्षता प्रदर्शित करते हैं। इसके अलावा, फोकल-प्लेन प्रोसेसिंग में प्रगति ऊर्जा-कुशल समाधानों में से एक के रूप में उभरने वाली जैव-प्रेरित छवि संपीड़न योजनाओं का समर्थन करती है। हालांकि, इनमें से कई दृष्टिकोण विशिष्ट जानकारी प्रदान करते हैं और रवास्तविक समय में छवियों के पूर्ण पुनर्निर्माण को सुनिश्चित करने में विफल होते हैं।

इमेज सेंसर रीडआउट की बिजली की खपतसेंसर के स्थानिक रिज़ॉल्यूशन, गति और रबिट-डेथ पर निर्भर करती है। अधिकांश कार्य बिजली की खपतको कम करने के लिए स्थानिक या लौकिक संकल्पों को कम करने पर ध्यान केंद्रित करते हैं, और रपिक्सेल की गहराई पर संपीड़न को शायद ही कभी माना जाता है। इस काम में, बिट-डेथ कम्प्रेसन को प्राप्त करने के लिए एक इमेज सेंसर की फोटॉन शॉट नॉइज़ विशेषता का उपयोग किया जाता है। फोटॉन शॉट शोर-प्रेरित छवि सेंसर ढलान एडीसी में डेटा रूपांतरण में तेजी लाने के लिए उच्च प्रकाश स्थितियों में बढ़े हुए परिमाणीकरण चरणआकार

का उपयोग करते हैं। यहां, बिट-डेप्थ कम्प्रेसन को प्राप्त करने के लिए एकसमान गिनती के साथ एक त्वरित रैंप प्रस्तावित है।

त्वरित रैंप का उपयोग करने वाले ढलान एडीसी के परिणामस्वरूप उनकी स्थानांतरण विशेषताओं में ढलान-निर्भर गैर-रैखिकताएं होती हैं। एक डिक्लेरेटेड-रैंप स्लोप एडीसी प्रत्येक एनालॉग क्वांटिज़ेशन रेंज के लिए अद्वितीय डिजिटल आउटपुट सुनिश्चित करता है, इस प्रकार गैर-रेखीयता में कमी सुनिश्चित करता है। 0.18 माइक्रो मीटर सीएमओएस प्रक्रिया में डिज़ाइन किए गए एक धीमी-रैंप ढलान एडीसी में बैंडविड्थ-सीमित तुलनित्रों के साथ भी कोई लापता-निर्णय-स्तर नहीं है। ढलान पर निर्भर विलंबता के कारण गैर-रैखिकता 0.5 एलएसबी से कम हो जाती है। कम गैर-रैखिकता के साथ, दूसरे स्तर के संपीड़न को बिट-गहराई वाले संपीड़ित आउटपुट पर लागू किया जा सकता है।

हमारे बिट-डेप्थ कम्प्रेसन का उपयोग करते हुए दो-स्तरीय छवि संपीड़न और उसके बाद डिस्क्रीट कोसाइन ट्रांसफॉर्म प्रस्तावित है। गुणवत्ता कारक  $Q=16$  के लिए दो-स्तरीय संपीड़न 48.9 dB का एक पीसेनर और 0.99 का एक येसेयियम प्राप्त करता है। परिणामी पेयेसेनर और रयस्यसैयम समान गुणवत्ता कारक और रसमान डेटा दर के लिए बिट-डेप्थ कम्प्रेसन के बिना ट्रांसफॉर्म डोमेन कंप्रेसन से 5.5 डीबी और 0.0126 अधिक है।

डेप्थ-सेंसिंग इमेजर उन उपयुक्त अनुप्रयोगों में से एक हैं जहां हमारे बिट-डेप्थ कम्प्रेसन का उपयोग किया जा सकता है। डेप्थ-सेंसिंग इमेजर्स में, जैसे-जैसे ऑब्जेक्ट सेंसर के करीब जाता है, सिग्नल और रफोटॉन शॉट नॉइज़ में वृद्धि होती है। इसलिए, सेंसर के करीब वस्तु के डेटा रूपांतरण के दौरान रैंप का परिमाणीकरण चरण बढ़ाया जा सकता है। बिट-डेप्थ कम्प्रेसन अपने डिजिटल प्रतिनिधित्व के लिए कम बिट्स के साथ उच्च रिज़ॉल्यूशन एडीसी का समर्थन करता है। डेप्थ-सेंसिंग एप्लिकेशन में प्रस्तावित बिट-डेप्थ कम्प्रेसन के लाभों का अध्ययन 0.35 माइक्रोमीटर एम्स-एण्डो प्रक्रिया में निर्मित टाइम-ऑफ़-फ्लाइट सेंसर के माप परिणामों का उपयोग करके किया जाता है। विश्लेषण में, 11-बिट (रैखिक) पिक्सेल आउटपुट के लिए 10-बिट (बिट-डेप्थ कंप्रेस्ड) डिजिटल प्रतिनिधित्व माना जाता है। बढ़ा हुआ एडीसी रिज़ॉल्यूशन रैखिक 10-बिट रीडआउट की तुलना में दूरी माप में कम मत्रुटि की भविष्यवाणी करता है।

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