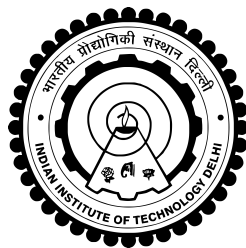


# **PRECISION REFERENCES FOR ANALOG AND MIXED SIGNAL APPLICATIONS**

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**DEPARTMENT OF ELECTRICAL ENGINEERING  
INDIAN INSTITUTE OF TECHNOLOGY DELHI  
JANUARY, 2025**

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by

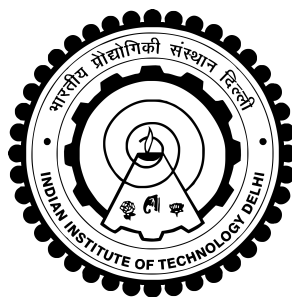
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Submitted

**in fulfillment of the requirements of the degree of Doctor of Philosophy**

to the



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**JANUARY, 2025**

To my loving son *Vivaswaan*

## Certificate

This is to certify that the thesis titled **Precision References for Analog and Mixed Signal Applications**, submitted by **Sweta Agarwal (2015EEZ8110)**, to the Indian Institute of Technology, Delhi, for the award of the degree of **Doctor of Philosophy**, is a bonafide record of the research work done by her under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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# Abstract

Precision circuits for analog and mixed-signal applications are at the forefront of today's modern technologies, driven by the increasing demands for enhanced accuracy, reduced form factor, and cost-efficient solutions. The design of on-chip voltage, current, and frequency references has become pivotal in System of Chip (SoC), addressing challenges related to Process, Voltage, Temperature (PVT) variations, and external environmental factors. Commercially, chips are plastic packaged for protection and versatility in various applications. However, these plastic packages are susceptible to environmental conditions, resulting in mechanical stress on the silicon die (chip) due to a mismatch in the thermal and hygroscopic properties of package components and the chip. Although the chip is not directly exposed to the environment, it experiences the effects of external conditions through the package. Achieving stability in precision references, measured in parts per million (ppm) over varying operational conditions, remains paramount. Bridging the gap between simulation and on-chip measurements ensures robustness and reliability, making precision references indispensable for various applications.

This thesis comprehensively investigates CMOS-integrated frequency and voltage references, presenting several significant findings and discoveries. The work addresses the challenges in designing PVT and package stress-tolerant precision references. It involves architecture, circuit design, and layout choices, prioritizing the precision reference's robustness while minimizing error sources contributing to the temperature coefficient (TC).

The frequency output in an RC-based frequency reference mainly depends on the PVT and package-induced sensitivity of the CMOS process resistor and capacitor. However, the first-order TC of resistors is approximately 1000 ppm/°C in any CMOS technology node. This means that temperature compensation is needed for use in frequency references. The TC of MIM capacitors in matured technology nodes is less than 30 ppm/°C. In contrast, only MOM capacitors are available in lower technology nodes, and they have a TC of 70 ppm/°C, necessitating TC compensation. The precision references must withstand a military temperature range of -40°C to 125°C.

The second chapter of the thesis focuses on designing a near Zero Temperature Coefficient (ZTC) resistor that is PVT tolerant. The ZTC resistor, fabricated in TSMC 180 nm technology, exhibits a best-case temperature spread of 2.93 ppm/°C across a wide range of -40°C to 125°C in simulations. This versatile component is suitable for lower technology nodes where complementary resistors are unavailable.

The third chapter investigates the impact of thermo-mechanical package stress on HRI-poly



resistors and MIM capacitors with a dedicated test chip with nine identical MIM capacitors and HRI-poly resistors placed at nine locations. Our findings showed that the effective mismatch between the identical resistor and capacitor pairs changes with temperature and location. We developed a mathematical model to estimate the impact of stress in terms of stress coefficients, effectively de-embedding the mismatch, thermal dependence of material properties, and layout routing parasitics. In conclusion, we provide analog engineers with layout guidelines for placing HRI-poly resistors and MIM capacitors for a temperature-independent mismatch.

We have fabricated a frequency reference circuit in CMOS 28 nm technology that addresses the shortcomings of the gyrator-based ZTC resistor. The architecture is physics based and does not require post-silicon trimming for ppm accuracy. The proposed architecture cancels the first order resistor and capacitor TC with physics based parameters. The proposed frequency reference uses a low TC MOS capacitor of 8 ppm/°C. Our proposed frequency reference operates at 3.75 MHz with an energy efficiency of 122.64 pJ/cycle on a 1.8 V supply. Moreover, the temperature sensitivity of the proposed frequency reference is 26 ppm/°C ( $\mu + 3\sigma$ ) over a temperature range of -40°C to 125°C without any trim.

The shortcomings of the frequency reference presented in Chapter 4 were addressed in Chapter 5. It presents a 1V chopper-less physics-based 200 MHz RC frequency reference with a Phase-Locked-Loop (PLL) single-point trim. The frequency reference is based on the physics based model proposed in Chapter 4 achieving an accuracy of 17.5 ppm/°C over a temperature range of -40 to 120°C. PLL one-point (1T) trim adjusts the center frequency, while accuracy over temperature does not require any trim. A 120-hour burn-in aging test changes the frequency accuracy by 1.14 ppm/°C across temperatures. The prototype designed in TSMC 65nm draws 400  $\mu$ A from a 1 V supply with an Allan deviation of 80.5 ppm and line regulation of 1.27%/V. The chip could not be measured because the modeled MOS leakage current was higher than the fabricated one.

The issues posed by the proposed frequency reference resulted in the design of a sub-1V bandgap in TSMC 28 nm CMOS technology, generating 538 mV operating with a 0.85 V power supply. A novel curvature compensation scheme is proposed and validated across PVT simulations, achieving 12 ppm/°C with a single-point trim. The proposed bandgap consumes a power of 15  $\mu$ W in TSMC 28 nm.

In addition, we performed SPICE modeling of RF inductors and MIM capacitors fabricated in SCL 180 nm CMOS technology, acknowledging the effects of fringing, parasitic, and substrate effects on MIM capacitors and spiral inductors. Model development and validation are performed using Keysight-IC-CAP software, with simulated and measured data showing  $\pm 1.25\%$  agreement.

The findings presented in this thesis significantly contribute to the advancement of CMOS-integrated frequency and voltage references, offering innovative solutions and deep insights into the design and performance of precision components for various applications in modern integrated circuits.

## सार

एनालॉग और मिश्रित-सिग्नल अनुप्रयोगों के लिए सटीक सर्किट आज की आधुनिक तकनीकों में सबसे आगे हैं। यह बेहतर सटीकता, छोटे आकार, और लागत-कुशल समाधानों की बढ़ती मांगों से प्रेरित हैं। ऑन-चिप वोल्टेज, करंट, और फ्रिक्वेंसी संदर्भों की डिज़ाइन System on Chip (SoC) में महत्वपूर्ण हो गई है, जो प्रक्रिया, वोल्टेज, तापमान (PVT) विविधताओं और बाहरी पर्यावरणीय कारकों से संबंधित चुनौतियों को संबोधित करती है। वाणिज्यिक रूप से, चिप्स को सुरक्षा और विभिन्न अनुप्रयोगों में बहुमुखी उपयोगिता के लिए प्लास्टिक में पैकेज किया जाता है। हालाँकि, ये प्लास्टिक पैकेज पर्यावरणीय परिस्थितियों के प्रति संवेदनशील होते हैं, जिससे पैकेज घटकों और चिप के थर्मल और हाइग्रोस्कोपिक गुणों में असमानता के कारण सिलिकॉन डाई (चिप) पर यांत्रिक तनाव उत्पन्न होता है। हालाँकि चिप सीधे पर्यावरण के संपर्क में नहीं होता है, यह पैकेज के माध्यम से बाहरी परिस्थितियों के प्रभाव को महसूस करता है। विभिन्न परिचालन परिस्थितियों में भाग प्रति मिलियन (ppm) में मापी गई स्थिरता प्राप्त करना सर्वोपरि है। सिमुलेशन और ऑन-चिप मापों के बीच अंतर को पाटना मजबूती और विश्वसनीयता सुनिश्चित करता है, जिससे सटीक संदर्भ विभिन्न अनुप्रयोगों के लिए अपरिहार्य हो जाते हैं।

यह शोध प्रबंध CMOS-एकीकृत फ्रिक्वेंसी और वोल्टेज संदर्भों की व्यापक रूप से जांच करता है, जिसमें कई महत्वपूर्ण निष्कर्ष और खोज प्रस्तुत किए गए हैं। यह कार्य PVT और पैकेज तनाव-सहिष्णु सटीक संदर्भ डिज़ाइन की चुनौतियों को संबोधित करता है। इसमें आर्किटेक्चर, सर्किट डिज़ाइन, और लेआउट विकल्प शामिल हैं, जो सटीक संदर्भ की मजबूती को प्राथमिकता देते हैं और तापमान गुणांक (TC) में योगदान देने वाले त्रुटि स्रोतों को कम करते हैं। RC-आधारित फ्रिक्वेंसी संदर्भ में फ्रिक्वेंसी आउटपुट मुख्य रूप से CMOS प्रक्रिया resistor और capacitor की PVT और पैकेज-प्रेरित संवेदनशीलता पर निर्भर करता है। हालाँकि, किसी भी CMOS तकनीकी नोड में resistors का प्रथम-आदेश TC लगभग  $1000 \text{ ppm}/^{\circ}\text{C}$  है। इसका मतलब है कि फ्रिक्वेंसी संदर्भों में उपयोग के लिए तापमान मुआवजे की आवश्यकता है। परिपक्व तकनीकी नोड्स में MIM capacitors का TC  $30 \text{ ppm}/^{\circ}\text{C}$  से कम होता है। इसके विपरीत, निचले तकनीकी नोड्स में केवल MOM capacitors उपलब्ध होते हैं, जिनका TC  $70 \text{ ppm}/^{\circ}\text{C}$  होता है, जिससे TC मुआवजा आवश्यक हो जाता है। सटीक संदर्भों को  $-40^{\circ}\text{C}$  से  $125^{\circ}\text{C}$  की सैन्य तापमान सीमा का सामना करना चाहिए।

शोध प्रबंध के दूसरे अध्याय में Zero Temperature Coefficient (ZTC) resistor की डिज़ाइन पर ध्यान केंद्रित किया गया है, जो PVT-सहिष्णु है। TSMC 180 nm तकनीक में निर्मित ZTC resistor ने  $-40^{\circ}\text{C}$  से  $125^{\circ}\text{C}$  की विस्तृत सीमा में  $2.93 \text{ ppm}/^{\circ}\text{C}$  के सर्वोत्तम-स्थिति तापमान प्रसार का प्रदर्शन किया है। यह बहुमुखी घटक उन निचले तकनीकी नोड्स के लिए उपयुक्त है जहाँ पूरक resistors अनुपलब्ध हैं।

शोध प्रबंध के तीसरे अध्याय में HRI-poly resistors और MIM capacitors पर थर्मो-मैकेनिकल पैकेज तनाव के प्रभाव की जांच की गई है। इसके लिए नौ समान MIM capacitors और HRI-poly resistors वाले एक समर्पित परीक्षण चिप का उपयोग किया गया, जिन्हें नौ विभिन्न स्थानों पर रखा गया था। हमारे निष्कर्ष बताते हैं कि समान resistor और capacitor जोड़ों के बीच प्रभावी असमानता तापमान और स्थान के अनुसार बदलती है। हमने तनाव गुणांक की शर्तों में तनाव के प्रभाव का अनुमान लगाने के लिए एक गणितीय मॉडल विकसित किया, जिसने असमानता, सामग्री गुणों की थर्मल निर्भरता, और लेआउट रूटिंग पैरासिटिक्स को प्रभावी रूप से अलग किया।

निष्कर्ष के रूप में, हमने HRI-poly resistors और MIM capacitors को तापमान-स्वतंत्र असमानता सुनिश्चित करने के लिए रखने के लिए एनालॉग इंजीनियरों को लेआउट दिशानिर्देश प्रदान किए।

हमने CMOS 28 nm तकनीक में एक फ्रिक्वेंसी संदर्भ सर्किट का निर्माण किया, जो gyrator-आधारित ZTC resistor की कमियों को संबोधित करता है। यह आर्किटेक्चर भौतिकी-आधारित है और ppm सटीकता के लिए पोस्ट-सिलिकॉन ट्रिमिंग की आवश्यकता नहीं है। प्रस्तावित आर्किटेक्चर physics-based parameters का उपयोग करके resistor और capacitor के प्रथम-आदेश TC को रद्द करता है। प्रस्तावित फ्रिक्वेंसी संदर्भ 8 ppm/°C के कम TC वाले MOS capacitor का उपयोग करता है। हमारा प्रस्तावित फ्रिक्वेंसी संदर्भ 3.75 MHz पर संचालित होता है और 1.8 V आपूर्ति पर 122.64 pJ/चक्र की ऊर्जा दक्षता प्रदान करता है। इसके अलावा, -40°C से 125°C के तापमान रेंज में प्रस्तावित फ्रिक्वेंसी संदर्भ की तापमान संवेदनशीलता 26 ppm/°C ( $\mu + 3\sigma$ ) है, बिना किसी ट्रिम के।

चौथे अध्याय में प्रस्तुत फ्रिक्वेंसी संदर्भ की कमियों को पाँचवें अध्याय में संबोधित किया गया। यह एक 1V चॉपर-रहित भौतिकी-आधारित 200 MHz RC फ्रिक्वेंसी संदर्भ को एक Phase-Locked-Loop (PLL) एकल-बिंदु ट्रिम के साथ प्रस्तुत करता है। यह फ्रिक्वेंसी संदर्भ चौथे अध्याय में प्रस्तावित physics-based मॉडल पर आधारित है, जो -40°C से 120°C के तापमान रेंज में 17.5 ppm/°C की सटीकता प्राप्त करता है। PLL एक-बिंदु (1T) ट्रिम केंद्र फ्रिक्वेंसी को समायोजित करता है, जबकि तापमान पर सटीकता के लिए किसी ट्रिम की आवश्यकता नहीं होती है। 120-घंटे के aging टेस्ट में तापमान के साथ फ्रिक्वेंसी सटीकता में 1.14 ppm/°C का परिवर्तन हुआ। TSMC 65nm में डिज़ाइन किया गया प्रोटोटाइप 1 V आपूर्ति से 400  $\mu$ A खींचता है, जिसमें 80.5 ppm का एलन विचलन और 1.27%/V की लाइन विनियमन होती है।

इस प्रस्तावित फ्रिक्वेंसी संदर्भ के कारण उत्पन्न मुद्दों ने TSMC 28 nm CMOS तकनीक में एक sub-1V बैंडगैप डिज़ाइन का विकास किया, जो 0.85 V पावर आपूर्ति पर 538 mV उत्पन्न करता है। एक नई वक्रता मुआवजा योजना प्रस्तावित की गई और PVT सिमुलेशन में मान्य की गई, जो एक-बिंदु ट्रिम के साथ 12 ppm/°C प्राप्त करती है। प्रस्तावित बैंडगैप TSMC 28 nm में 15  $\mu$ W की शक्ति का उपभोग करता है।

इसके अतिरिक्त, हमने SCL 180 nm CMOS तकनीक में निर्मित RF inductors और MIM capacitors के SPICE मॉडलिंग का प्रदर्शन किया। MIM capacitors और स्पायरल inductors पर fringings, parasitics, और substrate प्रभावों को स्वीकार करते हुए मॉडल का विकास और सत्यापन Keysight-IC-CAP सॉफ्टवेयर का उपयोग करके किया गया, जिसमें सिमुलेटेड और मापा डेटा  $\pm 1.25\%$  की सहमति दिखाता है।

इस शोध प्रबंध में प्रस्तुत निष्कर्ष CMOS-एकीकृत फ्रिक्वेंसी और वोल्टेज संदर्भों की उन्नति में महत्वपूर्ण योगदान करते हैं। यह आधुनिक एकीकृत सर्किटों में विभिन्न अनुप्रयोगों के लिए सटीक घटकों की डिज़ाइन और प्रदर्शन पर नवोन्मेषी समाधान और गहन अंतर्दृष्टि प्रदान करता है।

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# Abbreviations

|              |                                                     |
|--------------|-----------------------------------------------------|
| <b>TC</b>    | Temperature Coefficient                             |
| <b>ZTC</b>   | Zero Temperature Coefficient                        |
| <b>NIC</b>   | Negative Impedance Converter                        |
| <b>SRS</b>   | Sequential Rotation Scheme                          |
| <b>CTE</b>   | Coefficient of Thermal Expansion                    |
| <b>MIM</b>   | Metal-Insulator-Metal                               |
| <b>MOM</b>   | Metal-Oxide-Metal                                   |
| <b>PTC</b>   | Positive Temperature Coefficient                    |
| <b>NTC</b>   | Negative Temperature Coefficient                    |
| <b>RF</b>    | Radio Frequency                                     |
| <b>QFN</b>   | Quad-Flat-No-Leads                                  |
| <b>CTAT</b>  | Complementary To Absolute Temperature               |
| <b>PTAT</b>  | Proportional To Absolute Temperature                |
| <b>PVT</b>   | Process-Voltage-Temperature                         |
| <b>CMOS</b>  | Complimentary Metal Oxide Semiconductor             |
| <b>BJT</b>   | Bipolar Junction Transistor                         |
| <b>SRF</b>   | Series Resonance Frequency                          |
| <b>SPICE</b> | Simulation Program with Integrated Circuit Emphasis |
| <b>DUT</b>   | Device Under Test                                   |
| <b>PCB</b>   | Printed Circuit Board                               |
| <b>PDK</b>   | Process Design Kit                                  |
| <b>PLL</b>   | Phase Locked Loop                                   |
| <b>FLL</b>   | Freequency Locked Loop                              |
| <b>Q</b>     | Quality Factor                                      |
| <b>LPF</b>   | Low Pass Filter                                     |
| <b>OSC</b>   | Oscillator                                          |
| <b>NIC</b>   | Negative Impedance Converter                        |
| <b>LDE</b>   | Layout Dependent Effects                            |
| <b>SPI</b>   | Serial Parallel Interface                           |
| <b>WSN</b>   | Wireless Sensor Network                             |
| <b>MCU</b>   | Microcontroller Unit                                |
| <b>VCO</b>   | Voltage Controlled Oscillator                       |
| <b>PSR</b>   | Power Supply Rejection Ratio                        |
| <b>LDO</b>   | Low Drop Out                                        |
| <b>VNA</b>   | Vector Network Analyzer                             |
| <b>PMU</b>   | Power Management Unit                               |
| <b>SoC</b>   | System-on-Chip                                      |
| <b>ENOB</b>  | Effective Number Of Bits                            |

|             |                                            |
|-------------|--------------------------------------------|
| <b>BoM</b>  | Bill of Materials                          |
| <b>ADC</b>  | Anaolog to Digital Coverter                |
| <b>MEMS</b> | Micro-Electro Mechanical Systems           |
| <b>BAW</b>  | Bulk Acoustic Wave                         |
| <b>TCXO</b> | Temperature Compensated Crystal Oscillator |