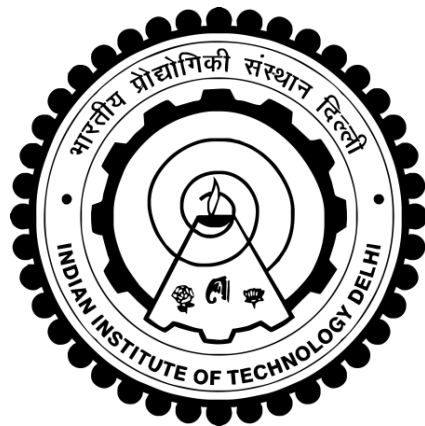


# **DESIGN AND DEVELOPMENT OF SWITCHED RELUCTANCE MOTOR DRIVE FOR LOW POWER APPLICATIONS**

**VIPIN KUMAR SINGH**



**DEPARTMENT OF ELECTRICAL ENGINEERING  
INDIAN INSTITUTE OF TECHNOLOGY DELHI  
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JANUARY 2026**

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by

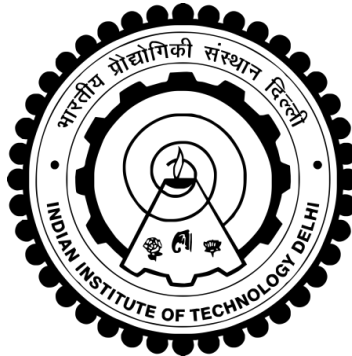
**VIPIN KUMAR SINGH**  
**Department of Electrical Engineering**

*Submitted*

*in fulfillment of the requirements of the degree of*

**DOCTOR OF PHILOSOPHY**

to the



**DEPARTMENT OF ELECTRICAL ENGINEERING**  
**INDIAN INSTITUTE OF TECHNOLOGY DELHI**  
**HAUZ KHAS, NEW DELHI – 110016, INDIA**  
**JANUARY 2026**



*Dedicated to My Family  
and My Mentor*



## **CERTIFICATE**

This is to certify that the thesis entitled, “**Design and Development of Switched Reluctance Motor Drive for Low Power Applications**” being submitted by **Mr. Vipin Kumar Singh** for the award of the degree of Doctor of Philosophy is a record of bonafide research work carried out by him in the Department of Electrical Engineering of Indian Institute of Technology Delhi.

**Mr. Vipin Kumar Singh** has worked under my guidance and supervision and has fulfilled the requirements for the submission of this thesis, which to my knowledge has reached the requisite standard. The results obtained here in have not been submitted to any other University or Institute for the award of any degree.

**Date: 30<sup>th</sup> January 2026**

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Dated: 30<sup>th</sup> January 2026

Vipin Kumar Singh

## ABSTRACT

This thesis presents an in-depth examination of design, control and implementation of energy-efficient switched reluctance motor (SRM) drives tailored for low-power applications, emphasizing enhancements in power quality, cost reduction, and facilitation of sensor-less control. This research work explores significant issues related to traditional motor drive systems, focusing on their efficiency, number of components, and their ability to adapt to varying grid conditions. The research commences by elaborating on design and development of a resilient, energy-efficient SRM tailored for low-power industrial exhaust fan applications. A methodology grounded in benchmarks, bolstered by analytical calculations and validated through 2D Finite Element Method (FEM) in Ansys Maxwell, is employed to delineate an optimized motor geometry. The design is experimentally validated through fabrication of a physical prototype, demonstrating its practical feasibility in low-power SRM drive applications. Additionally, exploration of power factor correction (PFC) converter topologies aims to improve input power quality and comply with harmonic standards, specifically IEC 61000-3-2, in context of SRM drive.

In order to enhance overall efficiency of the system while simultaneously minimizing expenses, bridgeless PFC converters are utilized in both single-output and dual-output arrangements for asymmetric bridge converter (ABC) and mid-point converter (MPC) powered SRM drives, respectively. Topologies including hybrid Cuk, hybrid SEPIC, integrated Zeta-Luo, and Zeta-Canonical Switching Cell (CSC) converters, are thoroughly developed to meet specific demands of SRM drives across a spectrum of load and supply conditions. These converters function in discontinuous conduction mode (DCM), thereby inherently attaining power factor correction while decreasing the necessity for numerous sensors and complex passive components. Furthermore, SRM drive system integrates a sensor less control strategy with a PFC front-end to improve energy efficiency, power quality, and reduce overall component count. By eliminating Hall-effect sensors and minimizing electrical sensing through simplified estimation algorithms using electrical feedback, system significantly lowers cost and design complexity. This approach delivers high performance while ensuring a scalable and low-cost solution, making it well-suited for low-power, cost-sensitive applications and contributing to advancement of efficient and sustainable motor drives in power electronics.



## सार

यह शोध प्रबंध कम विद्युत खपत वाले अनुप्रयोगों के लिए डिज़ाइन किए गए ऊर्जा-कुशल स्विच रिलक्टेंस मोटर (एसआरएम) ड्राइव के डिज़ाइन, नियंत्रण और कार्यान्वयन का गहन विश्लेषण प्रस्तुत करता है, जिसमें विद्युत गुणवत्ता में सुधार, लागत में कमी और सेंसर-रहित नियंत्रण की सुगमता पर बल दिया गया है। यह शोध कार्य पारंपरिक मोटर ड्राइव प्रणालियों से संबंधित महत्वपूर्ण मुद्दों का पता लगाता है, जिसमें उनकी दक्षता, घटकों की संख्या और विभिन्न ग्रिड स्थितियों के अनुकूल होने की क्षमता पर ध्यान केंद्रित किया गया है। शोध की शुरुआत कम विद्युत खपत वाले औद्योगिक एगजॉस्ट फैन अनुप्रयोगों के लिए डिज़ाइन किए गए एक लचीले, ऊर्जा-कुशल एसआरएम के डिज़ाइन और विकास पर विस्तार से चर्चा करने से होती है। एक अनुकूलित मोटर ज्यामिति को निर्धारित करने के लिए बेंचमार्क पर आधारित, विश्लेषणात्मक गणनाओं द्वारा समर्थित और एएनसिस मैक्सवेल में 2डी परिमित तत्व विधि (एफईएम) के माध्यम से मान्य एक पद्धति का उपयोग किया गया है। इस डिज़ाइन को भौतिक प्रोटोटाइप बनाकर प्रयोगात्मक रूप से प्रमाणित किया गया है, जो कम-शक्ति वाले एसआरएम ड्राइव अनुप्रयोगों में इसकी व्यावहारिक व्यवहार्यता को दर्शाता है। इसके अतिरिक्त, पावर फैक्टर करेक्शन (पीएफसी) कन्वर्टर टोपोलॉजी का अन्वेषण इनपुट पावर गुणवत्ता में सुधार लाने और एसआरएम ड्राइव के संदर्भ में हार्मोनिक मानकों, विशेष रूप से IEC 61000-3-2 का अनुपालन करने के उद्देश्य से किया गया है।

सिस्टम की समग्र दक्षता बढ़ाने के साथ-साथ खर्चों को कम करने के लिए, ब्रिजलेस पीएफसी कन्वर्टर का उपयोग एसिमेट्रिक ब्रिज कन्वर्टर (एबीसी) और मिड-पॉइंट कन्वर्टर (एमपीसी) द्वारा संचालित एसआरएम ड्राइव के लिए क्रमशः सिंगल-आउटपुट और डुअल-आउटपुट व्यवस्थाओं में किया जाता है। हाइब्रिड कुक, हाइब्रिड सेपिक, इंटीग्रेटेड ज़ेटा-लुओ और ज़ेटा कैपेसिटिव स्विचिंग सेल (सीएससी) कन्वर्टर सहित टोपोलॉजी को लोड और सप्लाय की विभिन्न स्थितियों में SRM ड्राइव की विशिष्ट मांगों को पूरा करने के लिए पूरी तरह से विकसित किया गया है। ये कन्वर्टर असंतुलित चालन मोड (डीसीएम) में कार्य करते हैं, जिससे स्वाभाविक रूप से पावर फैक्टर करेक्शन प्राप्त होता है और कई सेंसर और जटिल पैसिव कंपोनेंट्स की आवश्यकता कम हो जाती है। इसके अलावा, एसआरएम ड्राइव सिस्टम ऊर्जा दक्षता, पावर क्वालिटी में सुधार और कुल कंपोनेंट संख्या को कम करने के लिए पीएफसी फ्रंट-एंड के साथ सेंसर रहित नियंत्रण रणनीति को एकीकृत करता है। हॉल-इफेक्ट सेंसर को हटाकर और इलेक्ट्रिकल फीडबैक का उपयोग करके सरलीकृत अनुमान एल्गोरिदम के माध्यम से इलेक्ट्रिकल सेंसिंग को कम करके, सिस्टम लागत और डिज़ाइन की जटिलता को काफी कम कर देता है। यह दृष्टिकोण उच्च प्रदर्शन प्रदान करता है और साथ ही एक स्केलेबल और कम लागत वाला समाधान सुनिश्चित करता है, जिससे यह कम पावर, लागत-संवेदनशील अनुप्रयोगों के लिए उपयुक्त हो जाता है और पावर इलेक्ट्रॉनिक्स में कुशल और टिकाऊ मोटर ड्राइव के विकास में योगदान देता है।



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