

**DESIGN AND CONTROL OF HYBRID BUCK-SEPIC TWO-
INPUT DC-DC CONVERTER TOPOLOGIES**

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**DESIGN AND CONTROL OF HYBRID BUCK-SEPIC
TWO-INPUT DC-DC CONVERTER TOPOLOGIES**

by

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CERTIFICATE

This is to certify that the thesis entitled “**Design And Control of Hybrid Buck-Sepic Two-Input Dc-Dc Converter Topologies**” being submitted by **Mr. Vargil Kumar Eate** for the award of degree of **Doctor of Philosophy** is a record of a bonafide research work carried out by him in the Department of Electrical Engineering of Indian Institute of Technology Delhi, New Delhi. Mr. Vargil Kumar Eate worked under my guidance and supervision and has fulfilled the requirement for the submission of the thesis, which to my knowledge has reached the requisite standards. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any Degree or Diploma.

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ABSTRACT

In this thesis, design and control of hybrid buck-SEPIC two-input DC-DC converter topologies and its application in power management is investigated. The hybrid converter topologies are evolved with the aim to realize extreme step-down conversion ratios. The hybrid converters formulated in this work are: (i) Switched Inductor Hybrid Buck SEPIC two-input Converter (SIHBSTIC), (ii) Sixth-order Quadratic Buck-SEPIC two-input DC-DC Converter (QBSTIC), and (iii) Switched Capacitor-cell with Hybrid Buck-SEPIC two-input converter (SCHBSTIC) topology-1 and topology-2. All these topologies exhibit step-down voltage conversion features and are functions of two different pulse width modulated (PWM) controlling inputs. Further, they also draw power from two different voltage sources along with load sharing on the input dc-sources. All of these topologies offer the benefit of more bucking at lower duty ratios while some of the topologies exhibit quadratic bucking behavior. The topologies are evolved to not only give the benefit of more bucking but to also give the feature of lower ripple content in their source currents.

An extensive steady-state analysis of these proposed topologies is carried-out so as to understand the nature of these hybrid-buck converters. To further investigate the nature of these topologies, dynamic analysis is done and state-space models are formulated. As all these topologies belongs to multi-input multi-output (MIMO) systems and are primarily evolved for two-input applications, the transfer functions indicating the dependency of load voltage, source current on the controlling duty ratios are formulated. On the basis of these transfer functions controlling and controlled quantities dependency is identified and then their pairing is done for judicious power management.

After having enough understanding of the hybrid topologies evolved in this thesis, attention has been paid in designing the controller for achieving reliable power transfer. Though many multi-variable control strategies are possible for these hybrid buck topologies but this work primarily focuses on the Individual Channel Design (ICD), multi-variable quantitative feedback theory (QFT) based design so as to achieve controllers. By the virtue of multi-input structure, existence of interactions within the converter system are inevitable. For designing the diagonal controllers, the plant interactions dependent transfer functions need to be reflected on to the diagonal transfer functions. Although such transformation is possible but it would lead to ineffective handling of the high frequency dynamics. Thus to avoid all such transformation relevant issues and to accommodate the dynamics of the plant for the entire frequency range, a full-order or non-diagonal controller strategy design using MIMO-QFT is attempted.

Having done thorough investigations on steady-state, dynamics as well as the MIMO-controller design of all the proposed hybrid buck-SEPIC topologies, their validity is tested in the simulation platform. In all the topologies formulated, the effectiveness of the non-diagonal controller is seen both in steady-state as well as during dynamics. It clearly indicated that the resultant MIMO-controller takes into account the plant interactions effectively thus avoiding instability issues. To also test MIMO-controller effectiveness, several different disturbances are created and in all these cases the proposed topologies are stable and ensure power management indicating the designed controllers robustness.

सार

इस थीसिस में हाइब्रिड बक-एसईपीआईसी टू-इनपुट डीसी-डीसी कनवर्टर टोपोलॉजी के डिजाइन और नियंत्रण और बिजली प्रबंधन में इसके अनुप्रयोग की जांच की जाती है। हाइब्रिड कनवर्टर टोपोलॉजी को चरम स्टेप-डाउन रूपांतरण अनुपात का एहसास करने के उद्देश्य से विकसित किया गया है। इस कार्य में तैयार किए गए हाइब्रिड कनवर्टर हैं: (i) स्विच इंडक्टर हाइब्रिड बक एसईपीआईसी टू-इनपुट कनवर्टर (एसआईएचबीएसटीआईसी) (ii) सिक्स्थ-ऑर्डर क्वाड्रेटिक बक-एसईपीआईसी टू-इनपुट डीसी-डीसी कनवर्टर (क्यूबीएसटीआईसी) और (iii) हाइब्रिड बक-एसईपीआईसी टू-इनपुट कनवर्टर (एससीएचबीएसटीआईसी) के साथ स्विच कैपेसिटर-सेल टोपोलॉजी-1 और टोपोलॉजी-2। ये सभी टोपोलॉजी स्टेप-डाउन वोल्टेज रूपांतरण विशेषताओं को प्रदर्शित करते हैं और दो अलग-अलग पल्स विड्थ मॉड्युलेटेड (पीडब्लूएम) कंट्रोलिंग इनपुट के कार्य हैं। इसके अलावा, वे इनपुट डीसी-स्रोतों पर लोड शेयरिंग के साथ-साथ दो अलग-अलग वोल्टेज स्रोतों से भी बिजली प्राप्त करते हैं। ये सभी टोपोलॉजी कम शुल्क अनुपात पर अधिक बर्किंग का लाभ प्रदान करते हैं जबकि कुछ टोपोलॉजी द्विघात बर्किंग व्यवहार प्रदर्शित करते हैं। टोपोलॉजी को न केवल अधिक झुकने का लाभ देने के लिए विकसित किया गया है, बल्कि उनके स्रोत धाराओं में कम लहर सामग्री की विशेषता भी दी गई है।

इन प्रस्तावित स्थलविज्ञानों का एक व्यापक स्थिर-अवस्था विश्लेषण किया जाता है ताकि इन संकर-बक परिवर्तकों की प्रकृति को समझा जा सके। इन स्थलविज्ञानों की प्रकृति की आगे की जांच करने के लिए, गतिशील विश्लेषण किया जाता है और राज्य-अंतरिक्ष मॉडल तैयार किए जाते हैं। चूंकि ये सभी टोपोलॉजी बहु-इनपुट बहु-आउटपुट (एम. आई. एम. ओ.) प्रणालियों से संबंधित हैं और मुख्य रूप से दो-इनपुट अनुप्रयोगों के लिए विकसित किए गए हैं, इसलिए नियंत्रण शुल्क अनुपात पर लोड वोल्टेज, स्रोत धारा की निर्भरता का संकेत देने वाले स्थानांतरण कार्यों को तैयार किया जाता है। इन स्थानांतरण कार्यों के आधार पर नियंत्रण और नियंत्रित मात्राओं की निर्भरता की पहचान की जाती है और फिर विवेकपूर्ण शक्ति प्रबंधन के लिए उनकी जोड़ी बनाई जाती है।

वीआई इस थीसिस में विकसित हाइब्रिड टोपोलॉजी की पर्याप्त समझ होने के बाद, विश्वसनीय बिजली हस्तांतरण प्राप्त करने के लिए नियंत्रक को डिजाइन करने में ध्यान दिया गया है। हालांकि इन संकर बक टोपोलॉजी के लिए कई बहु-चर नियंत्रण रणनीतियाँ संभव हैं, लेकिन यह काम मुख्य रूप से व्यक्तिगत चैनल डिजाइन (आईसीडी) बहु-चर मात्रात्मक प्रतिक्रिया सिद्धांत (क्यूएफटी) आधारित डिजाइन पर केंद्रित है ताकि नियंत्रकों को प्राप्त किया जा सके। बहु-इनपुट संरचना के आधार पर, कनवर्टर प्रणाली के भीतर अंतःक्रियाओं का अस्तित्व अपरिहार्य है। विकर्ण नियंत्रकों को डिजाइन करने के लिए, संयंत्र की अंतःक्रियाओं पर निर्भर स्थानांतरण कार्यों को विकर्ण स्थानांतरण कार्यों पर प्रतिबिंबित करने की आवश्यकता होती है। हालाँकि इस तरह का परिवर्तन संभव है लेकिन इससे उच्च आवृत्ति गतिकी का अप्रभावी संचालन होगा। इस प्रकार इस तरह के सभी परिवर्तन प्रासंगिक मुद्दों से बचने के लिए और पूरी आवृत्ति सीमा के लिए संयंत्र की गतिशीलता को समायोजित करने के लिए, MIMO-QFT का उपयोग करके एक पूर्ण-क्रम या गैर-विकर्ण नियंत्रक रणनीति डिजाइन का प्रयास किया जाता है।

स्टेडी-स्टेट, डायनामिक्स के साथ-साथ सभी प्रस्तावित हाइब्रिड बक-एसईपीआईसी टोपोलॉजी के एमआईएमओ-कंट्रोलर डिजाइन पर गहन जांच करने के बाद, उनकी वैधता का सिमुलेशन प्लेटफॉर्म में परीक्षण किया जाता है। तैयार किए गए सभी स्थलविज्ञानों में, गैर-विकर्ण नियंत्रक की प्रभावशीलता स्थिर अवस्था के साथ-साथ गतिकी के दौरान भी देखी जाती है। इसने स्पष्ट रूप से संकेत दिया कि परिणामी एम. आई. एम. ओ.-नियंत्रक संयंत्र की अंतःक्रियाओं को प्रभावी ढंग से ध्यान में रखता है और इस प्रकार अस्थिरता के मुद्दों से बचता है। एम. आई. एम. ओ.-नियंत्रक की प्रभावशीलता का परीक्षण करने के लिए, कई अलग-अलग गड़बड़ी पैदा की जाती हैं और इन सभी मामलों में प्रस्तावित स्थलविज्ञान स्थिर होते हैं और बिजली प्रबंधन सुनिश्चित करते हैं जो डिज़ाइन किए गए नियंत्रक की मजबूती का संकेत देते हैं।

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Organization of the Thesis

Chapter-1: Introduction - The first chapter deals with the background literature pertaining to the evolution of two-input DC-DC converters (TICs) to cater to the needs of the hybrid and intermittent energy systems, and reliable electrical power generation systems etc. Review on conventional series-connected MICs, parallel-connected TIC topologies along with realization of pulsating voltage source and pulsating current source converters discourses. The need and significance of multi-input power processing are deliberated.

Chapter-2: Steady-state analysis and design of two-input hybrid converter topologies - In this chapter the steady-state analysis of SIHBSTIC, SCHBSTIC, QBSTIC will be discussed. The modes of operation are analyzed. The mathematical expressions of the steady-state voltage gain for the TICs, comparison of the voltage gain, output voltage variation, design the elements of MICs, voltage and current stress across the devices, source, and load ripple variations is studied and a comparison is made for all the TICs.

Chapter-3: Dynamic modeling of two-input DC-DC converters - In this chapter the dynamic behavior and stability of any TIC system operating with and without a controller can be entirely defined by using the six small-signal transfer functions (SSTF). For all the TICs this SSTFs is derived and the frequency responses of the SSTFs and the Frequency sweep plots of the same are superimposed to check the validity of the mathematical modeling. As the controller is designed the Discrete-time model formulation and relevant mathematics are derived.

Chapter-4: MIMO QFT Controller design methods - MIMO Control strategies are applied to TICs, the control pair identification using RGA and its interpretations is discussed. The implementation of SMIMOQFT, DDMIMOQFT, and ICD in the simulation environment with relevant discussion and the result analysis is discussed.

Chapter-5: Conclusions and future scope and Future Scope - This chapter gives the conclusions of the thesis work.

CHAPTER - 1

1. INTRODUCTION TO TWO-INPUT DC-DC CONVERTERS

Harvesting energy from renewable energy sources and fulfilling the ever-increasing power demand is gaining momentum in the modern era and has thus paved the path for the development of new technologies in the arena of hybrid DC power distribution systems [1]. Systems for renewable energy are built using several power sources that have distinct V-I characteristics. Power electronics converters that are dependable and extremely efficient are required to integrate these many renewable energy sources. Traditionally, separate DC-DC converters are used to mix various renewable energy sources. However, these setups are expensive and cumbersome. The conventional design exhibits a somewhat intricate structure, resulting in decreased overall effectiveness and inadequate dependability. Using multi-input DC-DC converters (MIC), several single-input renewable energy systems, such as fuel cells and photovoltaic cells (PV), can be paired to supply the load. Several renewable DC sources can be connected in series to create a single source as one technique [1] – [2]. Using PWM converters in parallel, with or without electrical isolation, is a further technique [3]. They are more efficient and feature a small design. These MICs have the ability to deliver power to loads from several renewable sources, either simultaneously or independently [4]. The goal of this thesis intends to develop two-input DC-DC converters (TICs) that can provide excessive bucking operation.

The following are the available power sources that can be used ([4], [5], [6]) to enhance the primary source capability.

- (i) Photo-voltaic generators (PVG's)
- (ii) PV energy harvested with AC mains
- (iii) Wind distribution systems
- (iv) Fuel cell systems
- (v) Battery energy storage systems
- (vi) Hybrid ultra-capacitor storage-based DC systems

Power must be utilized judiciously to cater to the excessive power demand, aided by proper power conversion methodologies. Renewable energy sources are intermittent, i.e., they cannot produce power continuously at a constant rate, and their power levels change continuously. This necessitates their integration with conventional sources so that the energy produced from renewable sources is effectively utilized and the burden on the primary source is reduced and shared with the intermittent sources to some extent. Since the voltage levels of different sources vary with time, it is not advisable to connect them in parallel. In order to transfer power between various sources and the load efficiently, a suitable power conversion system is needed, and it is here that the multi-input DC-DC converters (MICs) find their role [7].

Considering many applications, an assortment of numerous special types of switched-mode DC-DC converters, belonging to conventional and derived topologies are being proposed and their feasibility concerning many applications are presented in the literature. Integrating one or more different sources is made possible with evolution of integrated converters. Such a combination of different sources either collectively or individually feeding a common bus is being recognized as one of the prospective areas for research [8].

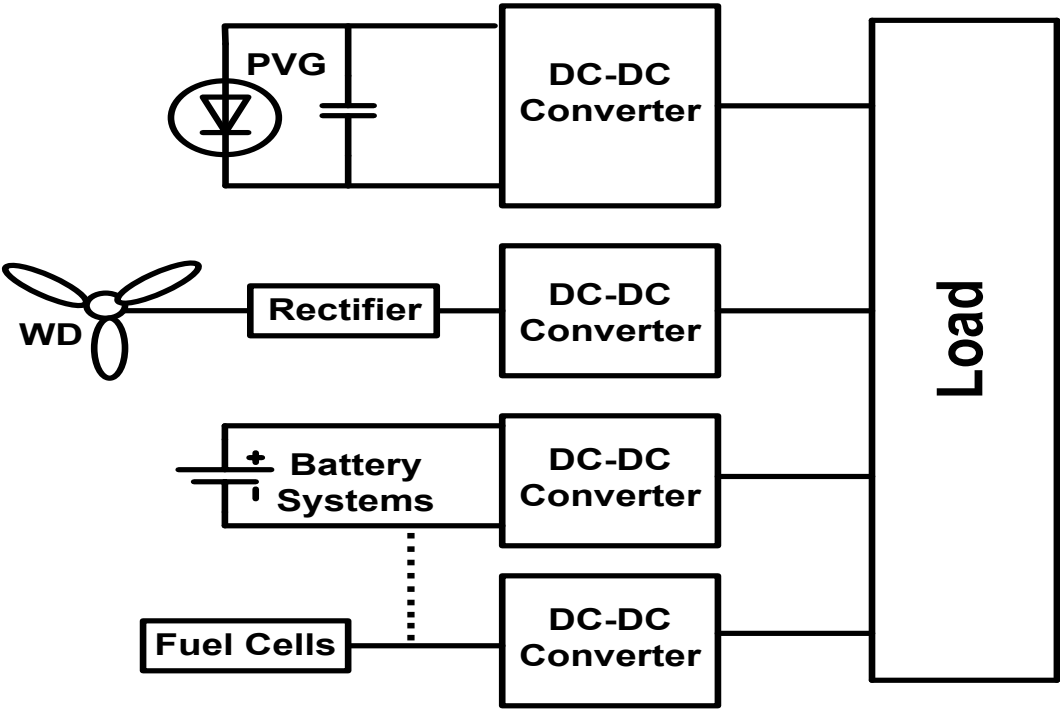


Fig. 1. 1. Hybrid energy systems with independent converters.

Associating a converter to each energy source was adopted in the traditional methods of MICs, which is flexible in terms of operation point of view and is a viable option for the hybrid vehicles of automotive industries, and even in remote DC stand-alone power supply system as shown in Fig. 1.1. The hybrid energy systems are shown in Fig. 1.2 connects different energy sources through a MIC to feed the load.

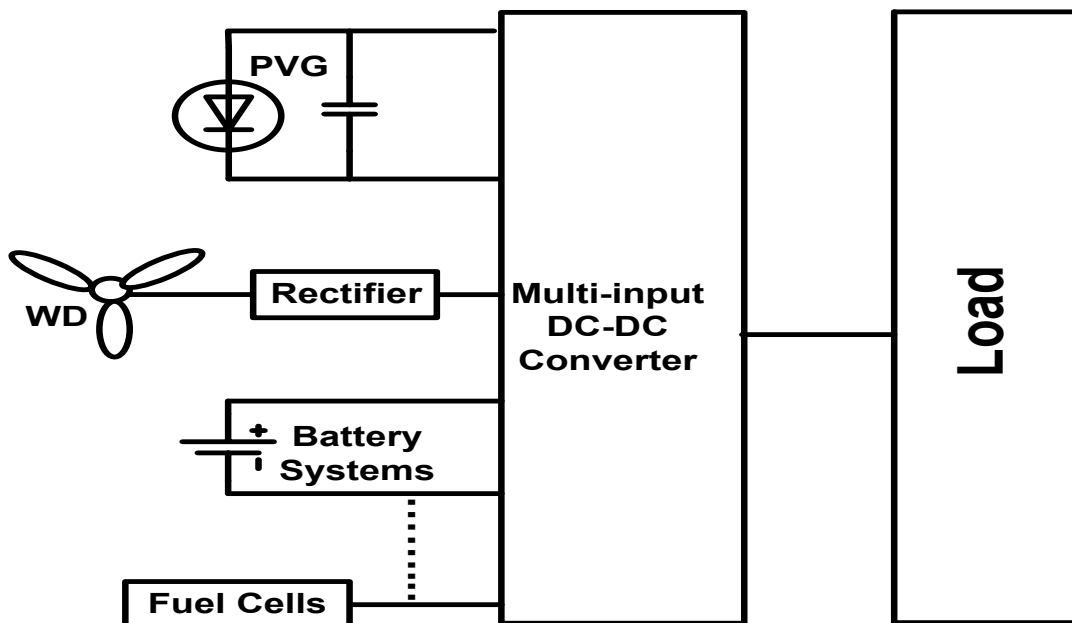


Fig. 1. 2. Structure of hybrid energy systems with multi-input converters [9].

1.1 Conventional Converters

The block diagram is shown in Fig. 1. 3 depicts a system in which converters are connected in parallel. Separate DC-DC conversion stages are utilized for individual sources. These converters are connected together at the dc bus and controlled freely. In certain systems, a communication bus may be included to exchange information and manage power flow between the sources. Various examples of such converters are interleaved boost converters. The main drawback of such a system lies in the fact that it is inherently complex and has a high cost due to the multiple conversion stages and communication devices between individual converters [10].

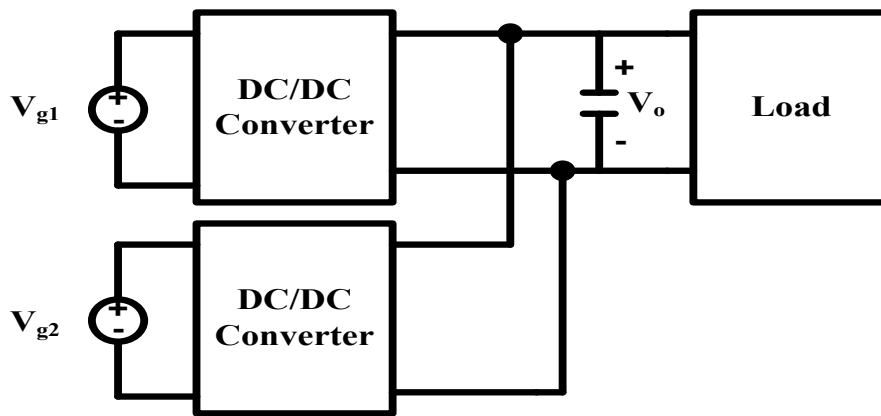


Fig. 1. 3. Structure of parallel-connected MIC converter [11].

The circuit shown in Fig. 1.4 is an integrated-type, two-input DC-DC converter. This setup has a few advantages, including the fact that (i) if one DC source fails to supply the load, the other DC source will continue to do so, and (ii) if one of the input DC sources' power-supplying capacities are limited, additional power will come from another source. It is more advantageous to use multi-input converters rather than several independent converters as it results in fewer number of components, simple control, more stability, and lower power losses in the system. The DC-DC converter topology has the following advantages: the DC source can deliver power to the load individually or and the magnitude of the input DC voltage can be higher or lower than the one with a regulated output.

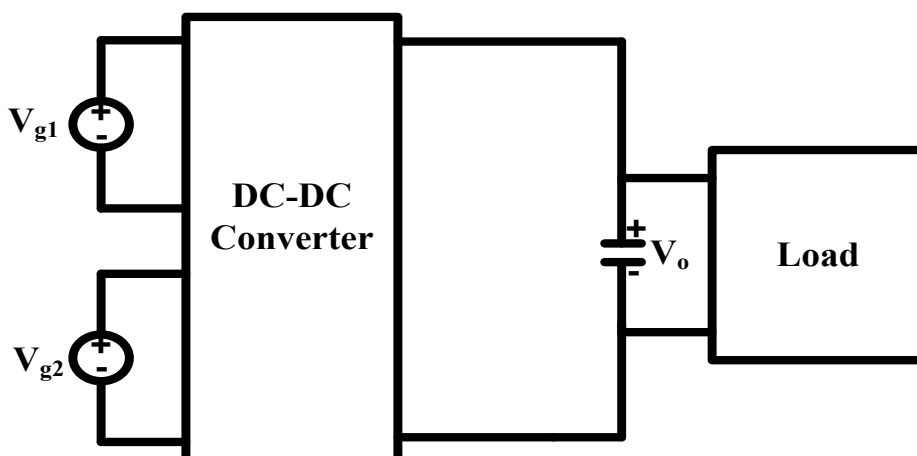


Fig. 1. 4. Integrated type DC-DC converters [12].

1.2 Significant Developments in MICs and their Control Strategies

The usefulness of MICs in obtaining regulated output voltage for clean electric power generation systems is given in [2]. Here, the basic principle of the two-input isolated buck-boost converter is introduced along with its modes of operation. It later discusses the solar arrays and AC commercial lines that use two-input power sources for isolated DC-DC converter with magnetic coupling to obtain voltage regulation. The equivalent circuit approach, theoretical aspects of steady-state and dynamic characteristics, and stability of TICs have also been presented. A Buck-Boost Multi-input DC-DC converter (MIC) topology for obtaining the combination of many dc sources which can accommodate various sources automatically with interchangeable input sources, with less part count of two energy storage elements and analyzed the converter in both continuous and discontinuous modes of operation has also been proposed [13]. The power supplies design based on inductor-less switched capacitor pocket computer systems, the concept of switching capacitor cells capable of charging in series and discharging in parallel are studied, the feature of average voltage across the switched and reduction of stresses and losses in the switches is presented in [4]. Various methods of synthesizing MICs and identifying feasible topological inception methods by introducing Pulsation Voltage Source Cells (PVSCs) and Pulsating Current Source Cells (PCSC) was discussed [12]. It also discussed the formation of feasible MICs along with methods of identification of quasi-MICs. Feasible inception regions are explained with certain rules and guidelines in all the six primary PWM DC-DC converters. The paper [14] proposed a novel double-input topology for high/low voltage source, three techniques for identifying a double input converter discussed concerning Buck-Buck-Boost configuration and later inception of the soft-switching cell was demonstrated to reduce the switching losses and improved the efficiency. It also discussed the method of generating gate pulses to the respective switches. In [15], MIC topology integrating multiple sources to a single converter with two energy storage elements was proposed which also realized the bi-directional operation of the same and was able to give the buck, boost and buck-boost

modes of operation separately without using any additional transformer with fixed frequency switching control strategy. The paper [16] presented a concept of using MICs to distributed generation based utility grids, where micro-sources connected to high-voltage sources were used as power inputs to telecom power supplies, emphasizing more on minimizing the energy storage requirements and also proposed simple input current control approaches to MICs.. The author of [17] discussed the feasibility of using MICs for Hybrid and Electric Vehicles and the flexibility of MICs for storage units like batteries, ultra-capacitor banks, etc., were also discussed. The paper discussed the usage of MICs for harvesting available energy using a buck-boost MIC and MICs with energy storage units and thereby converting regulated DC to AC. Its application to hybrid electric propulsion drives was also studied, and an attempt was made to investigate the optimal and feasible solution for different designs. The author of [18] discussed the Buck-SEPIC MIC topology, and its discrete-time model, the concepts and application of MIMO control theory to MICs, the concept of application of interaction based analysis, power management strategy and digital controller design for voltage regulation on for load and source disturbances are analyzed. To study the interactions, relative gain array technique (RGA) was used. Excellent mathematical analysis was done at different parts while explaining the concept. The closed-loop operation of the converter proposed was validated by using simulation and also experimentation. By the inception of switching capacitor and switching inductor cell based DC-DC converters, development of hybrid converters was carried out [19]. Both for high and low voltage realization, different topologies consisting of switched-inductors, switched-capacitors and multiplier structures are evolved ([5], [14], [20], [21], [22], [22], [23], [24]). Many evolutions of quadratic buck, as well as boost converters, are reported [25]-[26] and these are one of the prospective areas of research applicable to multi-input DC-DC converters.

Modeling of power electronic converters play an important role in studying and designing of realistic systems ([29], [48]). In the modern days digital control of power supplies has evolved as an attractive feature, because of high flexibility, reliability, programmability and advanced

control algorithms ([18], [27], [28], [29], [30]). Multi-input power electronic systems have many common energy storage elements which exchange of power. To study such interaction behavior several control theories were developed. A well-known interaction analysis method is relative gain array theory ([55], [56], [58]). The decentralized as well as the centralized controllers ([59], [60], [61], [62]) were adopted to regulate and manage the multi-input power electronic systems ([63], [64], [65], [66]).

1.3 MOTIVATION

The load distribution on the two-input voltage sources and the balance of input-output power are the two key issues in the power management of multi-input DC-DC converters involving a combination of DC-DC converters with two or more input sources, which can be energy storage units like batteries, ultra-capacitors, etc. Multi-input DC-DC converters are meant for integrating renewable energy sources, assisting in reducing the burden on primary (battery) sources and meeting the power demands of various applications like electric vehicles, telecom power supplies, etc. The operation of multi-input DC-DC converters for wide power conversion ranges with different capacities of input voltages and their control using digital control methodologies is a challenging issue. Therefore, suitable control approaches are needed for fulfilling power distribution demands.

A DC-DC power conversion is a form of power conditioning, i.e., the process of receiving power with a given voltage or current waveform and delivering that power, which is received on the output side, in a different form, which results in a change in the level of voltage or current (bucking, boosting operations). Over the years, significant research has been done in this area, and many new converter topologies have been developed that fall under the same classification as either bucking converters or boosting converters. All other topologies are derived from these two basic topologies. For example, the Buck-Boost topology is a combination of both buck and

boost topologies. Some other buck-boost topologies presented in the literature are Cuk, SEPIC, dual SEPIC converters, etc. [45]. The SEPIC has the following advantages:

- i. Reduced source current ripple
- ii. The operation of SEPIC converter in buck and boost mode while transferring power from source to load aids in the smooth operation of converter even at fluctuating loads.
- iii. Absence of common ground problem between source and load.
- iv. Absence of problems of inverted output voltage prevailing in CUK, high input current ripple in Zeta converters, etc.

While evolving the topologies, the following are the important considerations:

- a. For monitoring the power conversion during switching operation, various DC-DC conversion systems must have at least one variable resistor.
- b. At least one inductor must be present in a DC-DC converter so that volt-second balance may be applied to the inductor of the converter for obtaining the voltage gain expression. (amp-second balance in case of capacitor).

The development of technology has led to several applications, such as modern high-power consumption CPUs, telecom power supplies for providing internet services [19], high-intensity lighting for head lamps of electric vehicles, etc., that require either voltage bucking, boosting, or both. Furthermore, operating MOSFET gate drivers and switcher ICs with an excessive duty cycle may result in penalties for efficiency and minimum on-time limits. The active transistor in step-down converters and the diode (self-driven transistor) in step-up converters have very short conductivities. This means that the high duty cycle may even cause problems at high switching frequencies. Such parameters have an impact on the input voltage source, which is burdened since it must deliver a wide range of voltage and current profiles [19], [31].

The fundamental concepts of hybrid and quadratic converters are utilized with SEPIC and have been amalgamated with the multi-input converter leading to the evolution of two-input converter topologies. On the basis of this concept, many hybrid TIC's can be evolved but this thesis has primarily focused on the following topologies: (i) Switched inductor Hybrid Buck-SEPIC TIC (SIHBSTIC) [32], (ii) Switched-Capacitor Hybrid Buck-SEPIC TIC (SCHBSTIC) topology-1 and topology-2 ([33],[34]), and (iii) Quadratic Buck-SEPIC TIC (QBSTIC) ([35],[36]).

1.4. Objectives and Contribution of the Thesis

The objectives of the thesis are:

Firstly, four different two-input topologies based on hybrid and quadratic converters are developed. An extensive steady-state analysis is carried out to obtain the voltage transformation ratio of the respective topologies as well as to identify the benefits offered by them. Secondly, the design of the parameters of these two-input integrated DC-DC converters is done to explore their feasibility.

In order to understand the underlying issues prevailing in these two-input converter topologies, small-signal models that work with multiple-variable control frameworks are created. A detailed investigation is carried out to understand the interactions existing in the proposed topologies and choose the suitable control variable pairings of the controlled quantities. Once the control loops are paired, the right control strategy for regulating voltage and current must be created. This is done using a quantitative feedback transformation method. Validation of the designed strategy is done both in MATLAB and in circuit simulators.

CHAPTER - 2

2. STEADY-STATE ANALYSIS AND DESIGN OF TWO-INPUT HYBRID CONVERTER TOPOLOGIES

- The development of DC grids, decentralized power, and power generation has had a minimum impact on the environment and paved the way for the exploration of clean energy resources [2]. Realizing clean power generation is a challenging issue, and sufficient attention has been paid globally. Meeting the load demand through a single energy source is a difficult task, and thus the need to integrate such energy sources arises. All the sources may not have identical voltage and current profiles, and thus their interconnection is not straight-forward. In this context, power electronics technologies are able to provide reliable solutions as these converters are effective in interfacing different kinds of sources with a variable degree of voltage and current profiles. Recently, many multi-input DC-DC converters (MIC) have been reported in the literature suitable for sources exhibiting variable voltage and current profiles [13]. These MICs offer many advantages, of which a few salient benefits are: better versatility, reliability, and better utilization of power generated from clean energy sources [13]. The primary goal of MICs is not only to tap energy from various sources with different voltage-current profiles, but they should also perform the following tasks:
 - They should tap energy from multiple inputs and should have the capability to feed it to a common DC bus/load.
 - To the possible extent in the context of TICs each of the input to output port combinations should behave more like an individual PWM converter, for convenient transfer of the power.

- The MIC should not allow any exchange of power among the sources, i.e. the MIC must act as a unidirectional converter, however the exception is given if one of the sources is a battery.

While formulating the MICs with desired **voltage transformation ratios**, the features mentioned above are to be taken into account. A brief review of the existing MIC topologies which were formulated on the basis of step-down voltage transformation is discussed in the subsequent section.

2.1. Step-down Voltage Gain based Multi-input Converters

Buck-based topologies are more popular when loads are to be fed at lower voltages. MIC has to exhibit a step-down voltage conversion feature in order to feed a common load (connected to a low-voltage bus) by drawing power from multiple high-voltage sources. In this context, many MIC formulations are possible to generate by integrating other topologies with buck converters. As shown in Fig. 2.1, one such converter is a two-input integrated converter, which is the result of combining two buck converters. This MIC is capable of drawing power from two different high-voltage input sources, either simultaneously or individually. In this case, the sources supply pulsating currents, and hence handling the ripple current is the major issue in this MIC. To overcome this ripple issue, additional input filters are required to be connected, but at the expense of increased control complexity as well as reduced power density.

Another MIC that is capable of drawing power from two different input sources but exhibits a buck plus buck-boost transformation is shown in Fig. 2.2. This MIC is more straightforward in structure as it uses a smaller number of switches, diodes, and inductors as compared to the parallel connection of many individual converters. This dual-input DC-DC converter can draw power from two different voltage sources simultaneously or individually. Further, it always allows power flow from source to load, i.e., acts as a unidirectional converter.

The two integrated topologies discussed above can generate either buck or buck-boost voltage transformation ratios but exhibit high ripple content at the side of the source. To minimize

the ripple content and yet realize the buck-boost voltage transformation, a single-ended primary inductance converter (SEPIC) is integrated with the buck converter, as shown in Fig. 2.3, and is identified as the Buck-SEPIC two-input converter (TIC) [4]. In this converter, the ripple in one of the source currents is very low, and this feature comes without the addition of input filters. A two-input Buck-SEPIC converter uses one buck and one SEPIC converter, the integration of which led to the reduction of component count by one inductor and hence resulted in a fourth-order system, as shown in Fig. 2.3.

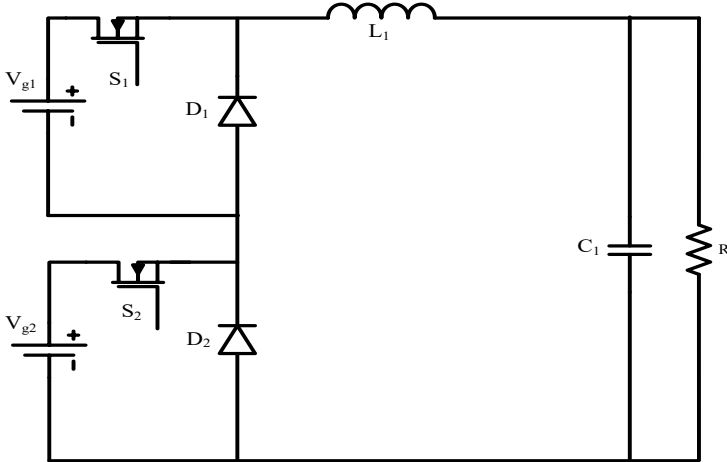


Fig. 2.1 Integrated buck-buck Converter

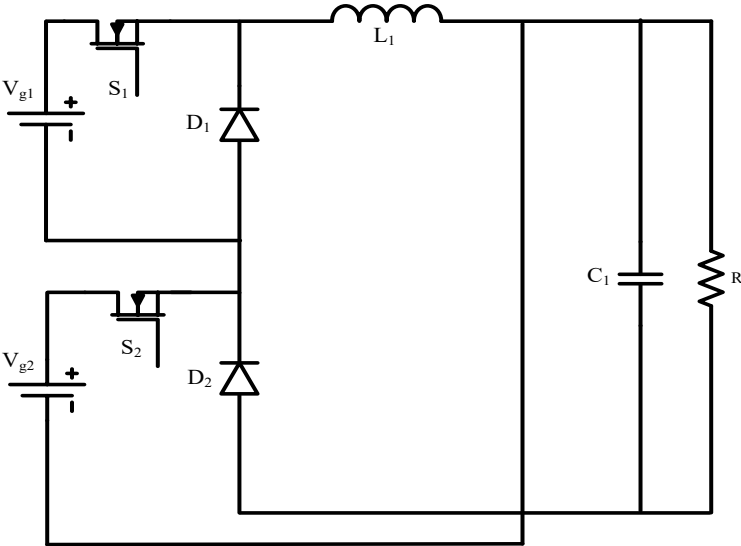


Fig. 2.2 Buck-buck boost converter

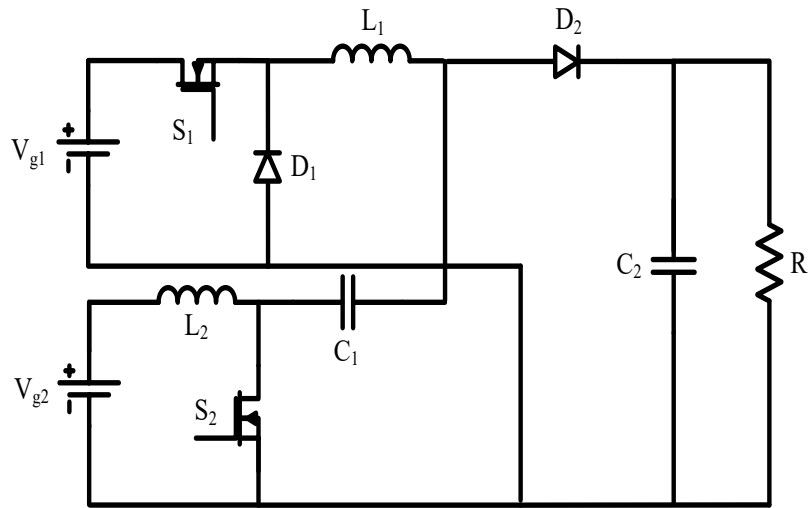


Fig. 2. 3 Two-input Buck-SEPIC converter.

Table 2.1 Output Voltage of TICs with the variation of d_1 and d_2 for $V_{g1}=36V$, $V_{g2}=12V$

Converter Topology	Output Voltage Equation	Variation of load voltage with duty ratio's
Buck-Buck	$V_o = V_{g1}d_1 + V_{g2}d_2$	
Buck-Buck-boost	$V_o = \frac{V_{g1}d_1}{(1-d_2)} + \frac{V_{g2}d_2}{(1-d_2)}$	
Buck-SEPIC TIC	$V_o = V_{g1}d_1 + V_{g2} \frac{d_2}{1-d_2}$	

From Fig. 2.4 it can be observed that load voltage is a function of both the duty ratios d_1 and d_2 . Moreover, Buck integrated Buck—Buck-Boost topology gives maximum load voltage [4], [37] compared to the other two topologies for the same duty ratios d_1 and d_2 . The buck-buck topology gives the least load voltage compared to other topologies for the same duty ratios.

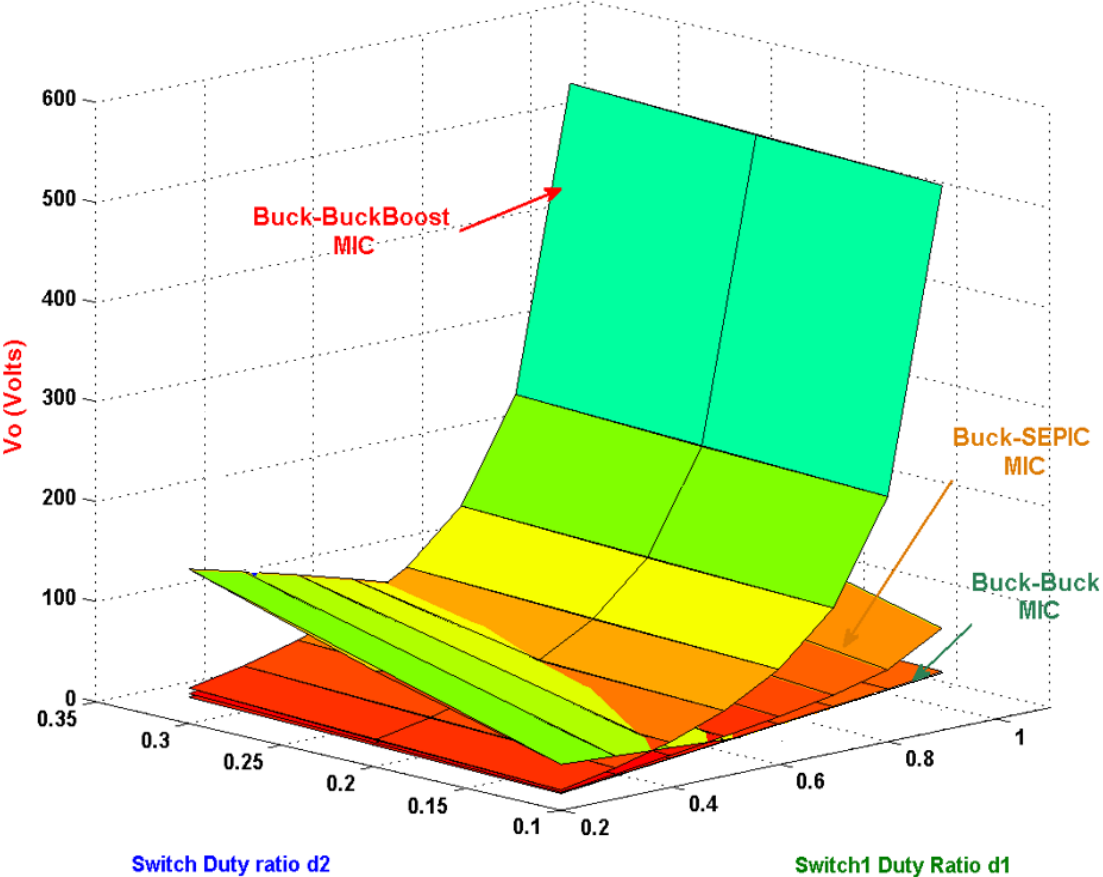


Fig. 2.4. Comparison of V_o of Various Buck based Multi-Input DC-DC Converter.

2.2 Hybrid Buck-SEPIC Topologies

The above discussed integrated topologies need to be operated at extreme duty ratios (d_1 , d_2) in order to maintain constant voltage against wide variation in the respective input voltages. Such operation may result in (i) higher source current ripple content, (ii) higher device stress, and (iii) reduced efficiency. To preserve the features of the Buck-SEPIC converter and to achieve additional bucking along with reduced ripple content in the sources, a hybrid switched-inductor

cell (SIC) and a switched-capacitor cell (SCC) are added into primary converters [19]. This led to the development of the Two-Input Hybrid Buck-SEPIC DC-DC Converters ([18]-[22]).

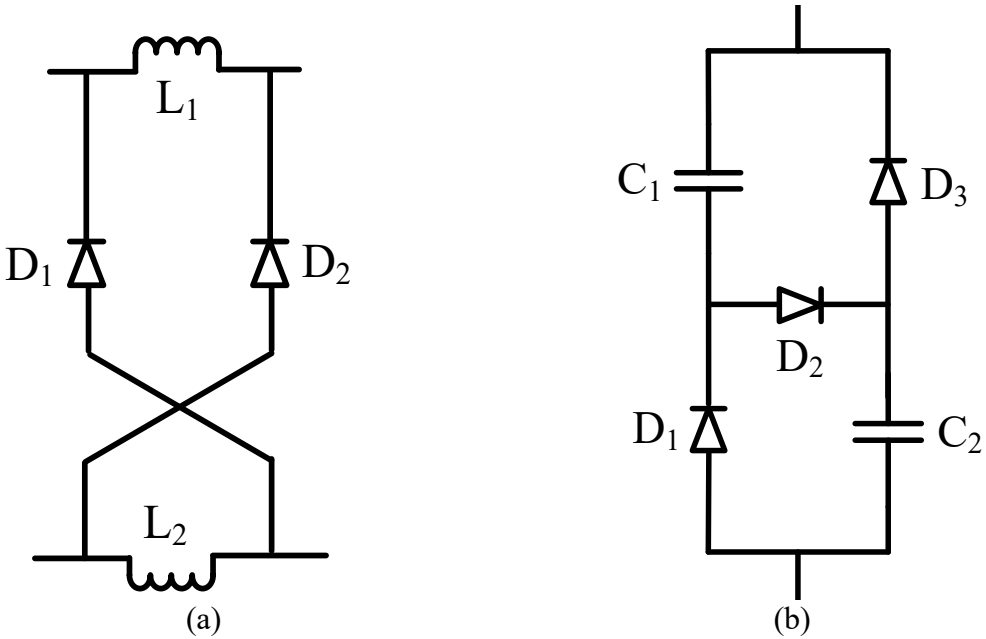


Fig. 2. 5. (a) Switched Inductor cell (SIC) (b) Switched-Capacitor cell (SCC).[19]

Though the amalgamation of SIC and SCC into primary DC-DC converters is feasible, it has the following limitations: (i) increase in their order, (ii) incurring of more losses due to increased component count, and (iii) tedious controller design. Despite these factors, it possesses better steady-state performance characteristics along with wider voltage transformation ratios.

On considering the above-stated points, firstly, modification to BSTIC (Fig. 2.3) is done by adding an inductor and a diode (shown in Fig. 2.5 (a)) to BSTIC to achieve extra-buckling of the output voltage. This led to the formulation of the Switched Inductor Hybrid Buck SEPIC Two-Input Converter (SIHBSTIC), shown in Fig. 2.6.

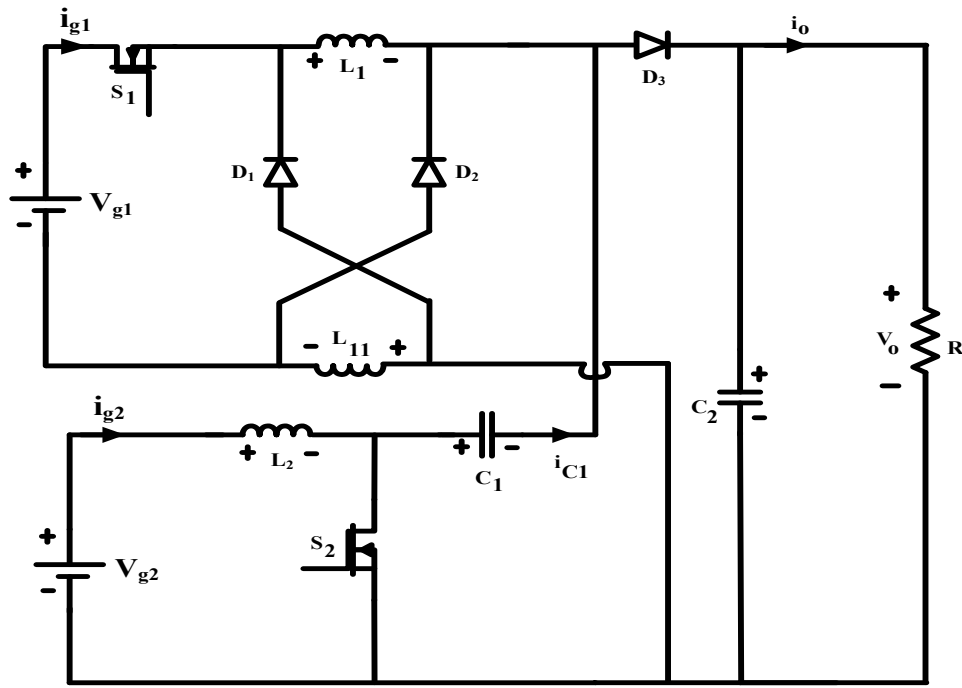
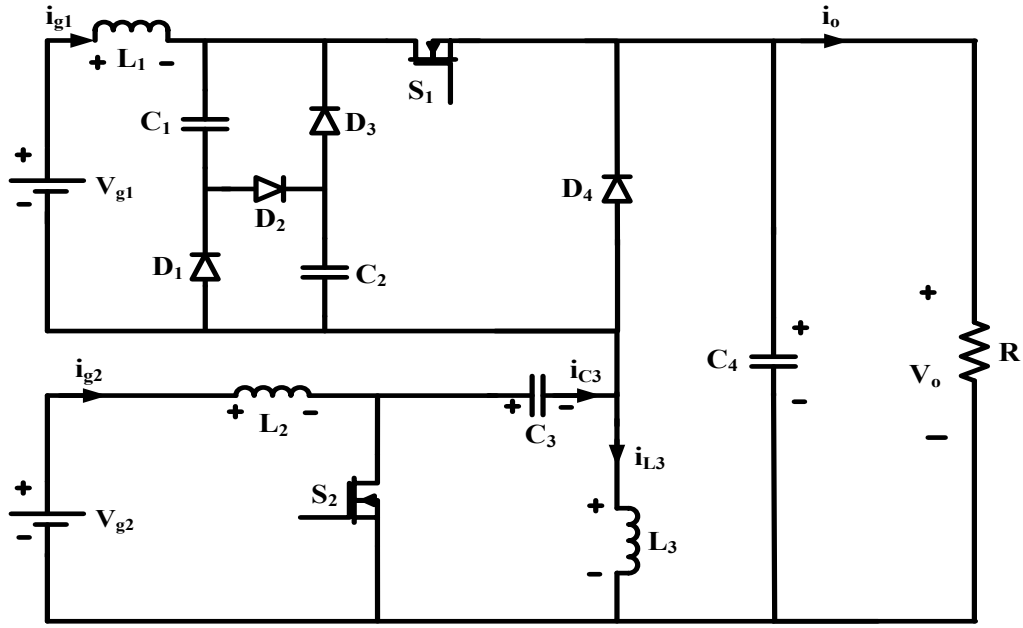


Fig. 2.6. Circuit Diagram of SIHBSTIC.

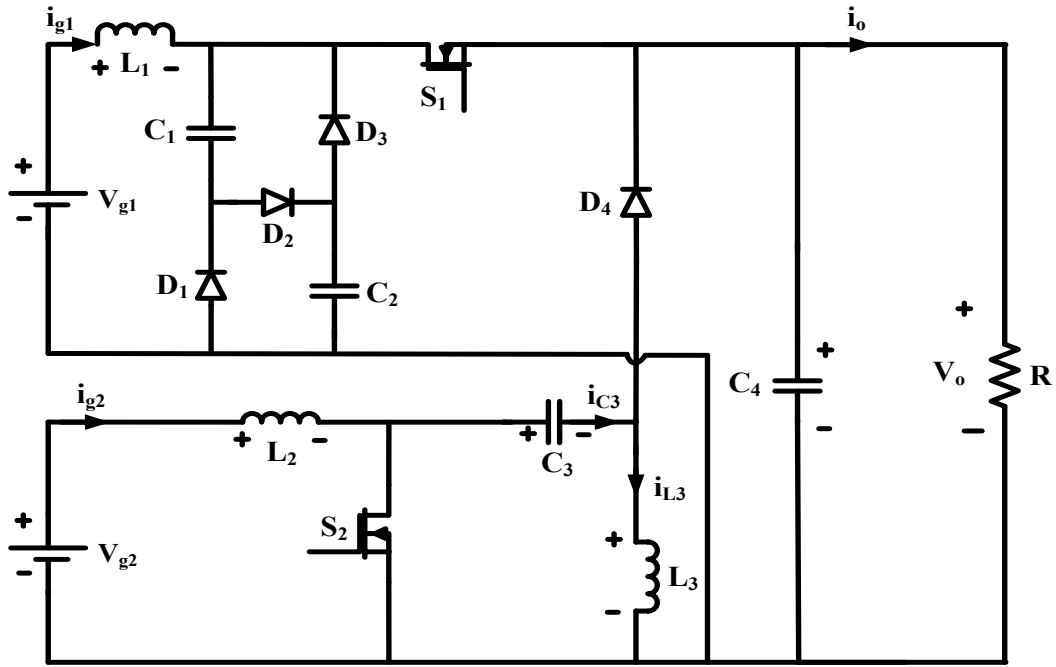
Applying volt-second balance to the inductors, the voltage gain expression is obtained as

$$V_o = V_{g1} \left(\frac{d_1}{(2-d_1)} \right) + V_{g2} \left(\frac{d_2}{(2-d_1)(1-d_2)} \right) \quad (2.1)$$

The SIHBSTIC, shown in Fig. 2.6, can deliver power to the load from two different voltage sources simultaneously or individually, and the topology consists of five energy storage elements which results in a fifth-order system. On observing the output voltage expression in eq. (2.1), the voltage gain is almost half of the BSTIC, it is observed that the source is connected to switch, which raises the possibility of high input source current ripple. To deal with this drawback; a second converter is formulated by initially incorporating an L-C input filter at source-1 (V_{g1}) of the BSTIC converter. The capacitor of the input L-C filter is replaced by a switched-capacitor cell (SCC) shown in Fig. 2.5(b), which led to the evolution of the new topology, as shown in Fig. 2.7. The topology has been formulated by combining the switched capacitor cell with a hybrid buck-SEPIC converter and is named as two-input DC-DC switched capacitor cell with the hybrid buck-SEPIC converter (SCHBSTIC). It is a seventh order converter that offers the benefit of source current ripple minimization with extra bucking of the output voltage.



(a) Topology-1



(a) Topology-2

Fig. 2.7. Circuit diagram of SCHBSTIC, integrated and parallel TICs.

Applying volt-second balance to the inductors, the voltage gain expression is obtained as
For SCHBSTIC Topology-1,

$$V_o = V_{g1} \frac{d_1 - d_2}{(2 - d_1 - 3d_2 + 2d_1d_2)} + V_{g2} \frac{2d_2(1 - d_1)}{(2 - d_1 - 3d_2 + 2d_1d_2)} \quad (2.2a)$$

For SCHBSTIC Topology-2,

$$V_o = V_{g1} \left[\frac{(d_1 - d_2)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right] + V_{g2} \left[\frac{2d_2(1 - d_1)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right] \quad (2.2b)$$

Though the SCHBSTIC topologies have the combined advantages of extra bucking of the output voltage at larger duty ratios and reduced source current ripple, it has a disadvantage of developing negative source current at lower duty ratios (d_1 and d_2) which violates one of the constraints imposed on MICs. The next modification was to incorporate a switched Inductor cell into the BSTIC in order to Overcome these drawbacks while maintaining the feature of extra-bucking and unidirectional current flow, a sixth-order quadratic buck-SEPIC two-input DC-DC converter (QBSTIC), depicted in Fig. 2.8

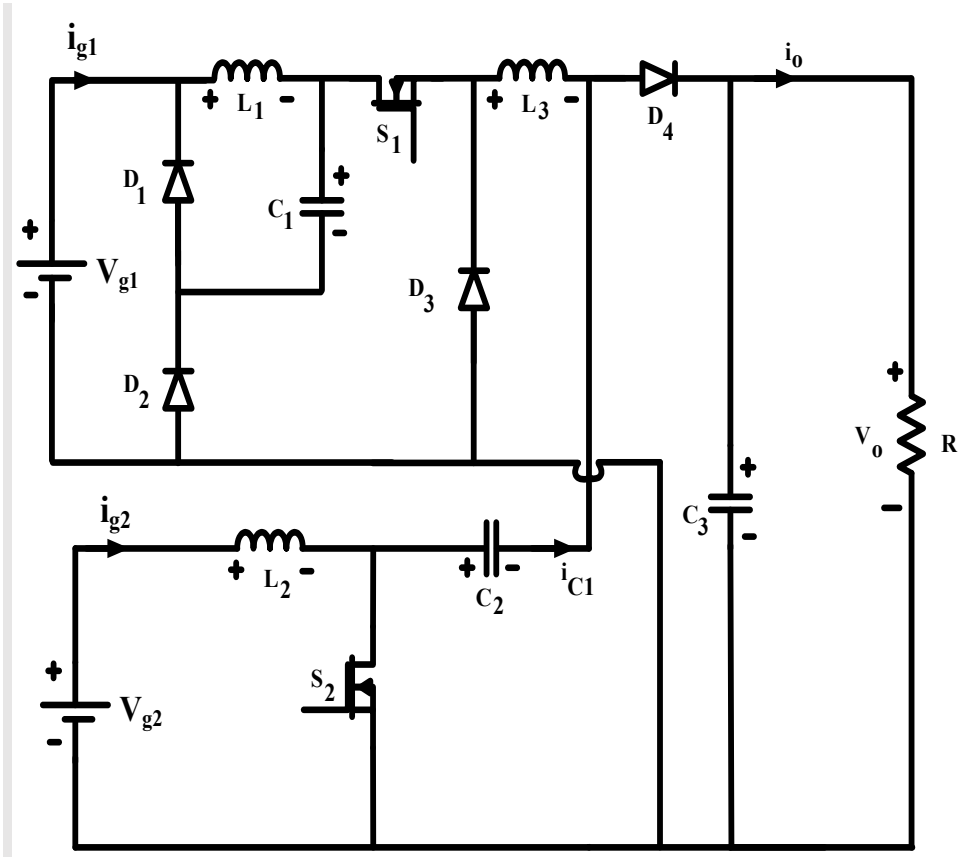


Fig. 2.8. Circuit Diagram of QBSTIC.

Applying the volt-second balance to the inductors the voltage gain expression is obtained as

$$V_o = V_{g1}d_1^2 + V_{g2} \left(\frac{d_2}{1-d_2} \right) \tag{2.3}$$

2.3 Switched Inductor Hybrid Buck-SEPIC TIC Topology

The circuit diagram of the SIHBSTIC shown in Fig. 2.9 consists of two input voltage sources, high voltage source V_{g1} and low voltage source V_{g2} , output voltage V_o . Input sources can be batteries, PV, fuel cells or any other dc sources.

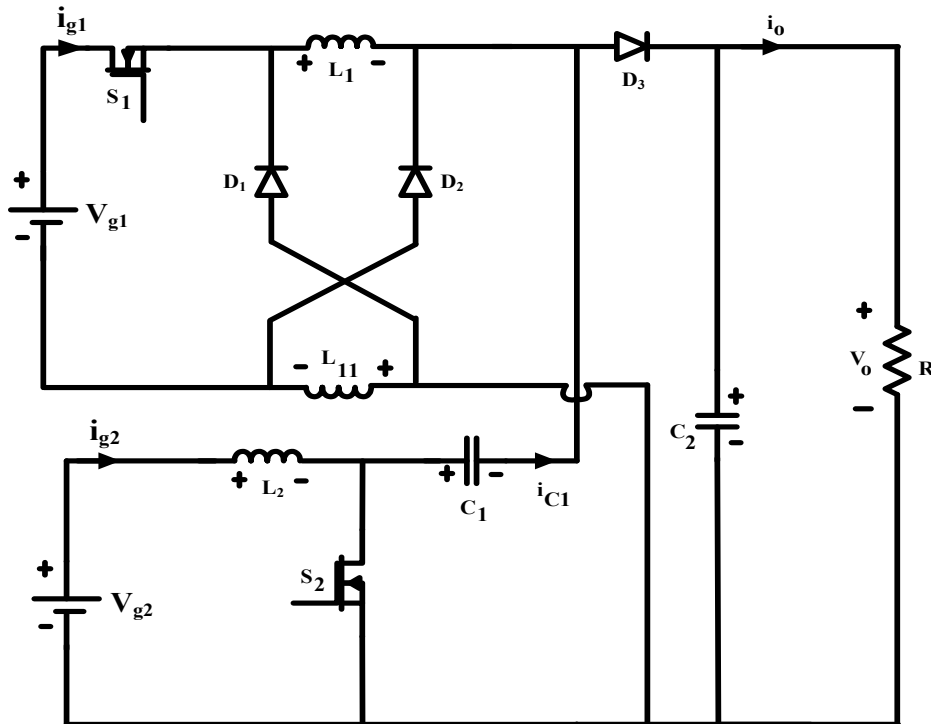


Fig. 2. 9. Circuit Diagram of SIHBSTIC.

The converter can deliver power from the two sources simultaneously or individually by operating the power switches S_1 and S_2 . This results in three modes of operation in one switching cycle. The number of stages may vary as it depends on the switching frequency, the magnitude of the load, and the source voltages. The converter operation also relies on the pulse width modulation (PWM) signals of the S_1 and S_2 phase differences. They can be synchronized either for trailing or leading-edge operations. Furthermore, three different modes are possible depending on the load demand and available power from each DC source. They are case (i) $P_1 > P_2$ or $d_1 > d_2$, case (ii) $P_1 < P_2$ or $d_1 < d_2$, case (iii) $P_1 = P_2$ or $d_1 = d_2$ where P_1, P_2 are the powers of the two sources; d_1, d_2 are duty ratio of switch S_1 and S_2 respectively. In cases (i) and (ii), there are three switching modes of operation are possible, namely S_1, S_2 on, S_1 on, S_1 off. However,

$P_1 = P_2$ or $d_1 = d_2$ case will result in only two operating modes. In the majority of the cases, the circuit has to operate either for $d_1 > d_2$, or $d_1 < d_2$, but in this thesis, $d_1 > d_2$ the case is analyzed for trailing-edge synchronized switching signals. For $d_1 > d_2$ the case, the switching instants and the turn-on and turn-off sequences are given in Table 2.3. A similar procedure is adopted for modeling for all the topologies considered in this thesis.

2.3.1 Modes of operation of SIHBSTIC

The equivalent circuit diagram for the operating modes of SIHBSTIC is shown in Figs. 2.10, 2.11, and 2.12 whereas the key waveforms is shown in Fig. 2.13. In mode-1, the switching devices S_1 and S_2 are turned ON, while diodes D_1 , D_2 , and D_3 are in turned-OFF. In this mode, the source V_{g1} will charge the inductors L_1 , L_{11} in series while that of source V_{g2} charges inductor L_2 respectively. The load demand is met by the load capacitor C_2 alone. The intermediate capacitor C_1 gets discharged through the conducting switch S_2 .

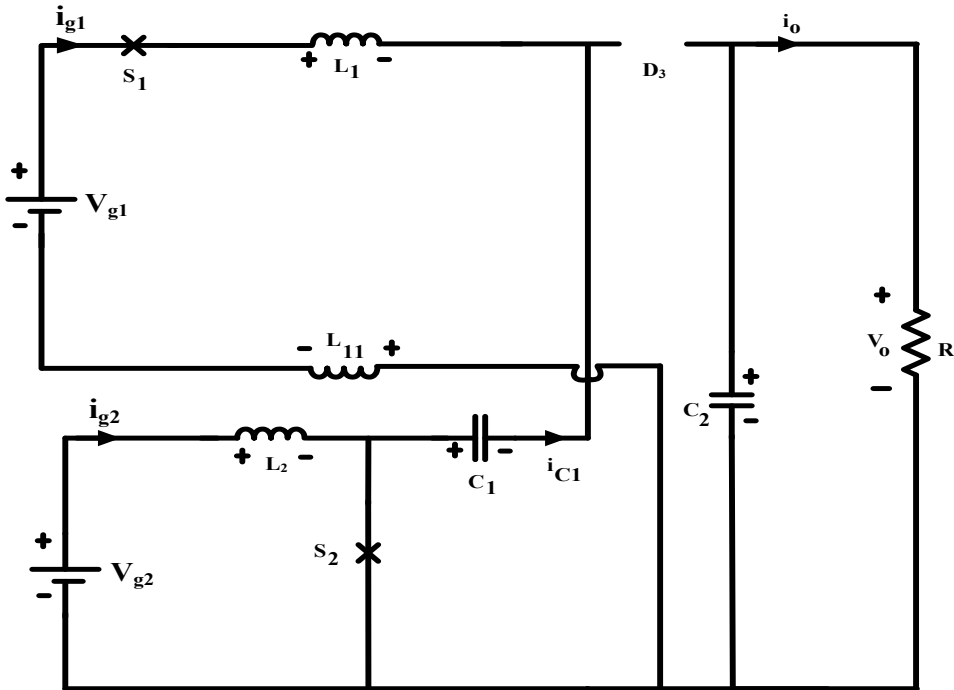


Fig. 2.10. Equivalent circuit diagram for mode-1 operation.

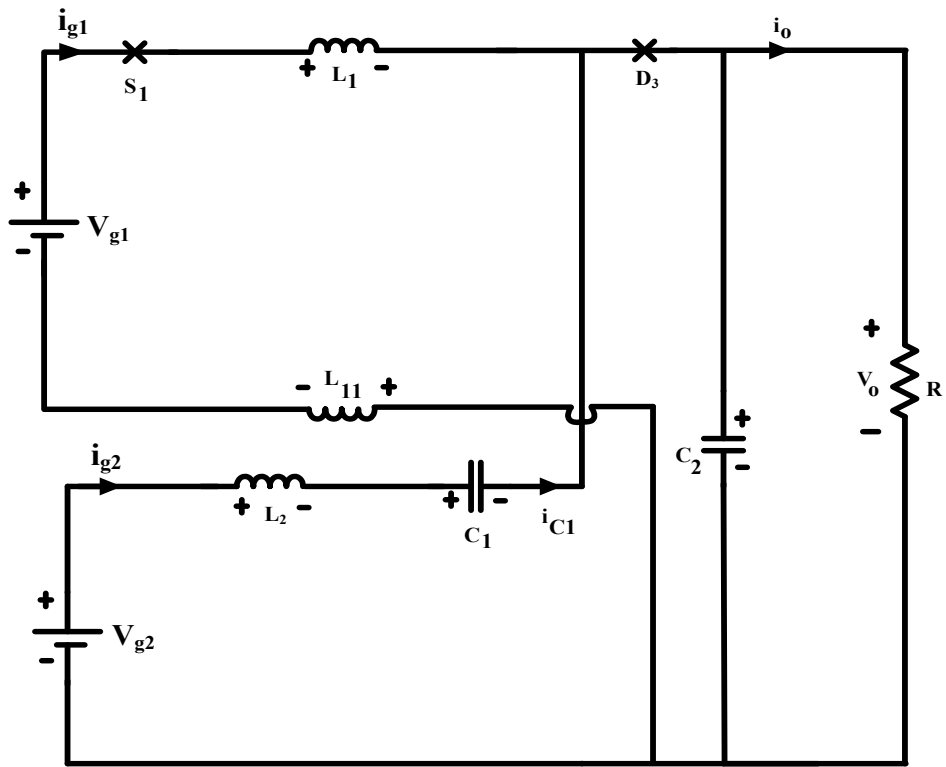


Fig. 2.11. Equivalent circuit diagram for mode-2 operation.

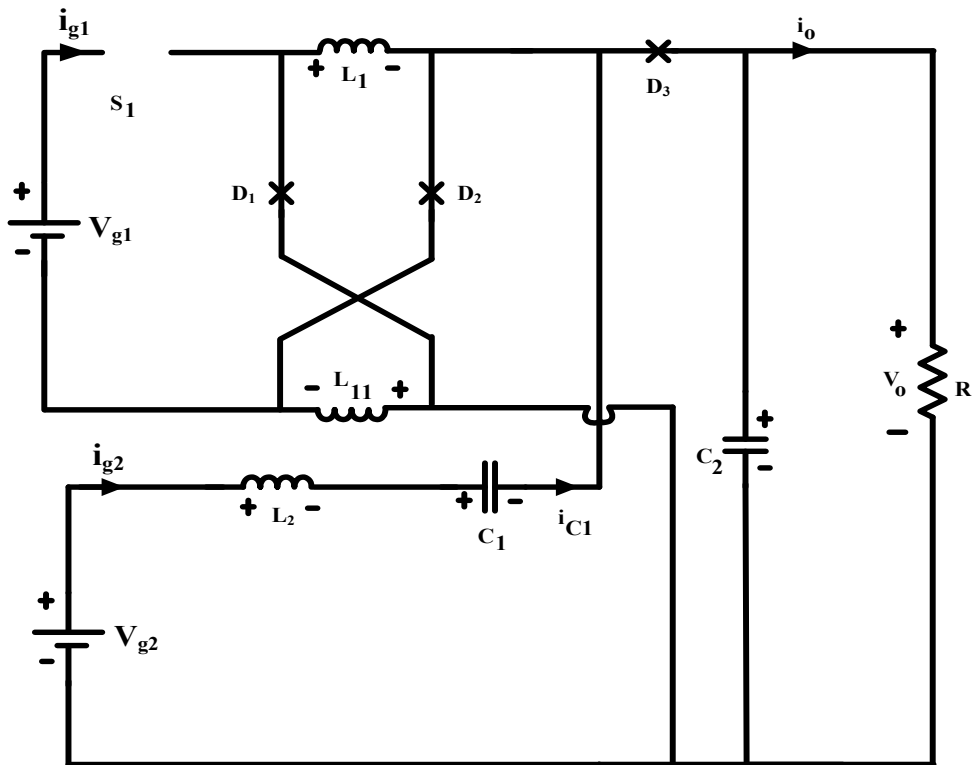


Fig. 2.12. Equivalent circuit diagram for mode-3 operation.

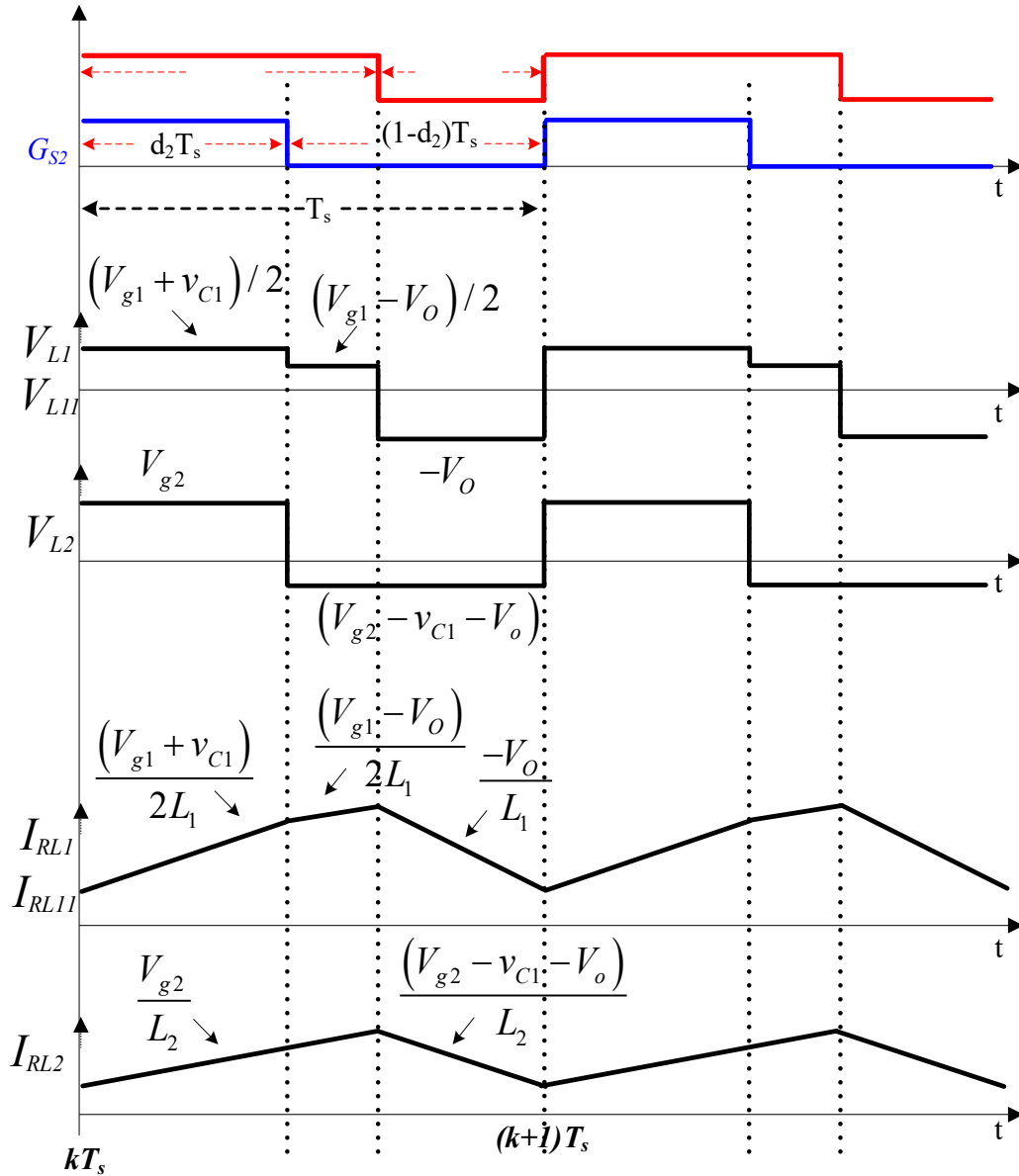


Fig. 2. 13 Fundamental Waveforms of SIHBSTIC.

The equivalent circuit of mode-2 is shown in Fig. 2.11, wherein the power switching devices S_1 is turned ON and S_2 are turned OFF, while D_1 , D_2 is in OFF state and D_3 is in ON state. In this mode, the source V_{g1} will charge the inductors L_1 , L_{11} , while the load demand is met by the sources V_{g1} and V_{g2} . The intermediate capacitor C_1 gets charged through inductor L_2 . The equivalent circuit of mode-3 is shown in Fig. 2.12 wherein S_1 , S_2 is in the OFF-state and diode D_3 is ON state. Diodes D_1 and D_2 are ON, and they will provide a bypass path for inductor currents i_{L1} , i_{L11} . In this mode, the load demand is met by the source, V_{g2} . The voltage conversion ratio of the converter can easily be derived by applying volt-second balance to the inductors.

Assuming the parasitic resistances of the inductor are negligible and solving the KVL equations of the inductor for different modes of operation, which are reported in Annexure-1, the voltage conversion ratio of this converter is obtained as follows:

$$V_o = V_{g1} \left(\frac{d_1}{2-d_1} \right) + V_{g2} \left(\frac{d_2}{(2-d_1)(1-d_2)} \right) \quad (2.4)$$

The above equation is formulated under the assumption of negligible parasitic components. However, in reality, this voltage gain depends on the non-idealities of the converter and the load connected to it.

2.3.2 Design of SIHBSTIC Topology parameters

The ripple-based design approach is used to design the elements of SIHBSTIC. It was reported in the literature that “a good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 40%, [81], [82] and while to that of the voltage ripple is assumed to be less than 10% [81],[82]. The design parameters for validation are listed in Table 2.10.

Design of Inductors, Capacitors:

The design of inductors L_1 , L_{11} , and L_2 are based on voltage expressions given in Table 2.2 and Table 2.3, and the capacitors are designed based on the current expressions listed in Table 2.4.

Table 2.2. The voltage across inductor L_1 of SIHBSTIC

Mode-1 For $D=d_2$	Mode-2 For $D=(d_1-d_2)$	Mode-3 For $D=(1-d_1)$
<p>The voltage across inductor L_1 during d_2T_s</p> $L_1 \frac{di_{L1}}{dt} = \frac{V_{g1} - V_{C1}}{2}$ $L_1 = \left(\frac{V_{g1} - V_o}{\Delta I_{L1} f_s} \right)$	<p>The voltage across inductor L_1 during $(d_1-d_2)T_s$</p> $L_1 \frac{di_{L1}}{dt} = \frac{V_{g1} - V_o}{2}$ $L_1 = \frac{(V_{g1} - V_o)(d_1 - d_2)}{\Delta I_{L1} f_s}$	<p>The voltage across inductor L_1 during $(1-d_1)T_s$</p> $L_1 \frac{di_{L1}}{dt} = -V_o$ $L_1 = \frac{(-V_o)(1-d_1)}{\Delta I_{L1} f_s}$

Table 2.3. The voltage across inductor L_2 of SIHBSTIC

Mode-1 For $D=d_2$	Mode-2 For $D=(d_1-d_2)$	Mode-3 For $D=(1-d_1)$
<p>The voltage across inductor L_2 during d_2T_s</p> $L_2 \frac{di_{L2}}{dt} = V_{g2}$ $L_2 = \left(\frac{V_{g2}}{\Delta I_{L2}} \right) d_2 T_s$	<p>The voltage across inductor L_2 during $(d_1-d_2)T_s$</p> $L_2 \frac{di_{L2}}{dt} = V_{g2} - V_{c1} - V_o$ $L_2 = \frac{(V_{g2} - V_{c2} - V_o)(d_1 - d_2)}{\Delta I_{L2} f}$	<p>The voltage across inductor L_2 during $(1-d_1)T_s$</p> $L_2 \frac{di_{L2}}{dt} = V_{g2} - V_{c2} - V_o$ $L_2 = \frac{(V_{g2} - V_{c2} - V_o)(1 - d_1)}{\Delta I_{L2} f}$

Table 2.4. KCL expressions of SIHBSTIC

Modes of operation	Capacitor Current of C_1	Capacitor Current of C_2
Mode - 1 for $D=d_2$	$i_{C1} = -i_{L1}$	$i_{C2} = -I_o$
Mode - 2 for $D=(d_1-d_2)$	$i_{C1} = i_{L2}$	$i_{C2} = -I_o$
Mode - 3 for $D=(1-d_1)$	$i_{C1} = i_{L2}$	$i_{C2} = 2i_{L1} + i_{L2} - I_o$

The converter specifications are mentioned in Table 2.5 and switching frequency ' f_s ' is chosen as 50 kHz for all the converters [80],[81]. The mathematical expressions of all the energy storage elements are obtained and tabulated in Table 2.6.

Table 2.5 Converter voltage and power ratings

Parameter	Specifications
V_{g1}	36 V
V_{g2}	12 V
V_o	24 V
P_o	~ 100 W
R	~ 10 Ω

For the converter rating mentioned in Table 2.5, the component values are computed and are presented in Table 2.6. The converter voltage and power ratings listed in Table 2.5 are considered for computing the energy storage elements for all the TICs.

Table 2.6. Converter L-C expressions and parameters

Element	SIHBSTIC Parameters	Rating
L_1	$\frac{V_o}{\Delta i_{L1} f_s}$	175 μH
L_{11}	$\frac{V_o}{\Delta i_{L1} f_s}$	175 μH
L_2	$\frac{V_{g2} d_2}{\Delta i_{L2} f_s}$	230 μH
C_1	$\frac{V_o}{R f_s \Delta v_{c1}} \left(\frac{d_1 d_2}{(2-d_1)(1-d_2)} \right)$	150 μF
C_2	$\frac{V_o(1-d_1)}{R \Delta v_{c2} f_s}$	100 μF

The expressions for obtaining other parameters of the TIC are reported in Annexure-1.

The subsequent sections discuss the steady-state analysis and design of the SCHBSTIC Topology-1 and QBSTIC.

2.4 Switched Capacitor Hybrid Buck SEPIC Two-input DC-DC Converter

Topology-1

The SCHBSTIC Topology-1 is shown in Fig. 2.14. In this proposed converter, both the sources are always connected through an inductor and hence the source current ripple is low. Furthermore, the subsequent switched-capacitor stage provides a steep step-down voltage gain at moderate duty ratios. This is one of the salient features of this converter which is also responsible for better switch utilization. **Depending on the load demand, the source side inductor currents can either be smooth continuous waveform, or discontinuous waveform.** One of the areas of applications of TIC is DC-grids, and its voltage levels vary depending upon

the size of the grid. In low voltage grids, the source current magnitude is higher (if supplying higher loads). So for most of the loads, the inductor currents are continuous. Taking into account of this, the converter is analyzed here for the continuous current mode of operation only. The $d_1 > d_2$ case is analyzed here for the trailing-edge synchronized switching signals, which was implemented for the converters mentioned above also. The equivalent circuits for these operating modes are shown in Figs—2.15 to 2.17. The fundamental waveforms of the converter are given in Fig. 2.18. The status of the conducting devices of SCHBSTIC Topology-1 is given in Table 2.7.

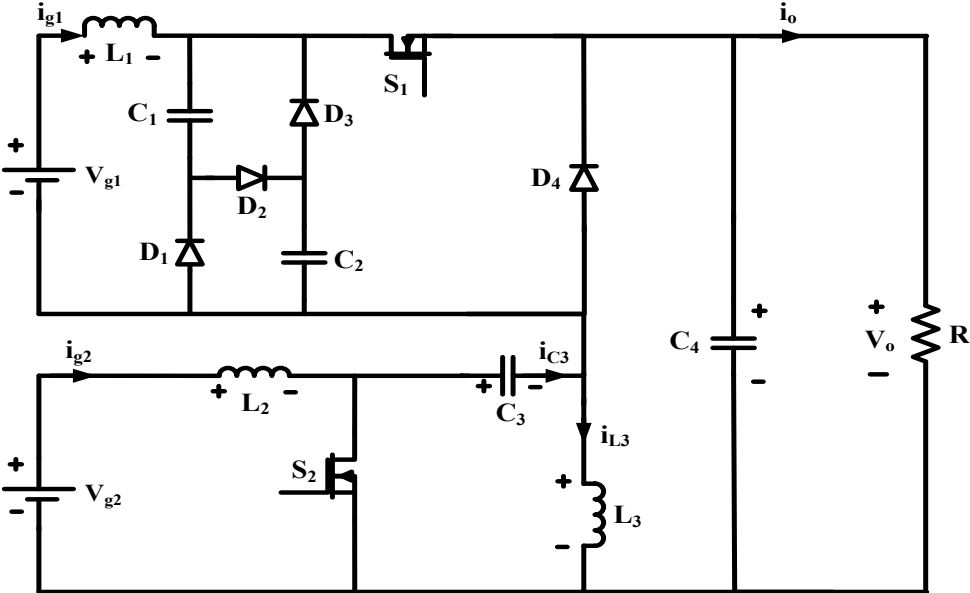


Fig. 2. 14. Circuit diagram of SCHBSTIC Topology-1.

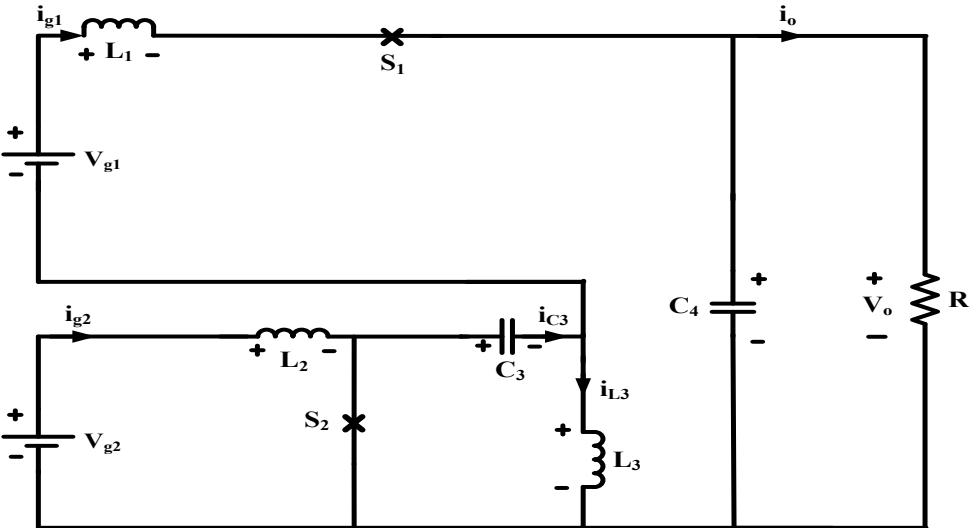


Fig. 2. 15. Equivalent circuit of Mode-1 of SCHBSTIC Topology-1.

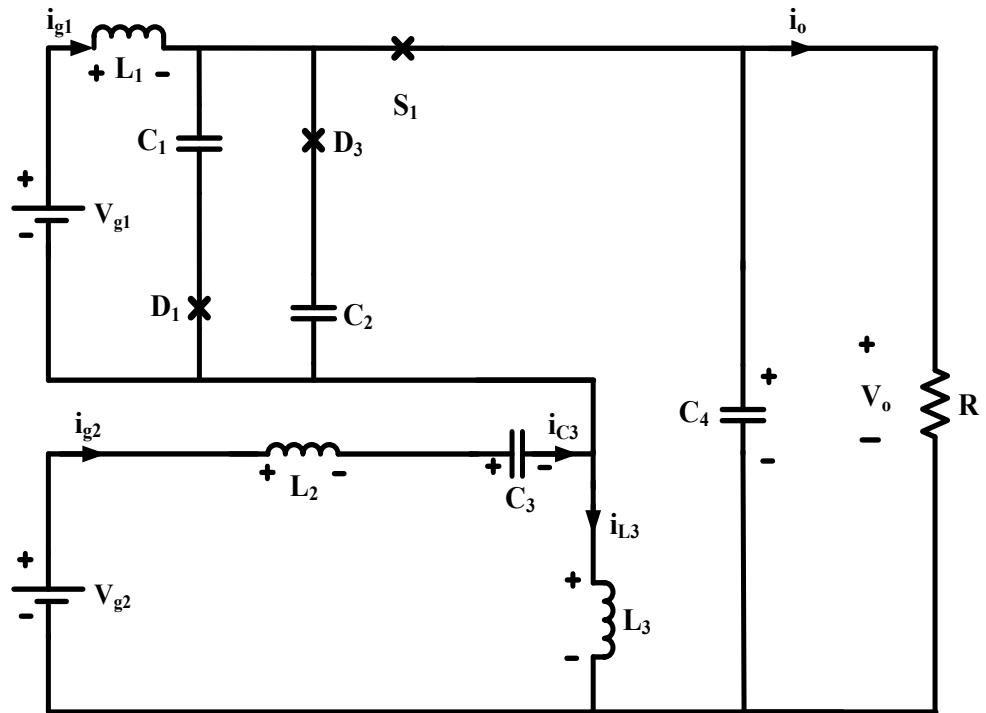


Fig. 2. 16. Equivalent circuit of Mode-2 of SCHBSTIC Topology-1.

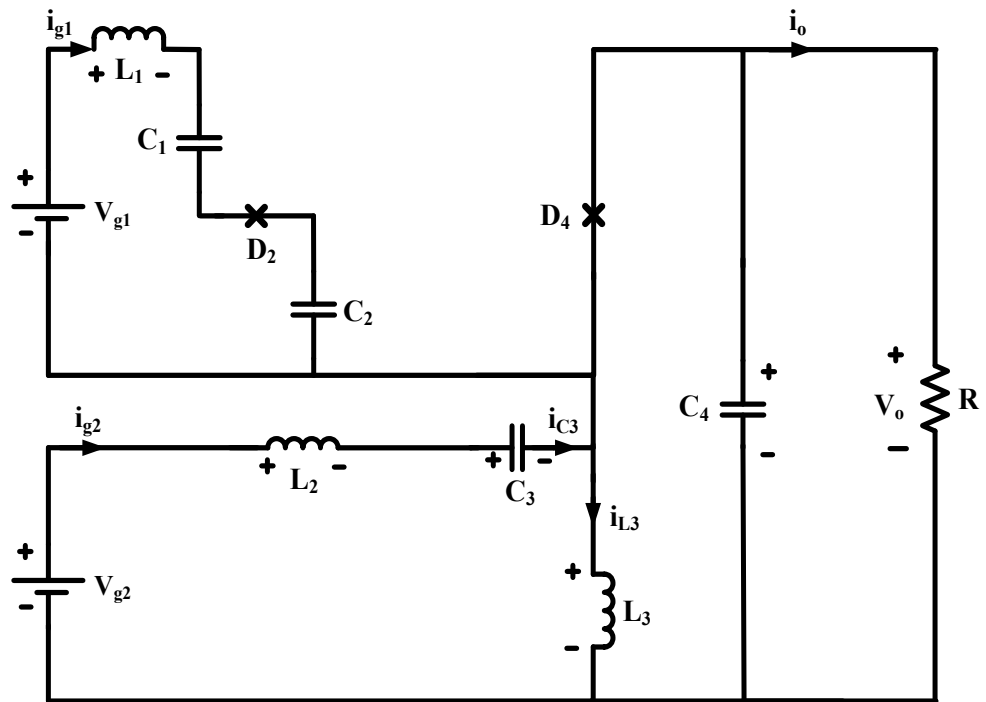


Fig. 2. 17. Equivalent circuit of Mode-3 of SCHBSTIC Topology-1.

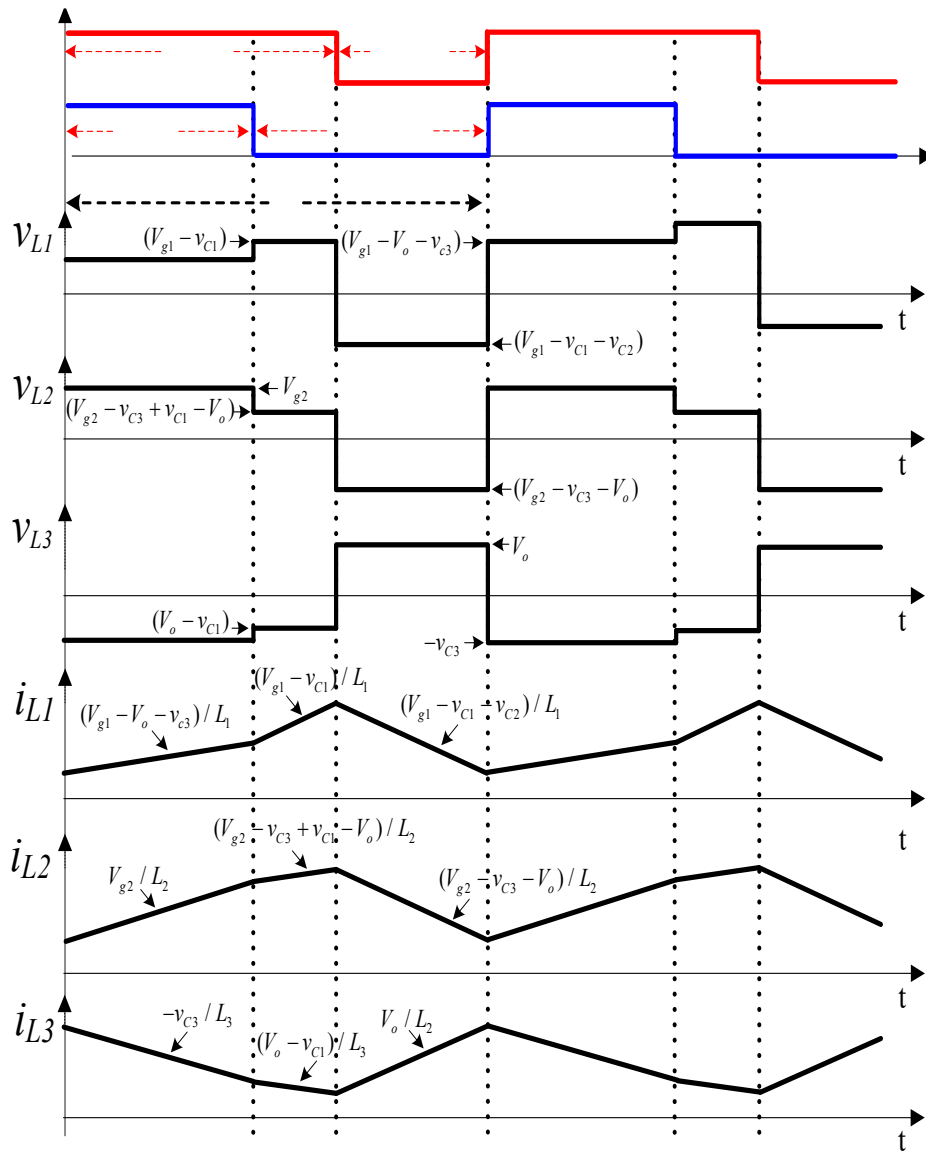


Fig. 2. 18. Key waveforms of SCHBSTIC Topology-1.

Table 2. 7. Status of the conducting devices of SCHBSTIC Topology-1

Mode	Devices-ON	Devices-OFF
Mode-1	S_1, S_2, D_2	D_1, D_3, D_4
Mode-2	S_1, D_2, D_4	S_1, D_1, D_3
Mode-3	D_2, D_4	S_1, S_2, D_1

Table 2. 8. Operating modes of SCHBSTIC Topology-1

Working Modes	Inductor voltages (v_{L1} , v_{L2} , v_{L3})	Supplying Source	ON-state switch
Mode-1	$v_{L1} = (V_{g1} - V_o - v_{c3})$	V_{g1}	S_1
	$v_{L2} = V_{g2}$	V_{g2}	S_2
	$v_{L3} = -v_{C3}$	-	
Mode-2	$v_{L1} = (V_{g1} - v_{C1})$	V_{g1}	S_1
	$v_{L2} = (V_{g2} - v_{C3} + v_{C1} - V_o)$	V_{g2}	
	$v_{L3} = (V_o - v_{C1})$	-	
Mode-3	$v_{L1} = (V_{g1} - v_{C1} - v_{C2})$	-	
	$v_{L2} = (V_{g2} - v_{C3} - V_o)$	V_{g2}	
	$v_{L3} = V_o$		

Assuming the parasitic resistances of Inductor are negligible, and solving the KVL equations of inductor for different modes of operation which are reported in Annexure-1, the voltage conversion ratio of this converter is obtained as:

$$V_o = V_{g1} \frac{d_1 - d_2}{(2 - d_1 - 3d_2 + 2d_1d_2)} + V_{g2} \frac{2d_2(1 - d_1)}{(2 - d_1 - 3d_2 + 2d_1d_2)} \quad (2.5)$$

2.4.1 Design of SCHBSTIC Topology-1 parameters

The ripple-based design approach is used to design the elements of SCHBSTIC Topology-1. The peak-to-peak current ripple is assumed to be less than 20%, while the voltage ripple is assumed to be less than 10%. The design parameters for validation are listed in Table 2.10.

Inductor Design L_1

Table 2. 9. The voltage across inductor L_1 of SCHBSTIC Topology-1

Mode-1 for $D=d_2$	Mode-2 for $D=(d_1-d_2)$	Mode-3 for $D=(1-d_1)$
Voltage across inductor L_1 during d_2T_s	Voltage across inductor L_1 during $(d_1-d_2)T_s$	Voltage across inductor L_1 during $(1-d_1)T_s$
$L_1 \frac{di_{L1}}{dt} = V_{g1} - V_o - v_{c3}$	$L_1 \frac{di_{L1}}{dt} = \frac{V_{g1} - V_o}{2}$	$L_1 \frac{di_{L1}}{dt} = (V_o - v_{c1} - v_{c2})(1-d_1)T_s$
$L_1 = \left(\frac{V_{g1} - V_o - v_{c3}}{\Delta I_{L1} \times f_s} \right) d_2 T_s$	$L_1 = \frac{(V_{g1} - V_o)(d_1 - d_2)}{\Delta I_{L1} \times f_s}$	$L_1 = \frac{(V_o - v_{c1} - v_{c2})(1-d_1)}{\Delta I_{L2} \times f_s}$

Inductor Design L_2

Table 2. 10. Voltage across inductor L_2 of SCHBSTIC Topology-1

Mode-1 for $D=d_2$	Mode-2 for $D=(d_1-d_2)$	Mode-3 for $D=(1-d_1)$
Voltage across inductor L_2 during d_2T_s	Voltage across inductor L_2 during $(d_1-d_2)T_s$	Voltage across inductor L_2 during $(1-d_1)T_s$
$L_2 \frac{di_{L2}}{dt} = V_{g2}$	$L_2 \frac{di_{L2}}{dt} = V_{g2} - V_{c3} + V_{c1} - V_o$	$L_2 \frac{di_{L2}}{dt} = V_{g2} - V_{c3} - V_o$
$L_2 = \left(\frac{V_{g2}}{\Delta I_{L2}} \right) \times d_2 T_s$	$L_2 = \frac{(V_{g2} - V_{c3} + V_{c1} - V_o)(d_1 - d_2)}{\Delta I_{L2} \times f}$	$L_2 = \frac{(V_{g2} - V_{c3} - V_o)(1-d_1)}{\Delta I_{L2} \times f}$

Inductor Design L_3

Table 2. 11. Voltage across inductor L_3 of SCHBSTIC-1

Mode-1 for $D=d_2$	Mode-2 for $D=(d_1-d_2)$	Mode-3 for $D=(1-d_1)$
Voltage across inductor L_3 during d_2T_s	Voltage across inductor L_3 during $(d_1-d_2)T_s$	Voltage across inductor L_3 during $(1-d_1)T_s$
$L_3 \frac{di_{L3}}{dt} = -v_{c3}$	$L_3 \frac{di_{L3}}{dt} = V_o - v_{c1}$	$L_3 \frac{di_{L3}}{dt} = V_o$
$L_3 = \left(\frac{V_{c3}}{\Delta I_{L3}} \right) \times d_2 T_s$	$L_3 = \left(\frac{V_o - v_{c1}}{\Delta I_{L3}} \right) \times (d_1 - d_2) T_s$	$L_3 = \left(\frac{V_o}{\Delta I_{L3}} \right) \times (1-d_1) T_s$

For the converter ratings mentioned in Table 2.5, the component values were computed, and their respective values are presented in Table-2.12.

Table 2. 12. Converter parameter expressions

Element	SCHBSTIC Topology-1 Parameters	Values
L_1	$\frac{(V_{g1} - 2V_{c1})(d_1 - d_2)}{\Delta i_{L1} f_s}$	$150 \mu H$
L_2	$\frac{V_{g2} d_2}{\Delta i_{L2} f_s}$	$530 \mu H$
L_3	$\frac{V_o(1 - d_1)}{\Delta i_{L3} f_s}$	$210 \mu H$
C_1, C_2	$\frac{V_o}{R \Delta v_{c1} f_s} \left(\frac{(1 - d_1)(d_1 - d_2)}{(2 - d_1 - 3d_2 + 2d_1 d_2)} \right)$	$33 \mu F$
C_3	$\frac{V_o}{R f_s \Delta v_{c3}} \left(\frac{2d_2(1 - d_1)}{(2 - d_1 - 3d_2 + 2d_1 d_2)} \right)$	$47 \mu F$
C_4	$\frac{V_o d_2}{R \Delta v_{c4} f_s} \left(\frac{1 - d_1}{(2 - d_1 - 3d_2 + 2d_1 d_2)} \right)$	$100 \mu F$

2.5 Quadratic Buck-SEPIC DC-DC Converter Topology

The SCHBSTIC Topology-1 converter, which was detailed above, has the ability to provide lower source and load ripple currents, and reduced component power losses. However, it has the disadvantage of being a higher order converter (7th order), which could make the process of synthesizing controllers laborious. So, a new converter was needed that could maintain the wide range of voltage conversion capabilities of buck-SEPIC converters and able to provide excessive bucking. The quadratic converter and SEPIC were combined to create the Quadratic Buck-SEPIC DC-DC converter (QBSTIC) which was a sixth order TIC. In this thesis, the trailing-edge synchronized switching signals are used to assess the QBSTIC performance for the $d_1 > d_2$ condition. The switching sequence and associated operating modes are provided in Tables 2.13 and 2.14, respectively.

Table 2.13. Modes of operation of QBSTIC

Mode	Devices-ON	Devices-OFF
Mode-1	S_1, S_2, D_2	D_1, D_3, D_4
Mode-2	S_1, D_2, D_4	S_2, D_1, D_3
Mode-3	D_1, D_3, D_4	S_1, S_2, D_2

Table 2.14. Operating modes of the proposed QBSTIC

Working Mode	Inductor Voltages (v_{L1}, v_{L2}, v_{L3})	Supplying source	ON State switch
Mode-I	$V_{g1} - v_{C1}$	V_{g1}	S_1
	V_{g2}	V_{g2}	S_2
	$V_{C1} + v_{C2}$		
Mode-II	$V_{g1} - v_{C1}$	V_{g1}	S_1
	$V_{g2} - v_{C2} - V_o$	V_{g2}	
	$v_{C1} - V_o$		
Mode-III	$-v_{C1}$		
	$V_{g2} - v_{C2} - V_o$	V_{g2}	
	$-V_o$		

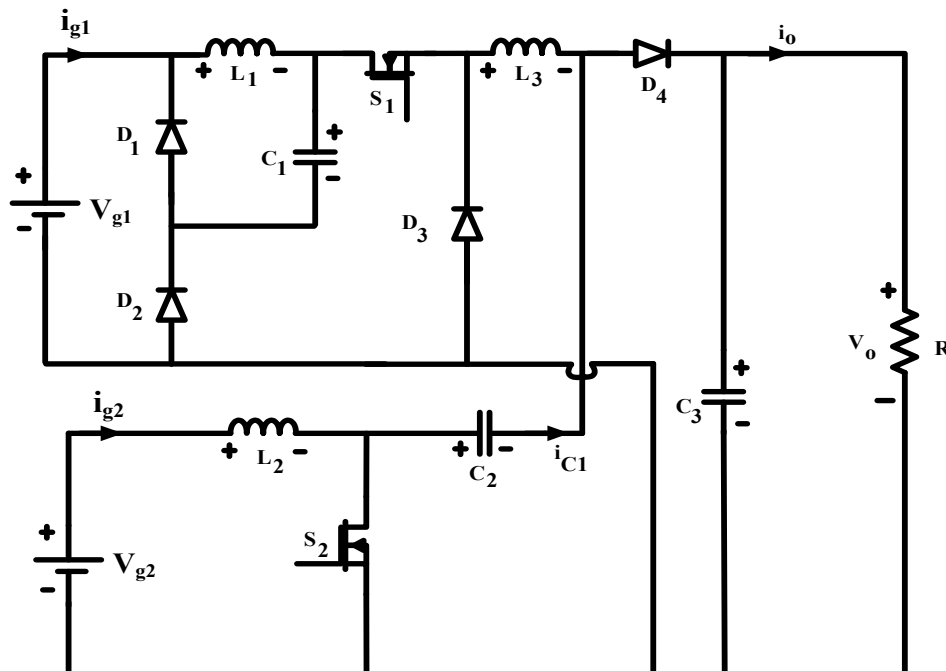


Fig. 2. 19. Circuit diagram of QBSTIC.

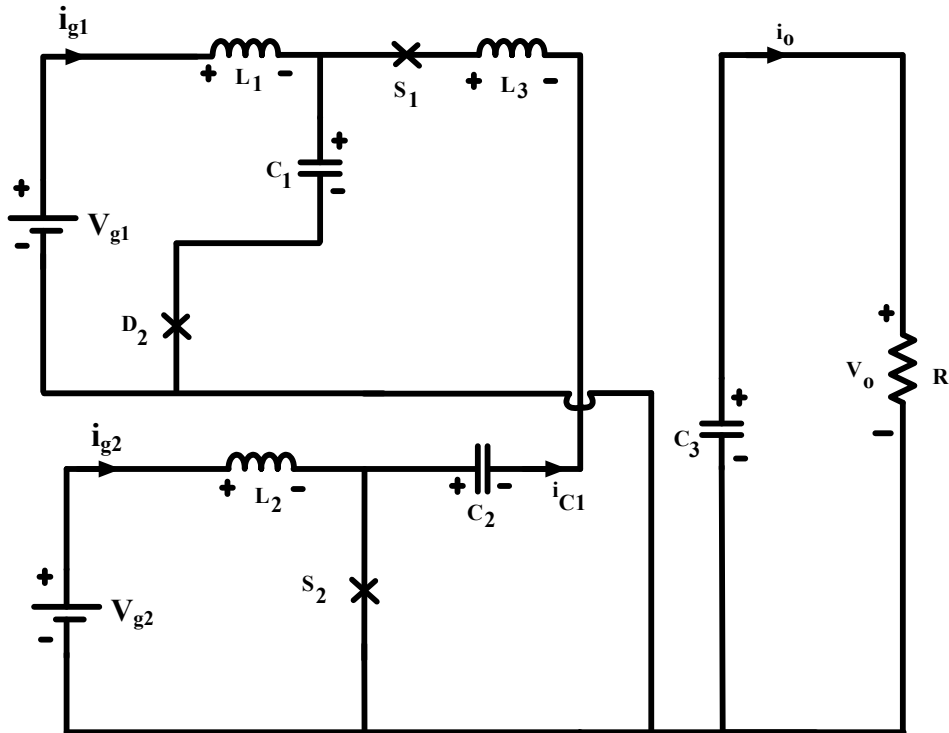


Fig. 2. 20 Equivalent circuit diagram for mode-1 operation.

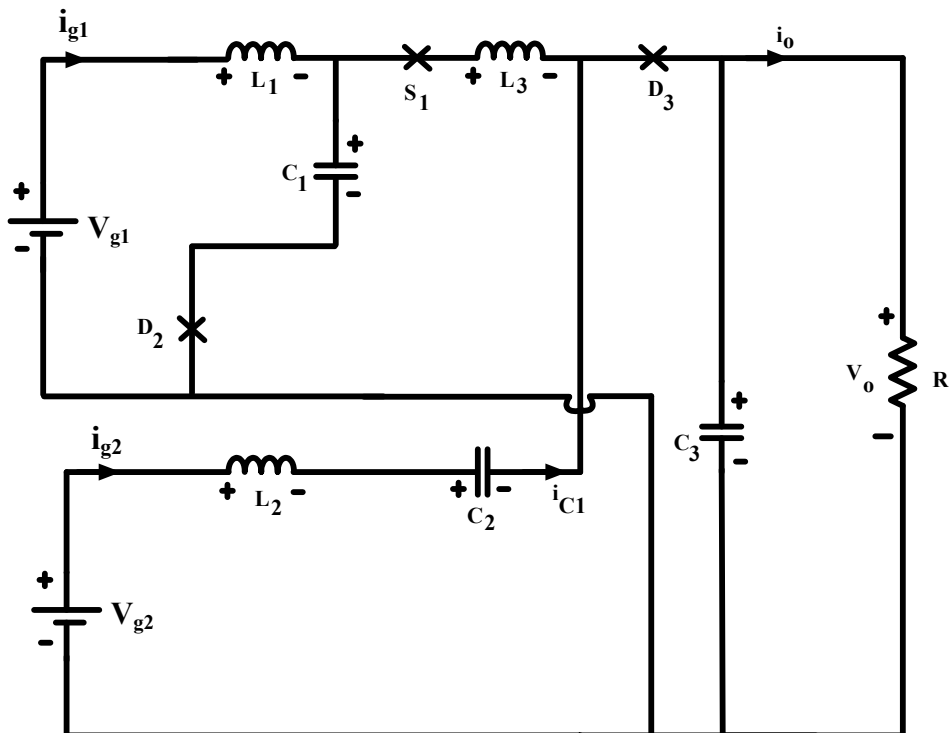


Fig. 2. 21 Equivalent circuit diagram for mode-2 operation.

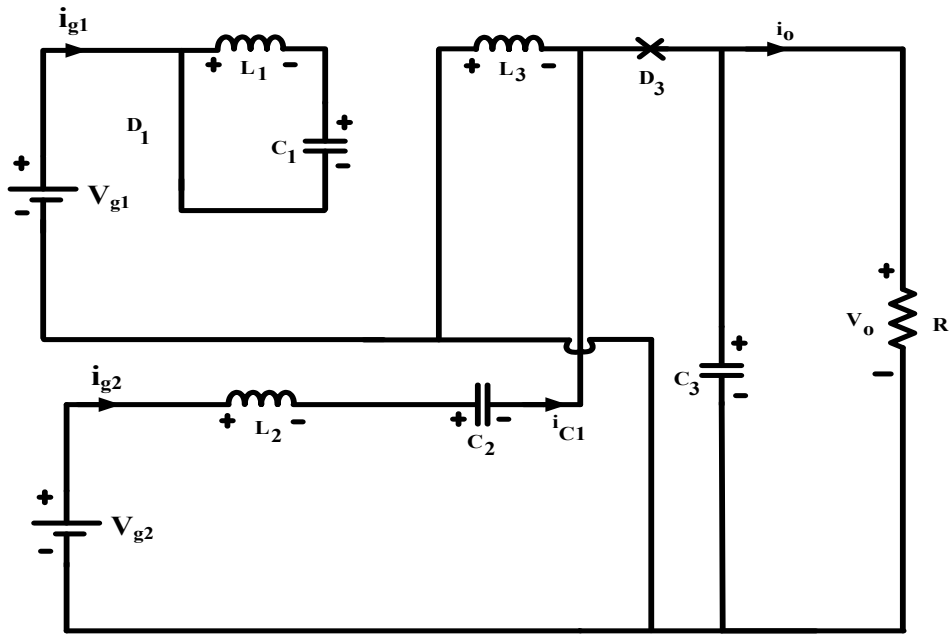


Fig. 2. 22. Equivalent circuit diagram for mode-3 operation.

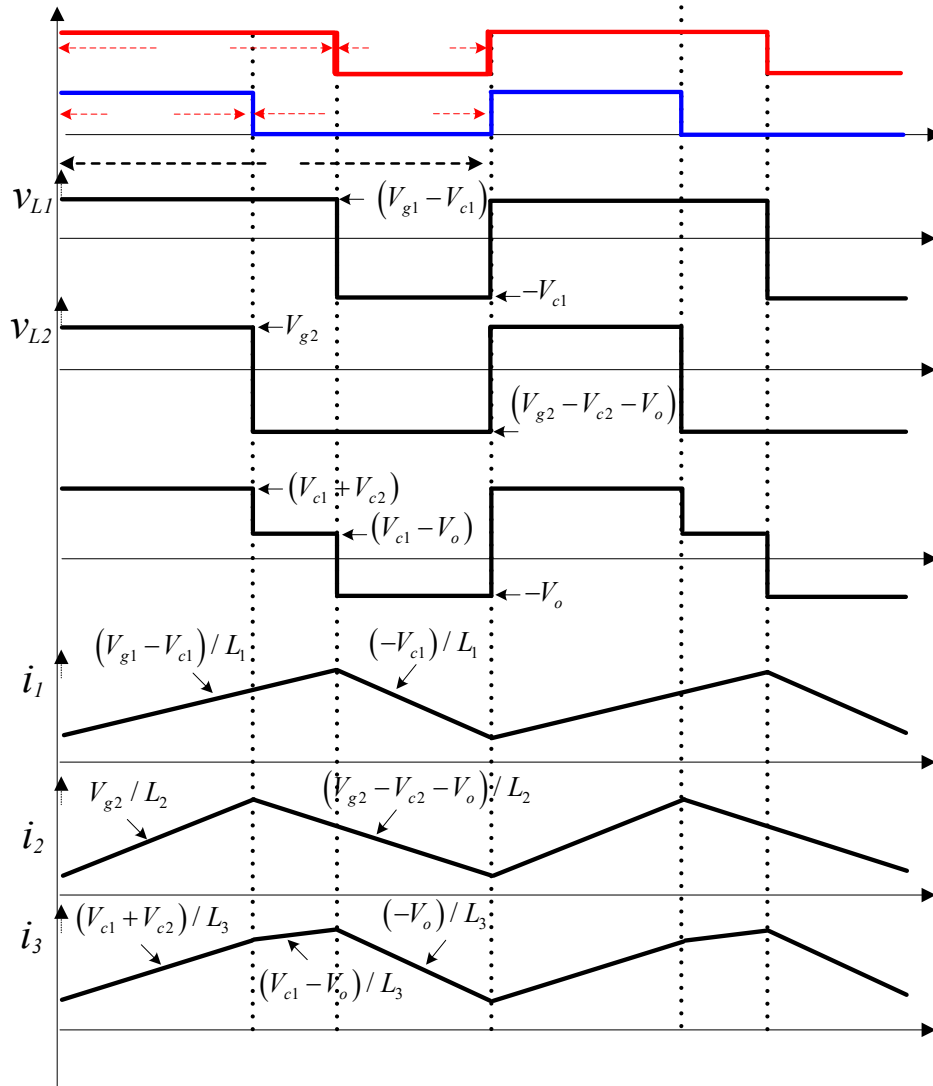


Fig. 2. 23. Key waveforms of QBSTIC.

The equivalent circuits for these operating modes are shown in Figs. 2.20, 2.21, 2.22, and the operating waveforms are shown in Fig. 2.23.

Considering the above three modes of operation and applying the volt-sec balance to inductors L_1 , L_2 , L_3 , the voltage conversion ratio of this converter is obtained as

$$V_o = V_{g1}d_1^2 + V_{g2} \frac{d_2}{(1-d_2)} \quad (2.6)$$

From the above equation, it is clear that the load voltage is controlled by the combination of switch duty ratios and also depends on both input dc sources voltage magnitudes.

The ripple-based design approach is used to design the elements of QBSTIC, which may be found in annexure-1. The design parameters for validation are listed in Table 2.18.

2.5.1 Design of QBSTIC Topology parameters

Inductor Design L_1 ,

Table 2.15. Voltage across inductor L_1 of QBSTIC

Mode – 1 for $D=d_2$	Mode – 2 for $D=d_1-d_2$	Mode – 3 for $D=1-d_1$
Voltage across inductor L_1 during d_2T_s	Voltage across inductor L_1 during $(d_1-d_2)T_s$	Voltage across inductor L_1 during $(1-d_1)T_s$
$L_1 \frac{di_{L1}}{dt} = V_{g1} - v_{c1}$	$L_1 \frac{di_{L1}}{dt} = V_{g1} - v_{c1}$	$L_1 \frac{di_{L1}}{dt} = -v_{c1}(1-d_1)T_s$
$L_1 = \left(\frac{V_{g1} - v_{c1}}{\Delta I_{L1} \times f_s} \right) d_2 T_s$	$L_1 = \left(\frac{V_{g1} - v_{c1}}{\Delta I_{L1} \times f_s} \right) d_2 T_s$	$L_1 = \frac{-v_{c1}(1-d_1)}{\Delta I_{L1} \times f_s}$

Inductor Design L_2

Table 2.16. Voltage across inductor L_2 of QBSTIC

Mode – 1 For $D=d_2$	Mode – 2 For $D=d_1-d_2$	Mode – 3 For $D=1-d_1$
Voltage across inductor L_2 during d_2T_s ,	Voltage across inductor L_2 during $(d_1-d_2) T_s$,	Voltage across inductor L_2 during $(1-d_1) T_s$,
$L_2 \frac{di_{L2}}{dt} = V_{g2}$	$L_2 \frac{di_{L2}}{dt} = V_{g2} - V_{c2} - V_o$	$L_2 \frac{di_{L2}}{dt} = V_{g2} - V_{c2} - V_o$
$L_2 = \left(\frac{V_{g2}}{\Delta I_{L2}} \right) \times d_2 T_s$	$L_2 = \frac{(V_{g2} - V_{c2} - V_{co})(d_1 - d_2)}{\Delta I_{L2} \times f}$	$L_2 = \frac{(V_{g2} - V_{c2} - V_o)(1 - d_1)}{\Delta I_{L2} \times f}$

Inductor Design L_3

Table 2.17. Voltage across inductor L_3 of QBSTIC

Mode – 1 For $D=d_2$	Mode – 2 For $D=d_1-d_2$	Mode – 3 For $D=1-d_1$
Voltage across inductor L_3 during d_2T_s , $L_3 \frac{di_{L3}}{dt} = (v_{C1} + v_{C2})$ $L_3 = \left(\frac{(v_{C1} + v_{C2})}{\Delta I_{L3}} \right) \times d_2 T_s$	Voltage across inductor L_3 during $(d_1-d_2) T_s$, $L_3 \frac{di_{L3}}{dt} = v_{C1} - V_o$ $L_3 = \left(\frac{v_{C1} - V_o}{\Delta I_{L3}} \right) \times (d_1 - d_2) T_s$	Voltage across inductor L_3 during $(1-d_1) T_s$, $L_3 \frac{di_{L3}}{dt} = V_o$ $L_3 = \left(\frac{V_o}{\Delta I_{L3}} \right) \times (1 - d_1) T_s$

For the converter rating mentioned in Table 2.5, the component values were evaluated, and their respective ratings are presented in and Table 2.18.

Table 2.18. Converter parameter expressions

Element	QBSTIC Parameters	Ratings
L_1	$L_1 \geq \frac{(V_{g1} - v_{c1})d_1}{\Delta i_{L1} f_s}$	190 μH
L_2	$L_2 \geq \frac{V_{g2}d_2}{\Delta i_{L2} f_s}$	150 μH
L_3	$L_3 \geq \frac{(v_{c1} + v_{c2})d_2}{\Delta i_{L3} f_s}$	135 μH
C_1	$C_1 \geq \frac{V_o d_1 (1 - d_2)}{R f_s \Delta v_{C1}}$	33 μF
C_2	$C_2 \geq \frac{V_o (1 - d_1)}{R f_s \Delta v_{C2}}$	220 μF
C_3	$C_3 \geq \frac{V_o d_2}{R f_s \Delta v_{C3}}$	100 μF

2.6 Switched Capacitor Hybrid Buck SEPIC Two-input DC-DC Converter

Topology-2

Fig. 2.24 shows the circuit diagram of the SCHBSTIC Topology-2, which has evolved from the SCHBSTIC Topology-1. This topology retains the benefit of low ripple content in both the source currents, as in the case of Topology-1. However, the main benefit of this converter is that both sources have a common ground. The equivalent circuit diagrams of each mode of the converter are shown in Figs. 2.25, 2.26 and 2.27, and the inductor voltages and currents are shown in Fig. 2.28. In mode-1, the source-1 is connected to load through L_1 . Source-2 charges L_3 and L_2 linearly by capacitor C_3 . In this mode, the capacitor C_1 and C_2 are floating. During mode-2, capacitor C_1 and C_2 comes in parallel to each other and are charged by source-1. V_{g2} comes in series with inductor L_2 and capacitor C_3 . In mode-3, capacitors C_1 and C_2 comes in series with source-1 and L_1 and discharges through the load.

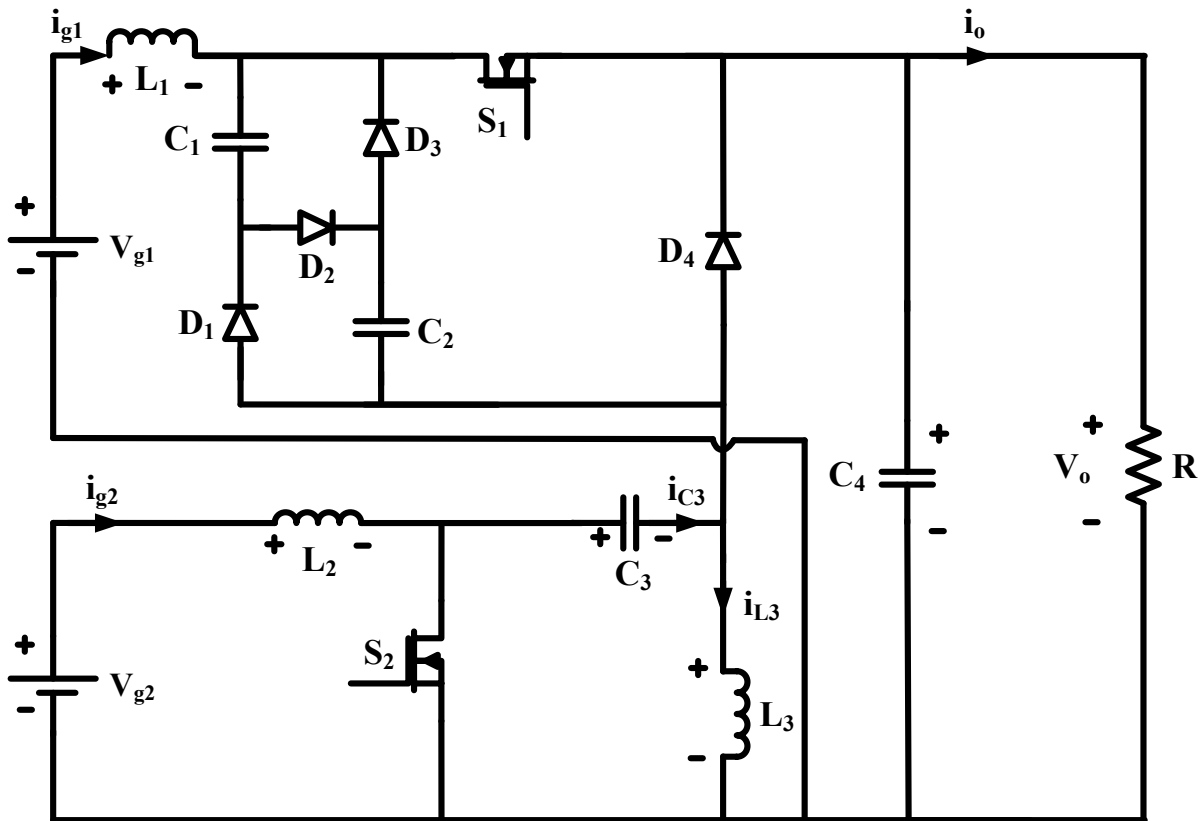


Fig. 2. 24 Circuit diagram of SCHBSTIC-2

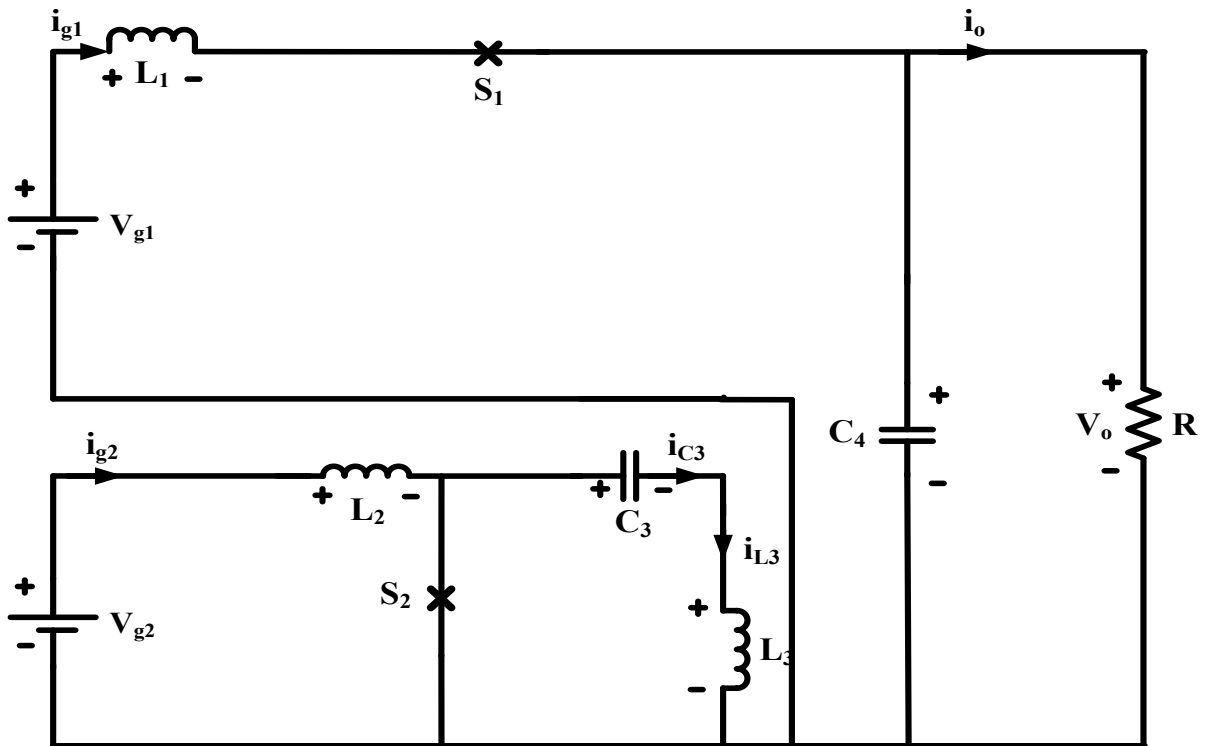


Fig. 2. 25 Equivalent circuit diagram for mode-1 operation.

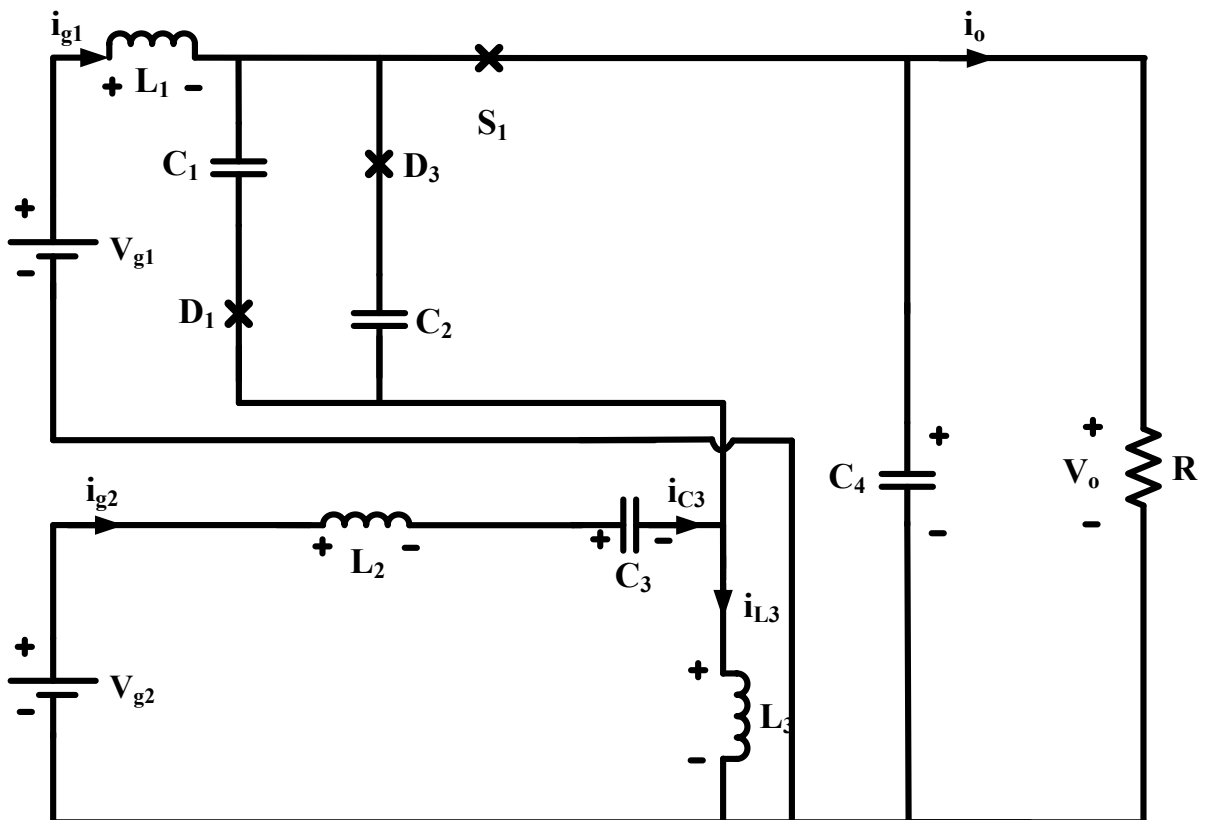


Fig. 2. 26. Equivalent circuit diagram for mode-2 operation.

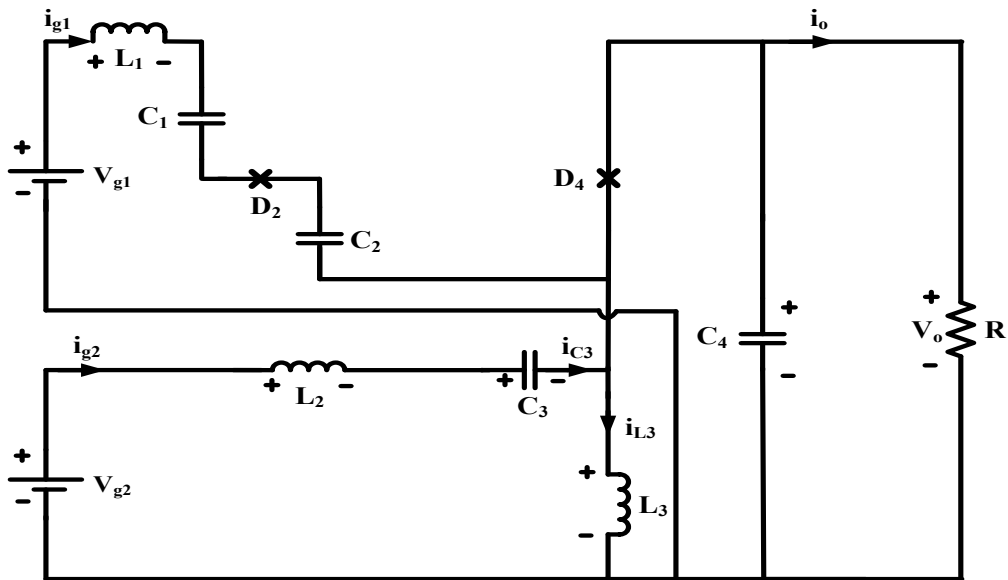


Fig. 2. 27. Equivalent circuit diagram for mode-3 operation.

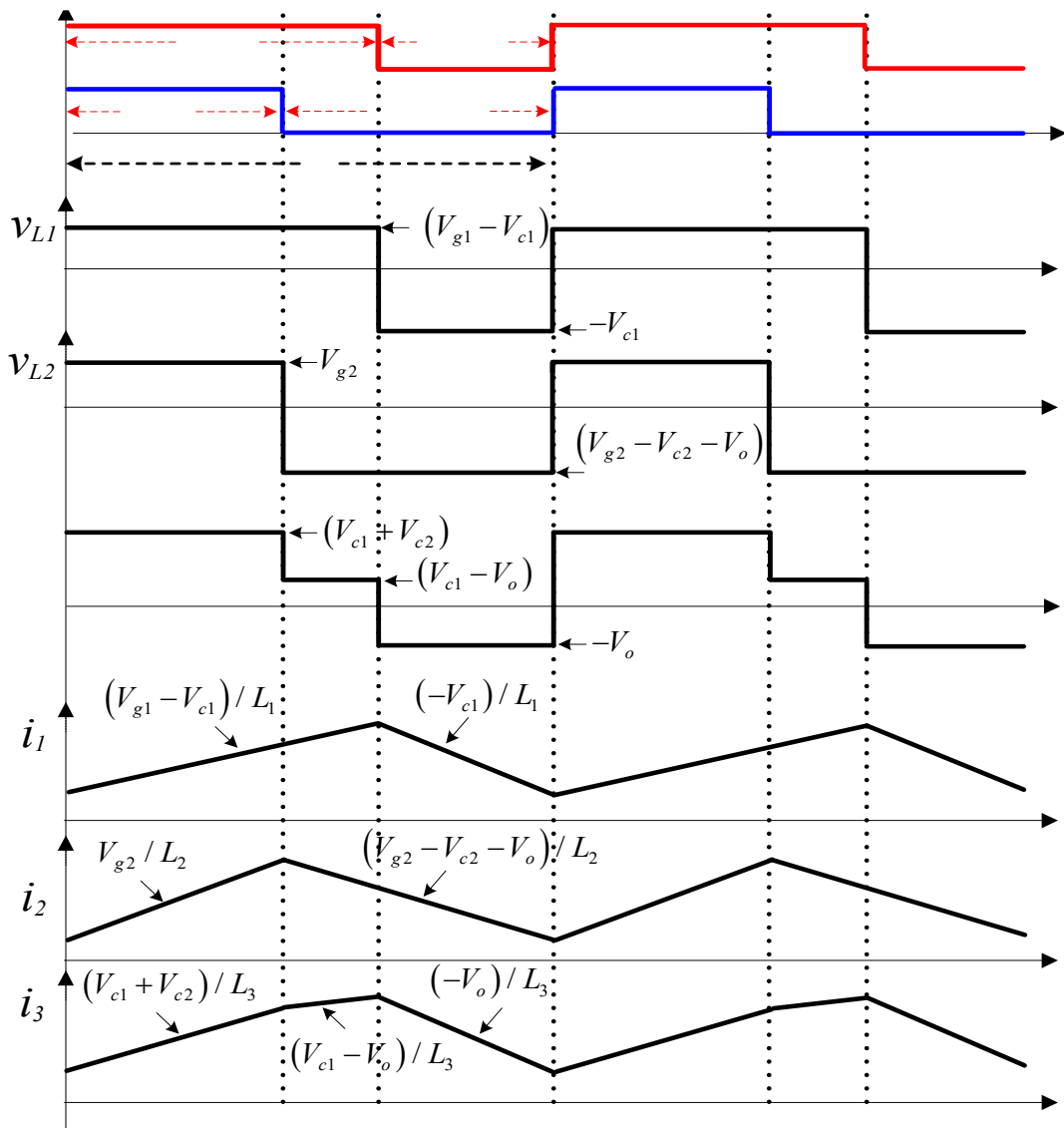


Fig. 2. 28. Key waveforms of Switched-Capacitor Topology-2.

Using the above equations, the voltage gain expression of the converter is obtained:

$$V_0 = V_{g1} \left[\frac{(d_1 - d_2)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right] + V_{g2} \left[\frac{2d_2(1 - d_1)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right] \quad (2.50)$$

Table 2.19. The voltage across each inductor of SCHBSTIC Topology-2

	Mode-1	Mode-2	Mode-3
v_{L1}	$(V_{g1} - V_0)$	$(V_{g1} - V_0)$	$(V_{g1} - 2v_{c1} - V_0)$
v_{L2}	V_{g2}	$(V_{g2} + v_{c1} - v_{c3} - V_0)$	$(V_{g2} - v_{c3} - V_0)$
v_{L3}	$(-v_{c3})$	$(V_0 - v_{c1})$	V_0

The voltage appearing across the inductors, L_1 , L_2 , and L_3 in each mode of the converter is given in Table 2.19. The steady-state expressions of the inductor currents, which are obtained by applying charge balance on capacitors C_1 , C_2 , C_3 , C_4 and capacitor voltages obtained by the volt-sec balance on inductors L_1 , L_2 and L_3 are given in Table 2.20.

Table 2.20. Steady-state expressions of SCHBSTIC Topology-2

Inductor currents	Capacitor voltages
$I_1 = \left[\frac{I_o(d_1 - d_2)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right]$	$V_{c1} = \frac{(V_{g1} - V_0)}{2(1 - d_1)}$
$I_2 = \left[\frac{I_o 2d_2(1 - d_1)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right]$	$V_{c2} = \frac{(V_{g1} - V_0)}{2(1 - d_1)}$
$I_3 = \left[\frac{2I_o(1 - d_1)(1 - d_2)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right]$	$V_{c3} = V_{g2}$
	$V_{c4} = V_o$

Table 2.21 gives the design equations for computing the values of the energy storage elements. The inductors are designed by considering the ripple current to be less than 20% of their average currents. The capacitors are designed by considering the ripple voltage to be less than 10% of

their respective average voltages. The values thus obtained by using these expressions are tabulated in Table 2.21.

Table 2.21. Design Expressions

Element	SCHBSTIC-2 Topology	Values
L_1	$L_1 \geq \left(\frac{(V_{g1} - 2V_{c1} - V_o)d_2}{\Delta i_{L1} f_s} \right)$	250 μH
L_2	$L_2 \geq \left(\frac{V_o(1-d_1)}{\Delta i_{L2} f_s} \right)$	450 μH
L_3	$L_3 \geq \left(\frac{V_o(1-d_1)}{\Delta i_{L3} f_s} \right)$	270 μH
C_1	$C_1 = C_2 \geq \left(\frac{I_{g1}(1-d_1)}{\Delta v_{c1} f_s} \right)$	33 μF
C_3	$C_3 \geq \left(\frac{I_{g2}(1-d_1)}{\Delta v_{c3} f_s} \right)$	33 μF
C_4	$C_4 \geq \left(\frac{(I_{L1} + I_{L2} - I_{L3} - I_o)(1-d_1)}{\Delta v_{c4} f_s} \right)$	100 μF

The state-space matrices were listed in Annexure – 1.

2.7 Results and Discussion

The steady-state time-domain analysis of all the TICs is performed to obtain the steady-state operating point expressions all the state variables which are inductor currents and capacitor voltages etc. shown in Table 2.22, followed by summarization of expressions for the energy storage elements in terms of their respective inductor ripple currents and capacitor ripples voltages in Table 2.23. Table 2.24 gives the mathematical expressions of the peak inductor currents, whereas voltages and current stresses of the switches and diodes for all the four topologies are listed in Table 2.25, and Table 2.28, and their respective RMS currents are listed

in Tables 2.29 and 2.30. Based upon these expressions, Table 2.26 compares the switch voltage and current stresses for identical load power (100 W) and source voltages V_{g1} (36 V) and V_{g2} (12 V) in all cases. Here, the switch voltages are normalized by taking nominal load voltage (24V) as base value whereas, the switch currents are normalized by taking load current (2.4 A) as the base value. The comparison chart is shown in Fig. 2.29. The table clearly illustrates that the voltage stress across switch S_1 is least for SCHBSTIC Topology-2 as compared to all other converters.

Similarly, the current stress of switch S_1 is minimum among all topologies. Even though the voltage stress of switch S_2 of SCHBSTIC Topology-2 is higher than BSTIC, SIHBSTIC and QBSTIC, it is still lower than SCHBSTIC Topology-1. The current stress of SCHBSTIC Topology-2 is lower than all topologies except SCHBSTIC Topology-1.

Table 2.22. Steady-state Inductor currents and capacitor Voltage Expressions of TICs

SIHBSTIC	SCHBSTIC-1	SCHBSTIC-2	QBSTIC
$I_{L_1} = I_o d_1$	$I_{L_1} = I_o H_1$	$I_{L_1} = I_o a_{sc2}$	$I_{L_1} = I_o d_1$
$I_{L_2} = I_o b_{si}$	$I_{L_2} = I_o H_2$	$I_{L_2} = I_o b_{sc2}$	$I_{L_2} = I_o b_{sq}$
---	$I_{L_3} = I_o$	$I_{L_3} = I_o (1 - a_{sc2})$	---
$V_{C_2} = \left(\frac{V_{g_2}}{1 - d_2} - V_o \right)$	$V_{C_1} = \left(\frac{V_{g_1}}{1 - d_1} - V_o \right)$	$V_{C_1} = \left(\frac{V_{g_1}}{1 - d_1} - V_o \right)$	$V_{C_1} = V_{g_1} d_1$
$V_{C_2} = V_o$	$V_{C_2} = \left(\frac{V_{g_1}}{1 - d_1} - V_o \right)$	$V_{C_2} = \left(\frac{V_{g_1}}{1 - d_1} - V_o \right)$	$V_{C_2} = \left(\frac{V_{g_2}}{1 - d_2} - V_o \right)$
---	$v_{C_3} = V_{g_2}$	$v_{C_3} = V_{g_2}$	$v_{C_3} = V_o$
---	$V_{C_4} = V_o$	$V_{C_4} = V_o$	---

Table 2.23 Design equations of TIC Topologies.

	SIHBSTIC	SCHBSTIC-1	SCHBSTIC-2	QBSTIC
Δi_{L1}	$\frac{L_1=L_2}{V_o(1-d_1)}$ $L_1 f_s$	$\frac{(V_{g1}-2V_{C1})(1-d_1)}{L_1 f_s}$	$\frac{(V_{g1}-V_o)d_1}{L_1 f_s}$	$\frac{(V_{g1}-V_o)d_2}{L_1 f_s}$
Δi_{L2}	$\frac{V_{g2}d_2}{L_2 f_s}$	$\frac{V_o(1-d_1)}{L_2 f_s}$	$\frac{V_o(1-d_1)}{L_2 f_s}$	$\frac{V_{g2}d_2}{L_2 f_s}$
Δi_{L3}	---	$\frac{V_o(1-d_1)}{L_3 f_s}$	$\frac{V_o(1-d_1)}{L_2 f_s}$	$\frac{V_o(1-d_1)}{L_3 f_s}$
Δv_{C1}	$\frac{V_o d_2^2}{C_1 R f_s K_{Si2}}$	$\frac{V_o H_1(1-d_1)}{C_1 R f_s}$	$\frac{V_o a_{sc2}(1-d_1)}{R f_s C_1}$	$\frac{V_o d_1(1-d_2)}{R f_s C_1}$
Δv_{C2}	$\frac{V_o Q_{Si}(1-d_1)}{R C_2 f_s}$	$\frac{V_o H_1(1-d_1)}{C_1 R f_s}$	$\frac{V_o a_{sc2}(1-d_1)}{R f_s C_2}$	$\frac{V_o b_{sq}(1-d_1)}{R f_s C_2}$
Δv_{C3}		$\frac{V_o H_2(1-d_1)}{C_2 R f_s}$	$\frac{V_o b_{sc2}(1-d_2)}{R f_s C_3}$	$\frac{V_o d_2}{R f C_3}$
Δv_{co}	---	$\frac{V_o(2-b_{sc1})(1-d_2)}{C_o R f_s}$	$\frac{V_o b_{sc2}(1-d_2)}{R f_s C_4}$	---

Table 2.24. Peak Value of Inductor current Expressions of TICs

SIHBSTIC	SCHBSTIC-1	SCHBSTIC-2	QBSTIC
$i_{L_1} = I_o d_1 \pm \frac{V_o(1-d_1)}{L_1 f_s}$	$i_{L_1} = I_o H_1 \pm \frac{(V_{g1} - V_o)(d_1 - d_2)}{L_1 f_s}$	$i_{L_1} = I_o a_{sc2} \pm \frac{(V_{g1} - V_o) d_1}{L_1 f_s}$	$i_{L_1} = I_o d_1 \pm \frac{(V_{g1} - V_o) d_2}{L_1 f_s}$
$i_{L_2} = I_o b_{si} \pm \frac{V_{g2} d_2}{L_2 f_s}$	$i_{L_2} = I_o H_2 \pm \frac{V_o(1-d_1)}{L_2 f_s}$	$i_{L_2} = I_o b_{sc2} \pm \frac{V_o(1-d_1)}{L_2 f_s}$	$i_{L_2} = I_o b_{sq} \pm \frac{V_{g2} d_2}{L_2 f_s}$
---	$i_{L_3} = I_o \pm \frac{V_o(1-d_1)}{L_3 f_s}$	$i_{L_3} = I_o(1-a_{sc2}) \pm \frac{V_o(1-d_1)}{L_2 f_s}$	---

Table 2.25. Comparison of Voltage and Current Stresses of Switches

	SIHBSTIC	SCHBSTIC-1	SCHBSTIC-2	QBSTIC
v_{s1}	$V_o(1+a_{si})$	$2K_{sc1}$	$2\left(\frac{V_{g1} - V_o}{1-d_1}\right)$	$V_{g1}(1+d_1)$
i_{s1}	$I_o a_{si}$	$I_o H_1$	$I_o \left(\frac{2-d_2-d_2}{d_{sc2}}\right)$	$I_o d_1$
v_{s2}	$\frac{V_{g2}}{(1-d_2)}$	$V_{g2} + V_o$	$V_o + V_{g2}$	$\frac{V_{g2}}{(1-d_2)}$
i_{s2}	$i_{L1 peak} + i_{L2 peak}$	$I_o H_2$	$I_o(1-(b_{sc2} + a_{sc2}))$	$I_o(1+b_{sq})$

Table 2.26. Normalized voltage and current stresses of switches

	SIHBSTIC	QBSTIC	SCHBSTIC-1	SCHBSTIC-2
i_{s1}	0.5461	1	0.6041	1.17525
i_{s2}	0.6935	1.4492	0.2525	0.62007
v_{s1}	2.6121	2.6851	2.1997	2.3473
v_{s2}	0.7142	0.724638	1.5161	1.5077

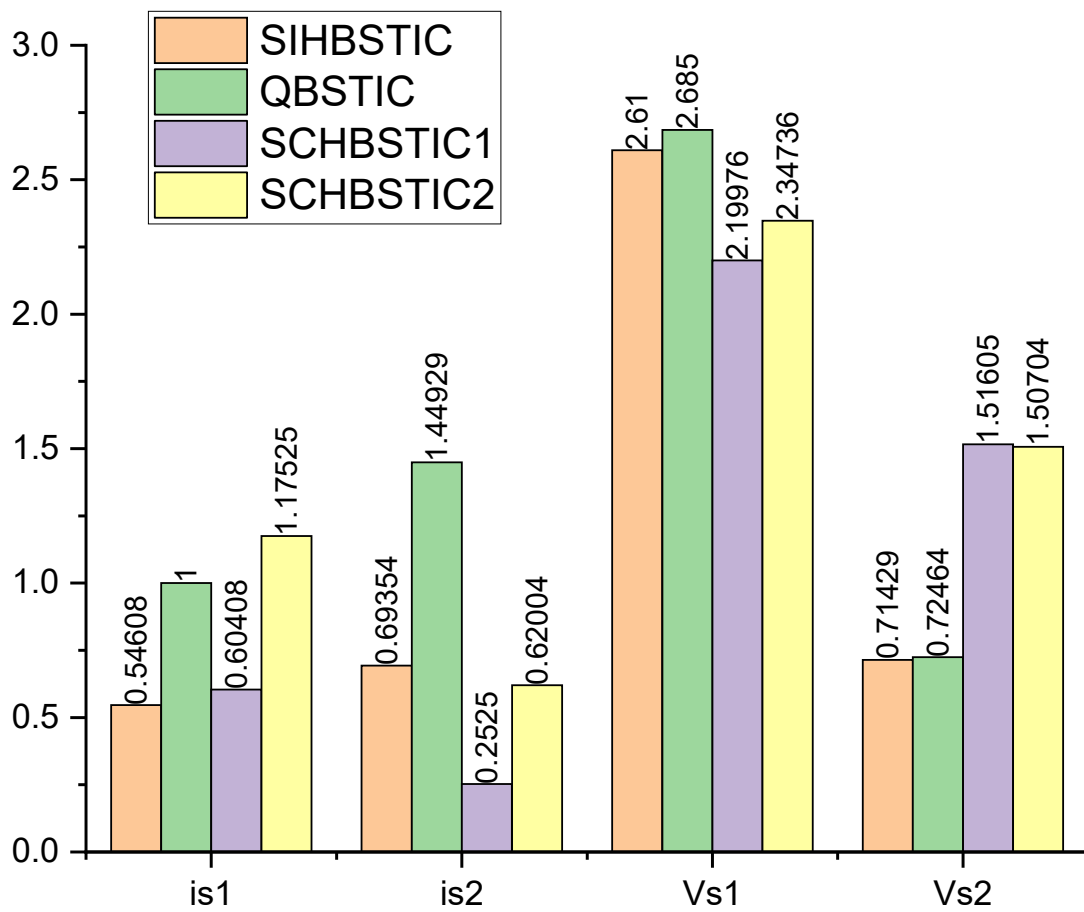


Fig. 2.29 Normalized voltage and current stresses of switches.

Table 2.27. Qualitative comparison of converters normalized voltages and currents

	SIHBSTIC	QBSTIC	SCHBSTIC-1	SCHBSTIC-2
i_{s1}	Very Low	high	low	Very high
i_{s2}	low	high	Very low	low
v_{s1}	high	Very high	Very low	low
v_{s2}	low	low	Very high	high

Table 2.28. Peak Current Stresses of Diodes

	SIHBSTIC	SCHBSTIC-1	SCHBSTIC-2	QBSTIC
i_{D1}	$I_o g_{si}$	$i_{L1 peak}$	$i_{L2 peak} - i_{L3 peak}$	$i_{L1 peak}$
i_{D2}	$I_o g_{si}$	$i_{L1 peak}$	$i_{L1 peak}$	$i_{L1 peak} - i_{L3 peak}$
i_{D3}		$i_{L1 peak}$	$i_{L2 peak} - i_{L3 peak}$	I_o
i_{DO}	$I_o(2a_{si} + b_{si})$	$i_{L2 peak} - i_{L3 peak}$	$I_o(1 - (b_{sc2} + a_{sc2}))$	$i_{L2 peak} + i_{L3 peak}$

Table 2.29. RMS Switch Currents

	SIHBSTIC	SCHBSTIC-1	SCHBSTIC-2	QBSTIC
i_{s1}	$I_o a_{si} \sqrt{d_1}$	$I_o \sqrt{H_1^2 d_2 + H_3^2 (d_1 - d_2)}$	$I_o \sqrt{\left(\frac{2 - d_1 - d_2}{d_{sc2}}\right)^2 (d_1 - d_2) + a_{sc2}^2 d_2}$	$I_o \sqrt{d_1}$
i_{s2}	$I_o \sqrt{(b_{si} + g_{si}) d_2}$	$I_o H_2 \sqrt{d_2}$	$I_o \left(\frac{d_1 + d_2 - 2d_1 d_2}{d_{sc2}}\right) \sqrt{d_2}$	$I_o e_{sq} \sqrt{d_2}$

Table 2.30. RMS Diode Current

	SIHBSTIC	SCHBSTIC-1	SCHBSTIC-2	QBSTIC
i_{D1}	$I_o g_{si} \sqrt{(1-d_1)}$	$2K_{SC1}$	$2 \left(\frac{V_{g1} - V_o}{1-d_1} \right)$	$V_{g1}(1+d_1)$
i_{D2}	$I_o g_{si} \sqrt{(1-d_1)}$	$2K_{SC1}$	$2 \left(\frac{V_{g1} - V_o}{1-d_1} \right)$	$V_{g1}(1+d_1)$
i_{D3}		$I_o H_2$	$I_o (1 - (b_{sc2} + a_{sc2}))$	$I_o (1 + b_{sq})$
i_{DO}	$I_o \sqrt{(4a_{si}^2 + b_{si}^2)(1-d_2)}$	$I_o H_2$	$I_o (1 - (b_{sc2} + a_{sc2}))$	$I_o (1 + b_{sq})$

On comparing the device stresses of Hybrid TICs with BSTIC, the voltage and current stresses of SIHBSTIC and QBSTIC are little more, where as that of SCHBSTIC Topology-1 are less except the voltage stress of switch ‘S₂’, this is because SCHBSTIC Topology-1 is an integrated TIC, the voltage of the intermediate isolation capacitor of the SEPIC converter is varying minimally, the discharging operation in mode-1 and the combined voltage of source-2 and inductor getting applied across it in the remaining two modes are the factors leading to the high voltage stress across S₂. Similarly, the presence of an LC circuit in QBSTIC is responsible for high current stress as they are forming a local discharge loop in mode-3 followed by discharging the capacitor through inductor L3 for mode-1,2 is responsible for the more current stress, which also flows through switch S₂ in the second half of converter leading to more voltage stress in S₂.

Voltage Gain Expression:

The output voltage equations of all the TICs are derived in the previous sections and are summarized in Table 2.27. For identical input voltages of V_{g1}=36V, V_{g2}=12V, the duty ratios are

varied such that always the condition $d_1 > d_2$ is met at all points of operation. The waveforms of output voltages are plotted on the same graph to make a comparison, shown in Fig. 2.29. (The Red dotted indicates the desired voltage of 24V at the output for all TICs).

Table 2.31 Output Voltage Expressions of TICs

BSTIC	SCHBSTIC-1	SIHBSTIC	QBSTIC	SCHBSTIC-2
$V_o = V_{g1}d_1 + V_{g2} \frac{d_2}{1-d_2}$	$V_o = \frac{\left(V_{g1}(d_1-d_2) + V_{g2}2d_2(1-d_1) \right)}{2-d_1-3d_2+2d_1d_2}$	$V_o = V_{g1} \frac{d_1}{2-d_1} + V_{g2} \frac{d_2}{(2-d_1)(1-d_2)}$	$V_o = V_{g1}d_1^2 + V_{g2} \frac{d_2}{1-d_2}$	$V_o = \frac{\left(V_{g1}(d_1-d_2) + V_{g2}2d_2(1-d_1) \right)}{2(1-d_1)(1-d_2) + (d_1-d_2)}$

To generate a voltage of say 24V, TIBSC for identical source voltages, needs to be operated at the duty ratio of $d_1=0.5$, $d_2=0.4$, in order to attain the same voltage, Hybrid Two-input converters (HTICs) are supposed to be operated at around $d_1=0.8$, $d_2=0.3$, so HTICs are to be operated at higher duty ratios to attain the same voltage, which may also be interpreted that they are capable of providing excessive bucking at nominal duty ratios. The two-dimensional plot of the output voltage for a fixed low duty ratio of $d_1=0.5$, $d_2=0.2$, is shown in Fig. 2.31, the point mentioned above is validated. Observing the plots of Figs. 2.30 and 2.31, it can be presumed that the hybrid Buck-SEPIC derived topologies providing approximately 50% to 60% lesser voltage compared to BSTIC, this is an advantage concerning bucking. However, on the other hand, the order of the Hybrid TICs is more, which indirectly points to higher dynamics and may also pose difficulties while designing the controllers.

On similar lines, for input voltages of $V_{g1}=36V$, $V_{g2}=12V$, the duty ratios are varied to observe the variation of source-1 and source-2 currents with duty ratios d_1 , d_2 are shown in Figs. 2.32 and 2.33.

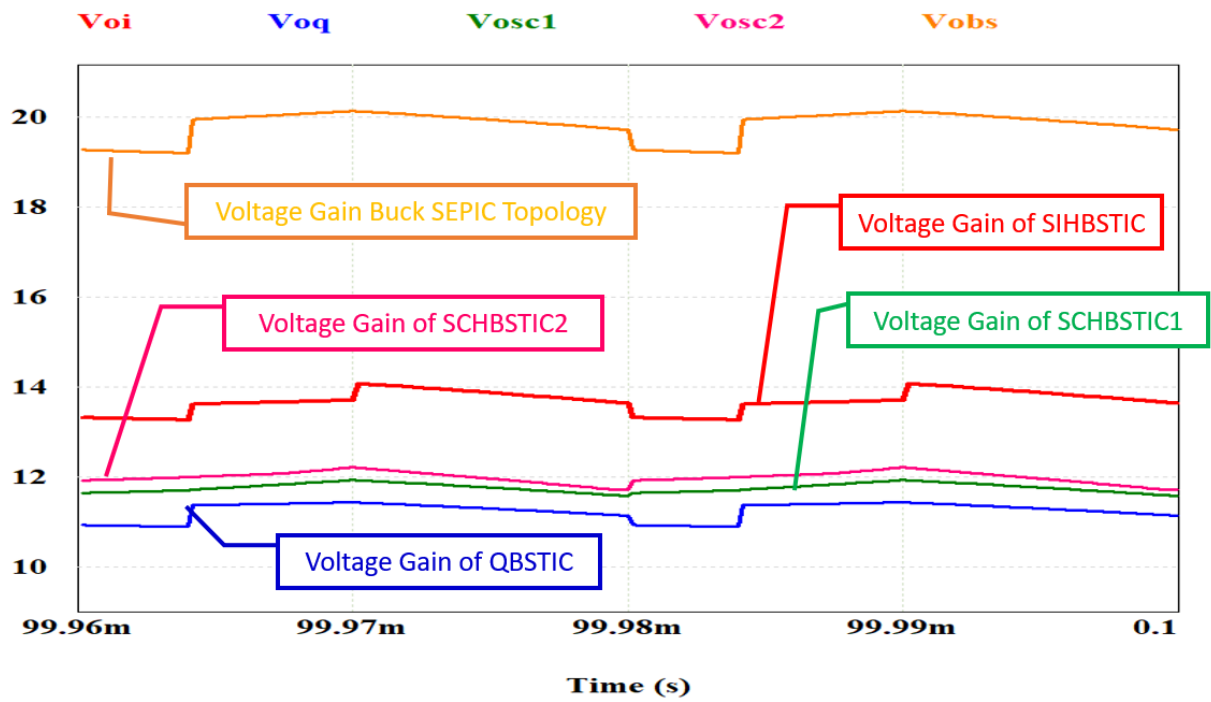


Fig. 2.30. The output voltage at lower duty ratios $d_1 = 0.5$, $d_2 = 0.2$.

Where the $V_{o(x)}$ where $x=i$ for SIHBSTIC, q-QBSTIC, sc1-SCHBSTIC-1, sc2-SCHBSTIC2

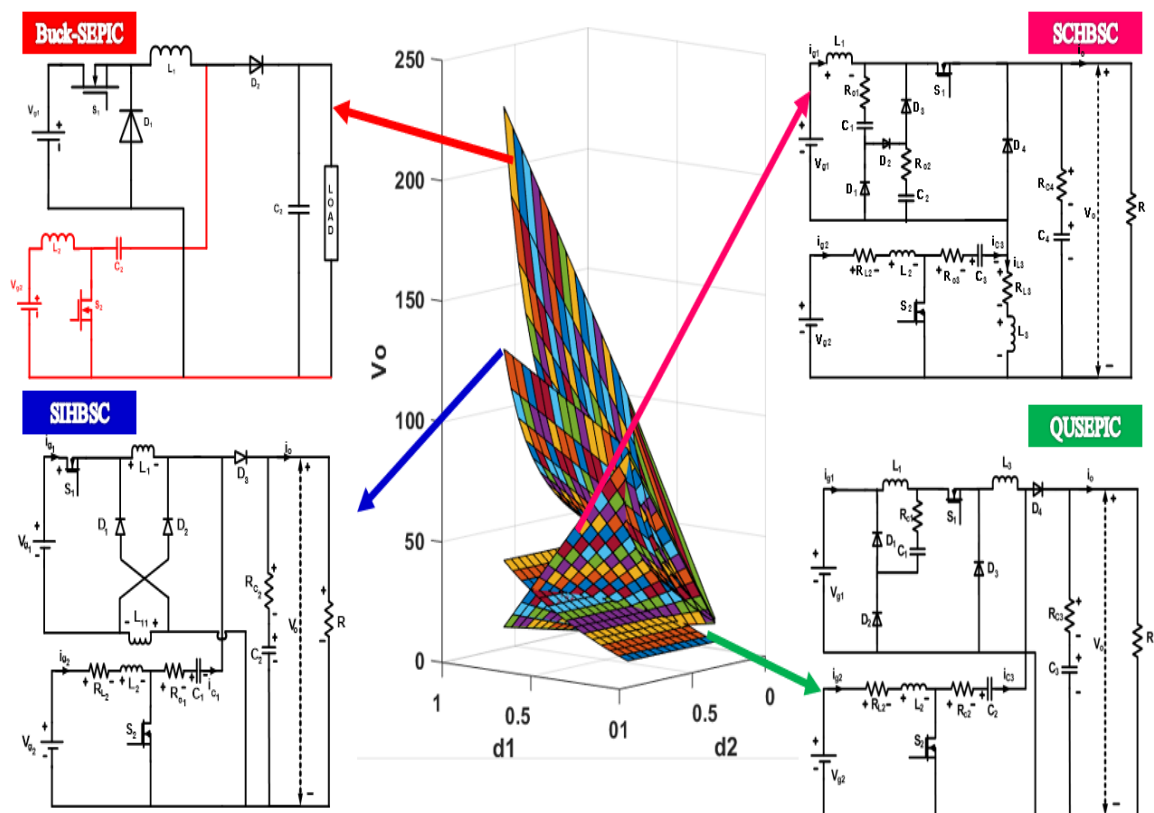


Fig. 2.31 The output voltage variation of TICs with duty ratios d_1 , d_2 .

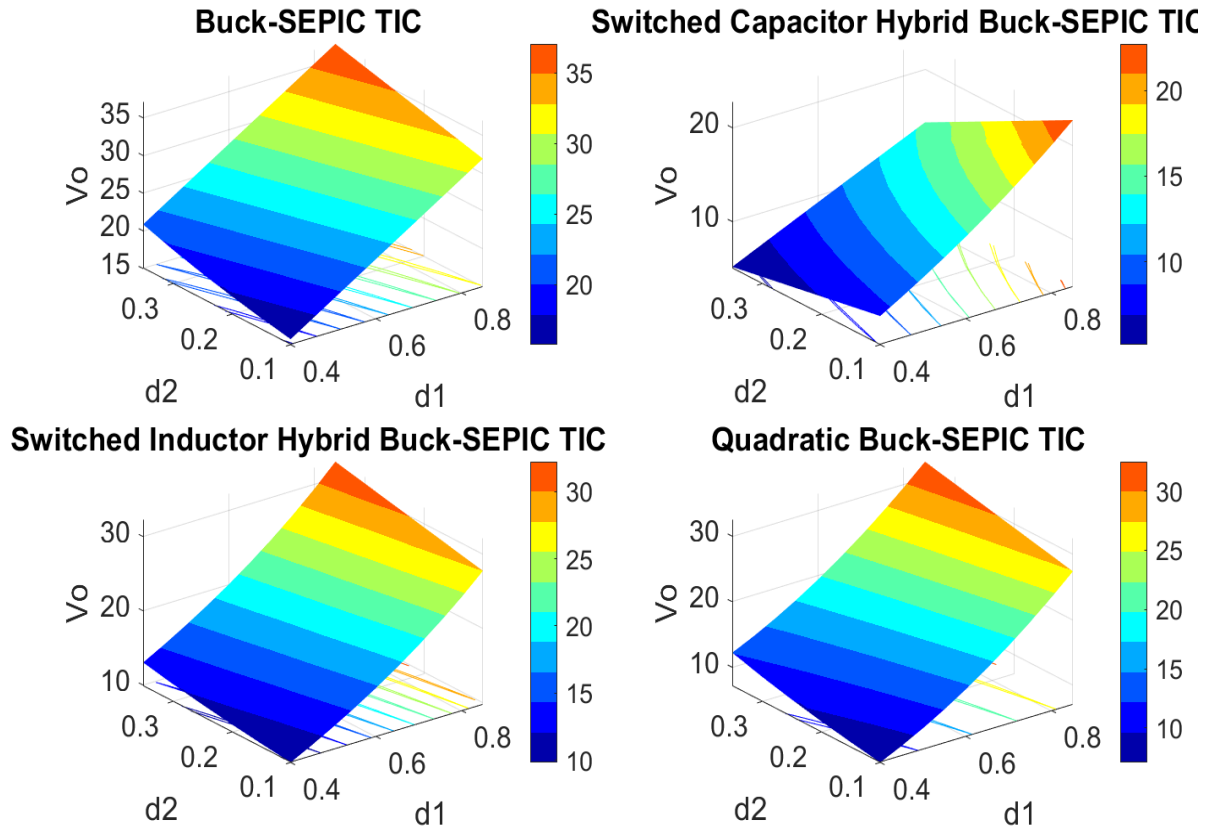


Fig. 2.32 The output voltage variation of TICs with duty ratios d_1 (0.4 to 0.9), d_2 (0.1 to 0.35) for the condition $d_1 > d_2$

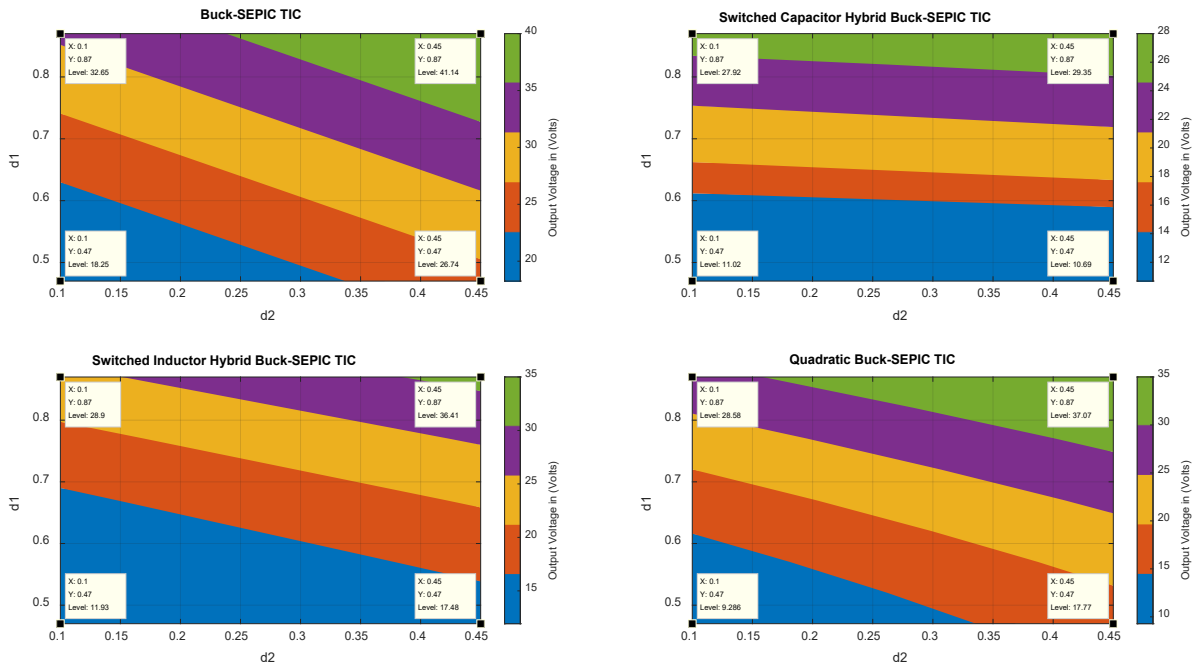


Fig. 2.33 2-d plots of Variation of Output Voltage with respect to duty ratios d_1 , d_2 .

The percentage peak ripple in the inductor currents and output capacitor voltage is plotted in Fig. 2.34. The average values of the load voltage and load currents of TICs are taken as base values, and for plotting the graph, all are found to be within acceptable limits. These graphs are plotted to trace the effect of the difference in duty ratio variation on source currents. The shorter the difference in duty ratio, which means longer is the period of power storage in inductor-2 and quicker is the discharge, results in a higher source-2 current. It can be seen that the ripple current of SCHBSTIC2 is a little bit higher compared to other TICs because it is continually supplying the current to the load in all modes, which is not the case with other TICs. Similar effects of variations are seen in output power for constant source voltages, as shown in Figs. 2.35 to 2.36.

Table 2.32 Output Voltage Expressions of TICs

Ripple	SIHBSTIC	QBSTIC	SCHBSTIC1	SCHBSTIC2
Inductor-1 $diL1(\Delta)$	14.0521	14.2133	11.4953	15.5743
Inductor-2 $diL2(\Delta)$	4.42917	7.04167	7.91667	9.4001
Capacitor $dVco(\Delta)$	1.99259	1.5002	1.3251	1.6875

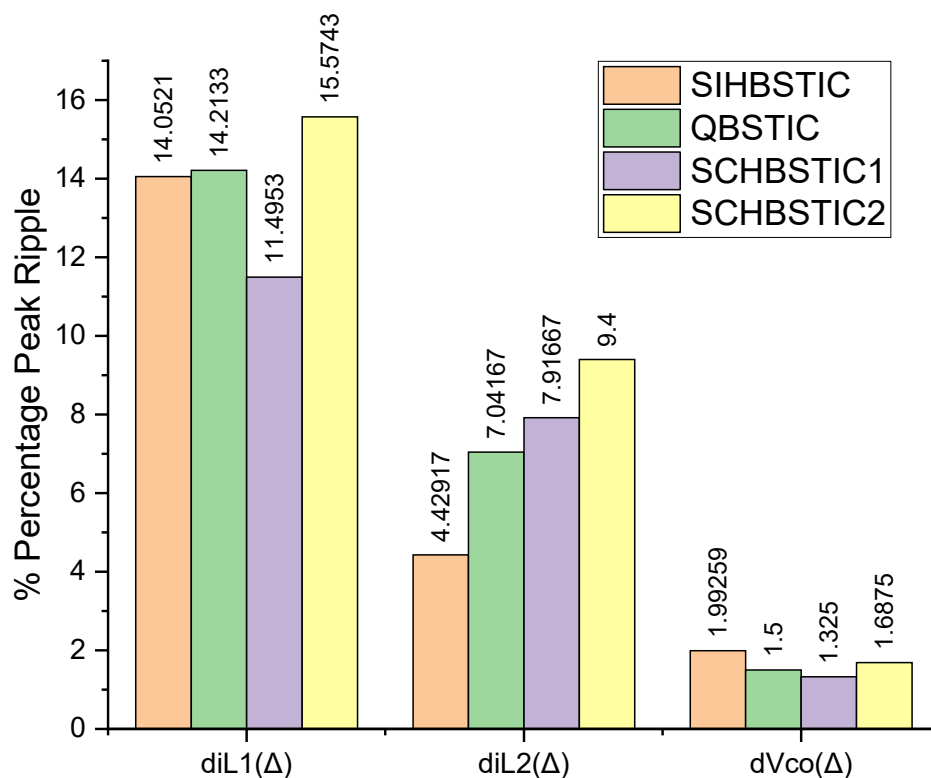


Fig. 2.34 The peak percentage ripple of inductor currents and output capacitor voltage.

Table 2.33 Percentage Power Losses of Components in TICs

	SIHBSTIC	QBSTIC	SCHBSTIC1	SCHBSTIC2
Efficiency	90.2481	88.1411	90.2	90.34
Output Power P_{output} (Watts)	61.53	61.34	59.4641	60.014
Total Loss (Watts)	6.1479	8.27	6.01	6.4295

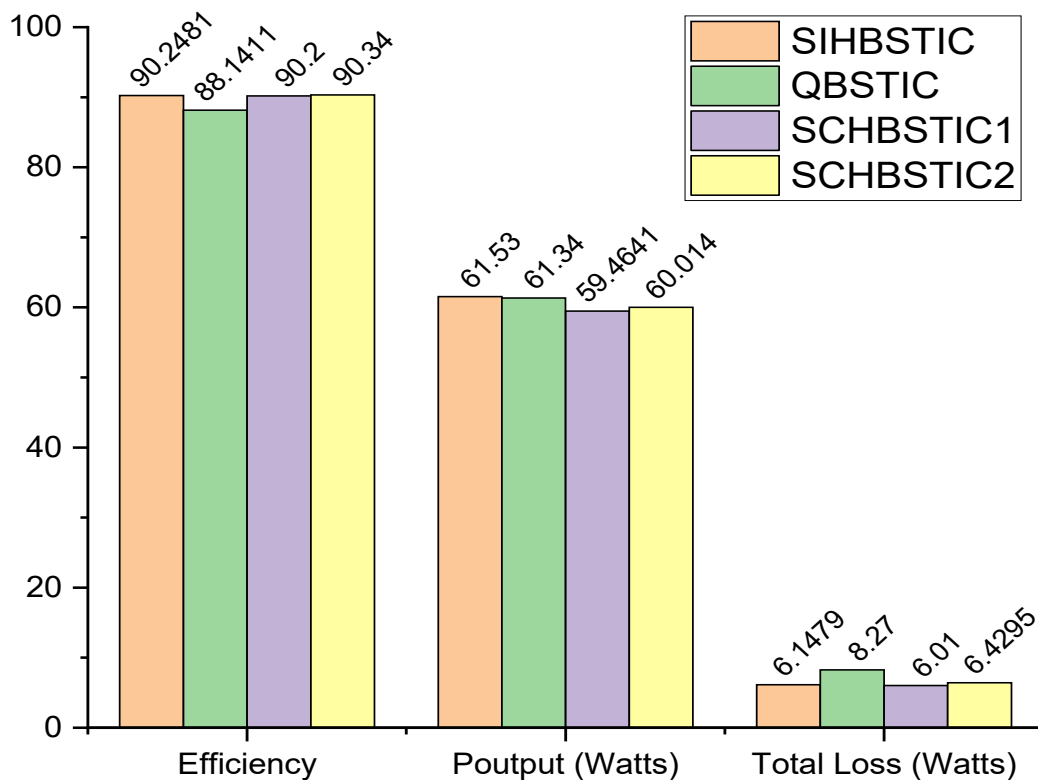


Fig. 2.35 Efficiency, Output Power, and Losses in TICs

The TICs efficiency is found to vary between 88% and 90%. The output power and losses are shown in Fig. 2.35. The graph shown in Fig. 2.36 depicts the power loss distribution across the switch, diode, inductor, and capacitors. The diode losses were found to be around 50%, while the inductor losses in SIHBSTIC are about 22%, which is high in comparison to other TICs, and the capacitor losses are found to be high, about 27% in SCHBSTIC 1, 2, as it comprises four capacitors. The switching losses are about 10% to 14% across different TICs.

Table 2.34 Percentage Power Losses of Components in TICs

Power Losses of Components	SIHBSTIC	QBSTIC	SCHBSTIC1	SCHBSTIC2
PLswitch	14.03	10.19	15.15	12.13
PLDiode	47.94	51.34	49.65	50.2
PLinductor	22.12	13.16	7.44	10.6
PLCapacitor	15.9	19.33	27.72	27.07

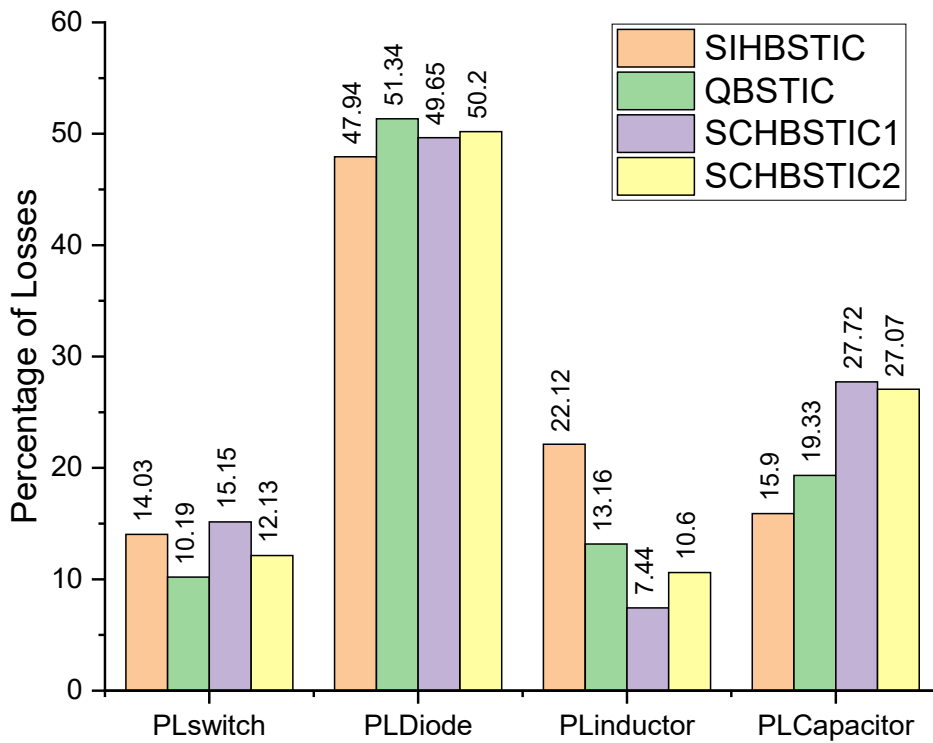


Fig. 2.36 Percentage Power Losses of TICs.

2.8 Summary

The mathematical modeling aspects of the proposed TIC topologies were discussed, and state-space models were formulated. The steady-state voltage gain in the case of all the hybrid converters was derived and presented. The hybrid TICs have evolved based on the existing Buck-SEPIC TIC. The operating principle, design of energy storage elements, and state-space matrices were derived for each TIC. A comparison among all TICs was performed by taking the voltage and current stresses of the switches into account. Further, it was seen that the switched capacitor-based topologies (SCHBSTIC-1 and SCHBSTIC-2) have better source current ripple performance compared to other topologies, and the comparison of power loss distribution and efficiencies of TICs was tabulated, and respective graphs were plotted.

CHAPTER - 3

3. MODELING OF TWO-INPUT DC-DC CONVERTERS

3.1 Introduction

This chapter aims at outlining the variables influencing the dynamical behavior of the DC-DC TICs working with and without a control loop. Examining the dynamic behavior of the switched-mode dc-dc converters is an essential requirement to develop a steady and high-performance closed-loop converter system [38]. The growing interest in practical digital control for high-frequency DC-DC converters has led to an increase in interest in discrete-time analysis and modeling of DC-DC converters to facilitate direct digital compensator design ([39], [22]). The earlier modeling methods explained how the converter state and the control variable behaved at a specific point in the switching period. Consequently, these types of methods aren't appropriate for A/D converters that are digitally controlled. Therefore, to overcome this, discrete-time modeling is employed for modeling the converter [40]. The discrete-time model considers sampling, measured impacts, and inborn delays in the digital control loop. Switch-mode DC-DC converters are discrete, and time-varying systems. Cyclic changes in power stage topologies describe the activity of these switching circuits. Each cycle can be separated into a few intervals relying on the state of the switches (either 'ON' or 'OFF') and the inductor current. Regardless, every one of these circuits is spoken to by many state conditions utilizing state-space techniques. Modeling of these converters is generally done using methods for the state-space averaging procedure. In spite of the fact that state-space averaging has a helpful continuous, time-invariant structure and has been applied effectively in numerous applications, however, it has a few constraints and disadvantages, as referenced underneath [24].

The model accuracy deteriorates rapidly as the frequency of interest approaching one half of the fundamental switching frequency of the converter.

1. The average model predicts high gain and less phase delay at higher frequencies.
2. The effect of a delay from a perturbation in the ON time interval to the subsequent perturbation of the OFF-time interval will prompt an extra high-frequency pole, which the regular state-space average model cannot foresee.

Stability can be analyzed if one realizes how a disturbance propagates through the controller and power stage to influence 'd', 'Vo'. In essence, this implies finding the suitable transfer functions which relate input voltage to power stage to yield output voltage, despite the fact that the power stage is switched and becomes non-linear when control loop is closed [41].

3.2 State-space analysis of Two-input DC-DC Converters

Utilizing KVL and KCL, the accompanying first-order differential equations are established in detail for all L-C components to obtain all inductor currents and capacitor voltages. Study and analysis of higher-order differential equations is a complex task and hence, all the inductor and capacitor voltages must be transformed into a set of first-order differential equations. In that case, all the network equations of each mode of operation can easily be represented in the state-space model. To study the dynamic behavior of HBSTIC, all three different state-space models are to be considered for analysis. However, analyzing each mode with the corresponding state-space model and extending it in sequence to all modes of the switching cycle is a tedious task. Hence to get rid of this complexity, the state-space averaging method is widely adopted [42], [43]. This method of averaging is found to be an immensely helpful tool for obtaining the average values of state variables in steady-state as well as for analysis of the dynamical variation of state variables [44], [45]. To attain a linearized state-space equation, small-signal AC perturbations are superposed in the duty ratios, voltages, and currents [44]. The state-space model of the system can be represented as:

$$\begin{aligned}\dot{X} &= [A]X + [B]U + [M]i_o \\ Y &= [E]X + [F]U + [J]i_o\end{aligned}\quad (3.1)$$

The steady-state solution (X_{ss}) is obtained by using:

$$\begin{aligned}X_{ss} &= -A^{-1}BU, \\ U &= \begin{bmatrix} V_{g1} \\ V_{g2} \end{bmatrix}\end{aligned}\quad (3.2)$$

where ' X_{ss} ' is the state vector containing all inductor currents and capacitor voltages.

State-space average model equations for the TICs are:

$$A = A_1d_1 + A_2(d_2 - d_1) + A_3(1 - d_2) = (A_1 - A_2)d_1 + (A_2 - A_3)d_2 + A_3 \quad (3.3)$$

$$B = B_1d_1 + B_2(d_2 - d_1) + B_3(1 - d_2) = (B_1 - B_2)d_1 + (B_2 - B_3)d_2 + B_3 \quad (3.4)$$

$$E = E_1d_1 + E_2(d_2 - d_1) + E_3(1 - d_2) = (E_1 - E_2)d_1 + (E_2 - E_3)d_2 + E_3 \quad (3.5)$$

$$P = P_1d_1 + P_2(d_2 - d_1) + P_3(1 - d_2) = (P_1 - P_2)d_1 + (P_2 - P_3)d_2 + P_3 \quad (3.6)$$

$$P = P_1d_1 + P_2(d_2 - d_1) + P_3(1 - d_2) = (P_1 - P_2)d_1 + (P_2 - P_3)d_2 + P_3 \quad (3.7)$$

$$P = P_1d_1 + P_2(d_2 - d_1) + P_3(1 - d_2) = (P_1 - P_2)d_1 + (P_2 - P_3)d_2 + P_3 \quad (3.8)$$

where A_i , B_i , C_i , D_i are the state-space matrices corresponding to i^{th} mode. The small-signal continuous-time model is obtained by perturbing [46] the control, line and load parameters

$$d_1 = (D_1 + \hat{d}_1), \quad d_2 = (D_2 + \hat{d}_2), \quad v_g = (V_g + \hat{v}_g), \quad v_o = (V_o + \hat{v}_o), \quad i_o = (I_o + \hat{i}_o).$$

3.3 The Small-signal Transfer Functions

The circuit operation depends on the type of controlling signal used for switching devices S_1 and S_2 . Two duty ratios need to be controlled, one for current control and the second for load voltage regulation. To design suitable controllers, firstly the converter transfer functions are to be formulated. These formulations are obtained after linearization of the converter system around

the operating point. Once these small-signal transfer functions are known, linear control systems theory is extended for closed-loop system stability analysis. In the following lines, the small-signal linearization of two-input converters and their transfer function formulations are explained. The state-space representation of the converter system is

$$\dot{X} = AX + BU \quad (3.9)$$

$$\dot{X} = [(A_1 - A_2)d_1 + (A_2 - A_3)d_2 + A_3]X + [(B_1 - B_2)d_1 + (B_2 - B_3)d_2 + B_3]U \quad (3.10)$$

Including small-signal perturbations and then linearizing gives

$$\begin{aligned} \dot{X} + \dot{\hat{x}} &= ((A_1 - A_2)(d_1 + \hat{d}_1) + (A_2 - A_3)(d_2 + \hat{d}_2) + A_3)(X + \hat{x}) + \\ & ((B_1 - B_2)(d_1 + \hat{d}_1) + (B_2 - B_3)(d_2 + \hat{d}_2) + B_3)(U + \hat{u}) \\ \dot{\hat{x}} &= A\hat{x} + B\hat{u} + [(A_1 - A_2)\hat{d}_1 + (A_2 - A_3)\hat{d}_2]X + [(B_1 - B_2)\hat{d}_1 + (B_2 - B_3)\hat{d}_2]U \end{aligned} \quad (3.11)$$

Applying Laplace transform results in

$$(sI - A)\hat{x}(s) = B\hat{u}(s) + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}_1(s) + [(A_2 - A_3)X + (B_2 - B_3)U]\hat{d}_2(s) \quad (3.12)$$

By substituting $\hat{d}_2(s) = 0, \hat{u}(s) = 0$ in eq. (3.11)

$$\left. \frac{\hat{x}(s)}{\hat{d}_1(s)} \right|_{\hat{d}_2(s)=0, \hat{u}(s)=0} = [sI - A]^{-1} [(A_1 - A_2)X + (B_1 - B_2)U] \quad (3.13)$$

By substituting $\hat{d}_1(s) = 0, \hat{u}(s) = 0$ in eq. (3.11)

$$\left. \frac{\hat{x}(s)}{\hat{d}_2(s)} \right|_{\hat{d}_1(s)=0, \hat{u}(s)=0} = [sI - A]^{-1} [(A_2 - A_3)X + (B_2 - B_3)U] \quad (3.14)$$

By substituting $\hat{d}_1(s) = 0, \hat{d}_2(s) = 0$ in eq. (3.11)

$$\left. \frac{\hat{x}(s)}{\hat{u}(s)} \right|_{\hat{d}_2(s)=0, \hat{d}_1(s)=0} = [sI - A]^{-1} B \quad (3.15)$$

The output equation is given by

$$Y = EX \quad (3.16)$$

$$Y = [(E_1 - E_2)d_1 + (E_2 - E_3)d_2 + E_3]X \quad (3.17)$$

Including perturbations and then linearizing the output equation gives

$$Y + \hat{y} = [(E_1 - E_2)(d_1 + \hat{d}_1) + (E_2 - E_3)(d_2 + \hat{d}_2) + E_3](X + \hat{x}) \quad (3.18)$$

$$\hat{y} = E\hat{x} + [(E_1 - E_2)\hat{d}_1 + (E_2 - E_3)\hat{d}_2]X \quad (3.19)$$

Applying the Laplace transform results in

$$\hat{V}_o(s) = E\hat{x}(s) + [(E_1 - E_2)X\hat{d}_1(s) + (E_2 - E_3)X\hat{d}_2(s)] \quad (3.20)$$

By substituting eq. (3.12) in eq. (3.20) and assuming $\hat{d}_2(s) = 0$

$$G_{11} = \frac{\hat{V}_o(s)}{\hat{d}_1(s)} = E\{[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)U]\} + [(E_1 - E_2)X] \quad (3.21)$$

By substituting eq. (3.12) in eq. (3.20) and assuming $\hat{d}_1(s) = 0$

$$G_{12} = \frac{\hat{V}_o(s)}{\hat{d}_2(s)} = E\{[sI - A]^{-1}[(A_2 - A_3)X + (B_2 - B_3)U]\} + [(E_2 - E_3)X] \quad (3.22)$$

$$\frac{\hat{x}(s)}{\hat{u}(s)} = E\{[sI - A]^{-1}B\} \quad (3.23)$$

The input current equation is given by

$$I_{in} = PX \quad (3.24)$$

$$I_{in} = [(P_1 - P_2)d_1 + (P_2 - P_3)d_2 + P_3]X \quad (3.25)$$

Including perturbations in the input source current and then linearizing gives

$$I_{in} + \hat{i}_{in} = [(P_1 - P_2)(d_1 + \hat{d}_1) + (P_2 - P_3)(d_2 + \hat{d}_2) + P_3][X + \hat{x}] \quad (3.26)$$

$$\hat{i}_{in} = P\hat{x} + [(P_1 - P_2)X]\hat{d}_1 + [(P_2 - P_3)X]\hat{d}_2 \quad (3.27)$$

Applying Laplace Transform results in

$$\hat{i}_m(s) = P\hat{x}(s) + [(P_1 - P_2)X]\hat{d}_1(s) + [(P_2 - P_3)X]\hat{d}_2(s) \quad (3.28)$$

By substituting eq. (3.13) in (3.28) and assuming $\hat{d}_2(s) = 0$

$$G_{21} = \frac{\hat{i}_m(s)}{\hat{d}_1(s)} = P\{[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)U]\} + [(P_1 - P_2)X] \quad (3.29)$$

By substituting eq. (3.12) in (3.28) and assuming $\hat{d}_1(s) = 0$

$$G_{22} = \frac{\hat{i}_m(s)}{\hat{d}_2(s)} = P\{[sI - A]^{-1}[(A_2 - A_3)X + (B_2 - B_3)U]\} + [(P_2 - P_3)X] \quad (3.30)$$

From all the above equations (eq. (3.21), (3.22) and (3.29), (3.30)), the two-input converter system is represented by the following matrix equation. This equation is formulated assuming the converter load voltage and one of the inductors current to be regulated.

$$\begin{bmatrix} V_o \\ I_{in} \end{bmatrix} = \begin{bmatrix} G_{11}(s) & G_{12}(s) \\ G_{21}(s) & G_{22}(s) \end{bmatrix} \begin{bmatrix} \hat{d}_1(s) \\ \hat{d}_2(s) \end{bmatrix} \quad (3.31)$$

Expressing the above s-domain matrix equation in the z-domain,

$$\begin{bmatrix} V_o \\ I_{in} \end{bmatrix} = \begin{bmatrix} G_{11}(z) & G_{12}(z) \\ G_{21}(z) & G_{22}(z) \end{bmatrix} \begin{bmatrix} \hat{d}_1(z) \\ \hat{d}_2(z) \end{bmatrix} \quad (3.32)$$

Including all the small-signal perturbations in the state-space model equations

$$\begin{aligned} \dot{X} &= AX + BU + MI_z \\ Y &= EX + FU + JI_z \\ I_{in} &= PX \end{aligned} \quad (3.33)$$

By considering initially all set of perturbations $d_1 = (D_1 + \hat{d}_1)$, $d_2 = (D_2 + \hat{d}_2)$, $v_g = (V_g + \hat{v}_g)$,

$u = (U + \hat{u})$, $i_{in} = (I_{in} + \hat{i}_{in})$, $i_z = (I_z + \hat{i}_z)$ and linearizing average model around a steady-state

operating point [46], the following eq.s are obtained.

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + B\hat{u} + M\hat{i}_z + \hat{d}_1[(A_2 - A_3)X_{ss} + (B_2 - B_3)U + (M_2 - M_3)I_z] \\ &\quad + \hat{d}_2[(A_1 - A_2)X_{ss} + (B_1 - B_2)U + (M_1 - M_2)I_z] \end{aligned} \quad (3.34)$$

$$\hat{v}_o = E\hat{x} + F\hat{v}_g + J\hat{i}_z + \hat{d}_1[(E_2 - E_3)X_{ss} + (F_2 - F_3)V_g + (J_2 - J_3)I_z] + \hat{d}_2[(E_1 - E_2)X_{ss} + (F_1 - F_2)U + (J_1 - J_2)I_z] \quad (3.35)$$

$$\hat{i}_m(s) = P\hat{x}(s) + \hat{d}_1(s)[(P_2 - P_3)X] + [(P_1 - P_2)X]\hat{d}_2(s) \quad (3.36)$$

Various small-signal transfer functions that describe the dynamical behavior of converter can be derived from eq. s 3.34, 3.35, 3.36.

3.4 Discrete-Time Model Formulations

An exact small-signal discrete-time model for digitally controlled dc-dc converters, which is based on well-known approaches to discrete-time modeling and the standard Z-transform, takes into account sampling, modulator effects, and delays in the control loop. Such models can be used for any leading or trailing edge PWM converter operating in continuous conduction mode and with a single A/D sampling instant per switching period. The models can be used directly in software tools such as MATLAB for system analysis [39] and direct digital compensator design. In each state of the switch (1 or 2), the converter circuit is linear, time-invariant, with the corresponding state-space description.

$$\hat{x} = A_i x + B_i V_g \quad (3.37)$$

$$y = E_i x + D_i V_g \quad (3.38)$$

Where $i=1, 2$; 'x' is the vector of converter states (e.g., inductor current and capacitor voltage).

We assume the input voltage is constant since the primary interest is in the control-to output responses.

The small-signal discrete-time model can be written as,

$$\hat{x}[n] = \phi\hat{x}[n-1] + \gamma\hat{d}[n-1] \quad (3.39)$$

The output state-space equation can be written as follows:

$$\hat{y}[n] = E_i \hat{x}[n] \quad (3.40)$$

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + [(A_1 - A_2)\hat{d}_1 + (A_2 - A_3)\hat{d}_2]X + [(B_1 - B_2)\hat{d}_1 + (B_2 - B_3)\hat{d}_2] \quad (3.41)$$

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + K_1\hat{d}_1 + K_2\hat{d}_2 \quad (3.42)$$

where

$$\begin{aligned} K_1 &= (A_1 - A_2)X + (B_1 - B_2)U \\ K_2 &= (A_2 - A_3)X + (B_2 - B_3)U \end{aligned} \quad (3.43)$$

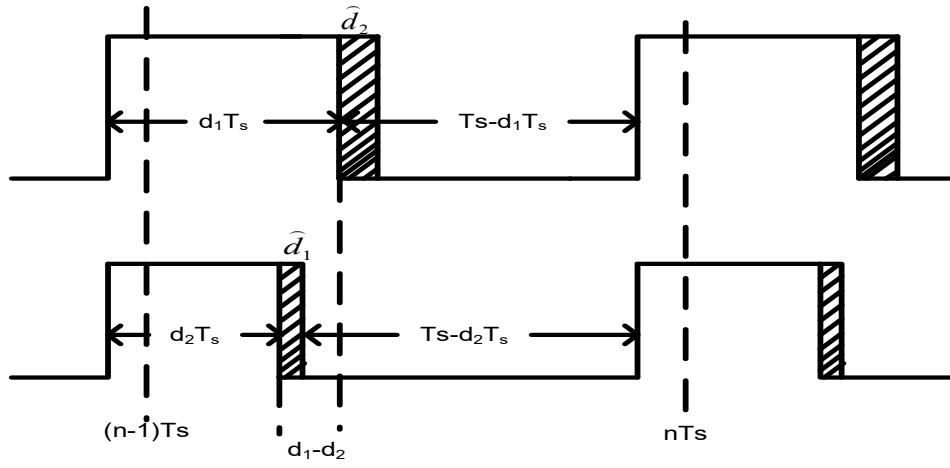


Fig. 3. 1 PWM for $d_1 > d_2$ sequence.

$$\dot{\hat{x}} = [A_1 d_1 + A_2(d_2 - d_1) + A_3(1 - d_2)]\hat{x} + [B_1 d_1 + B_2(d_2 - d_1) + B_3(1 - d_2)]\hat{u} + K_1\hat{d}_1 + K_2\hat{d}_2 \quad (3.44)$$

From $(n-1)T_s$ to $(n-1)T_s + t_d$

$$\dot{\hat{x}} = A_1 \hat{x} \quad (3.45)$$

Applying Laplace transform

$$\hat{x}(s) = \frac{\hat{x}(0)}{(sI - A_1)} \quad (3.46)$$

Applying inverse Laplace transform

$$\hat{x}(t) = e^{A_t} \hat{x}(0) \quad (3.47)$$

$$\hat{x}(t - t_o) = e^{A(t-t_o)} \hat{x}(t_o) \quad (3.48)$$

From $t_o = (n-1)T_s$;

$$\hat{x}[(n-1)T_s + t_d] = e^{A t_d} \hat{x}[(n-1)T_s] \quad (3.49)$$

From $(n-1)T_s + t_d$ **to** $(n-1)T_s + t_d + d_2 T_s - d_1 T_s$

$$\dot{\hat{x}} = A_2 \hat{x} + K_1 \hat{d}_1 \quad (3.50)$$

Apply Laplace transform

$$(sI - A_2) \hat{x}(s) = \hat{x}(0) + K_1 [\hat{d}_1(n-1)] e^{-((n-1)T_s + t_d)s} \quad (3.51)$$

Apply inverse Laplace Transform

$$\hat{x}(t) = e^{A_2 T_s} \hat{x}(0) + K_1 [\hat{d}_1(n-1)] e^{A_2(t - ((n-1)T_s + t_d))} \quad (3.52)$$

$$\hat{x}((n-1)T_s + t_d + d_2 T_s - d_1 T_s) = e^{A_2(d_2 T_s - d_1 T_s)} e^{A_2 t_d} \hat{x}((n-1)T_s + t_d) + K_1 [d_1(n-1)T_s] e^{A_2(d_2 T_s - d_1 T_s)} \quad (3.53)$$

From $(n-1)T_s + t_d + d_2 T_s - d_1 T_s$ to $(n-1)T_s + t_d + d_2 T_s - d_1 T_s + T_s - d_2 T_s$

$$\dot{\hat{x}} = A_3 \hat{x} + K_2 \hat{d}_2(n-1)T_s \delta(t - ((n-1)T_s + t_d + (d_2 T_s - d_1 T_s))) \quad (3.54)$$

Apply the Laplace transform

$$(sI - A_3) \hat{x}(s) = \hat{x}(0) + K_2 T_s \hat{d}_2(n-1) e^{-((n-1)T_s + t_d + d_2 T_s - d_1 T_s)s} \quad (3.55)$$

Apply the inverse Laplace transform

$$\hat{x}(t) = e^{A_3} \hat{x}(0) + k_2 T_s \hat{d}_2(n-1) e^{A_3[t - ((n-1)T_s + t_d + d_2 T_s - d_1 T_s)]} \quad (3.56)$$

$$x((n-1)T_s + t_d + (d_2 T_s - d_1 T_s) + T_s - d_2 T_s) = e^{A_3(T_s - d_2 T_s)} \hat{x}((n-1)T_s + t_d + d_2 T_s - d_1 T_s)$$

$$+K_2T_s\hat{d}_2(n-1)e^{A_3[T_s-d_2T_s]} \quad (3.57)$$

$$\begin{aligned} \hat{x}(t) = & e^{A_3(T_s-d_2T_s)} e^{A_2(d_2T_s-d_1T_s)} e^{A_2t_d} \hat{x}[(n-1)T_s] \\ & + K_1T_s e^{A_3(d_2T_s-d_1T_s)} e^{A_2t_d} \hat{x}[(n-1)T_s] + K_2T_s e^{A_3(T_s-d_2T_s)} \hat{d}_2(n-1) \end{aligned} \quad (3.58)$$

From interval $x((n-1)T_s+t_d+(d_2T_s-d_1T_s)+T_s-d_2T_s)$ to $\hat{x}(nT_s)$

$$\dot{\hat{x}} = A_1\hat{x} \quad (3.59)$$

Apply the Laplace transform

$$\hat{x}(s) = \frac{1}{sI - A_1} \hat{x}(0) \quad (3.60)$$

$$\begin{aligned} \hat{x}[nT_s] = & e^{A_1T_s} \hat{x}((n-1)T_s) + K_1T_s e^{A_3[T_s-d_2T_s]} e^{A_2[d_2T_s-d_1T_s]} e^{A_1[d_1T_s-t_d]} \hat{d}_1(n-1) \\ & + (KT) e^{A_3[T_s-d_2T_s]} e^{A_1[d_1T_s-t_d]} \hat{d}_2(n-1) \end{aligned} \quad (3.61)$$

$$\hat{x}[nT_s] = \phi\hat{x}((n-1)T_s) + \gamma_1\hat{d}_1(n-1) + \gamma_2\hat{d}_2(n-1) \quad (3.62)$$

Apply Z-transform to the eqn. (3.62)

$$\hat{x}(z) = \phi z^{-1}\hat{x}[z] + \gamma_1 z^{-1}\hat{d}_1(z) + \gamma_2 z^{-1}\hat{d}_2(z) \quad (3.63)$$

$$\hat{x}(z) = [zI - \phi]^{-1}\gamma_1\hat{d}_1(z) + [zI - \phi]^{-1}\gamma_2\hat{d}_2(z) \quad (3.64)$$

The output equation is given by

$$\hat{y}(n) = E\hat{x}(n) \quad (3.65)$$

By applying z-transform to eq. (3.65)

$$\hat{y}(z) = E\hat{x}(z) \quad (3.66)$$

Substituting eq. (63) in eq. (3.66) and assuming

$$\hat{d}_2(z) = 0$$

$$G_{11} = \left. \frac{\hat{V}_o(z)}{\hat{d}_1(z)} \right|_{\hat{d}_2(z)=0} = E[zI - \phi]^{-1} \gamma_1 \quad (3.67)$$

and assuming

$$\hat{d}_1(z) = 0$$

$$G_{12} = \left. \frac{\hat{V}_o(z)}{\hat{d}_2(z)} \right|_{\hat{d}_1(z)=0} = E[zI - \phi]^{-1} \gamma_2 \quad (3.68)$$

$$\text{Here } \phi = e^{AT_s}; \gamma_2 = K_1 e^{A_3[T_s - d_2 T_s]} e^{A_2[d_2 T_s - d_2 T_s]} e^{A_1[d_1 T_s - t_d]}$$

Similarly

$$G_{21} = \left. \frac{\hat{i}_m(z)}{\hat{d}_1(z)} \right|_{\hat{d}_2(z)=0} = P[zI - \phi]^{-1} \gamma_1 \quad (3.69)$$

$$G_{22} = \left. \frac{\hat{i}_m(z)}{\hat{d}_2(z)} \right|_{\hat{d}_1(z)=0} = P[zI - \phi]^{-1} \gamma_2 \quad (3.70)$$

$$\begin{bmatrix} V_o \\ I_{in} \end{bmatrix} = \begin{bmatrix} G_{11}(z) & G_{12}(z) \\ G_{21}(z) & G_{22}(z) \end{bmatrix} \begin{bmatrix} \hat{d}_1(z) \\ \hat{d}_2(z) \end{bmatrix} \quad (3.71)$$

The control to output and control to input discrete-time transfer functions are derived and given in eq. 3.71, in the similar lines the small-signal discrete performance transfer functions may be derived discussed in the next part.

3.5 Small signal open-loop discrete-time transfer functions

The open-loop dynamics of the converter which yields the performance of TICs to characterize the input and output open loop operations can be derived in the comparable lines of the procedure mentioned previously might be acquired for: line-to-output transfer function (G_{vg}), converter output impedance transfer function (Z_o), input admittance transfer function (G_{Yig}), Reverse current gain transfer function (G_{igo}), Control to Input Transfer function (G_{id}), from the small-signal transfer functions.

The controller is designed based on the small-signal transfer functions ([1], [47], [48], [49]).

There are six main small-signal transfer functions for a TICs used to define their dynamics completely. They are:

1. Converter control – to – Output transfer function ‘ G_{vd} ’: describes the influence of control signal $\hat{d}(z)$ on the output voltage given by eq. 3.72, and is a key component in the loop gain, derived by setting the small-signal variations of $\hat{v}_g(z)$, $\hat{i}_o(z)$ to zero.

$$G_{vd}(z) = \left. \frac{\hat{v}_o(z)}{\hat{d}_i(z)} \right|_{\hat{v}_{g_i}(z)=0, \hat{i}_o(z)=0} \quad (3.72)$$

2. Converter Output impedance transfer function ‘ Z_{out} ’: This transfer function is obtained by setting the source and duty cycle perturbations to zero. It describes how the variation in the load current affects the load voltage given in eq. 3.73.

$$Z_{out}(z) = \left. \frac{\hat{v}_o(z)}{\hat{i}_o(z)} \right|_{\hat{v}_{g_i}(z)=0, \hat{d}_i(z)=0} \quad (3.73)$$

3. Audio-susceptibility transfer function ‘ G_{vg} ’: is obtained by setting $\hat{d}(z), \hat{i}_o(z)$ to zero. It describes how the small-signal variation in the source reflects in the load voltage, shown in eq. (3.74).

$$G_{vg}(z) = \left. \frac{\hat{v}_o(z)}{\hat{v}_{gi}(z)} \right|_{\hat{d}_i(z)=0, \hat{i}_z(z)=0} \quad (3.74)$$

4. Input Admittance transfer function ‘ G_{Yig} ’: it is obtained by setting them $\hat{d}(z), \hat{i}_o(z)$ to zero and is given by eq. (3.75).

$$G_{Yig}(z) = \left. \frac{\hat{i}_g(z)}{\hat{v}_{gi}(z)} \right|_{\hat{d}_i(z)=0, \hat{i}_z(z)=0} \quad (3.75)$$

5. Reverse (input– to – output) current gain transfer function ‘ G_{igo} ’: also called as reverse current Audiosusceptibility obtained in eq. (3.76) by setting the source and control perturbations to zero.

$$G_{igo}(z) = \left. \frac{\hat{i}_{g2}(z)}{\hat{i}_z(z)} \right|_{\hat{v}_g(z)=0, \hat{d}(z)=0} \quad (3.76)$$

6. Control – to – Input transfer function ‘ G_{id} ’: this TF is useful in the point of obtaining the current loop in current mode control given in eq. 3.66, by setting the source and current perturbations to zero

$$G_{id}(z) = \left. \frac{\hat{i}_{g2}(z)}{\hat{d}_i(z)} \right|_{\hat{v}_{gi}(z)=0, \hat{i}_z(z)=0} \quad (3.77)$$

Table 3. 1 Small-signal transfer functions formulations

Small-signal Transfer Function	Formulae
Control-to-output	$\frac{\hat{v}_o(z)}{\hat{d}(z)} = E(zI - \Phi)^{-1}\gamma$
Audio-susceptibility	$\frac{\hat{v}_o(z)}{\hat{v}_g(z)} = E(zI - \Phi)^{-1}\psi + D$

Output impedance	$\frac{\hat{v}_o(z)}{\hat{i}_z(z)} = E(z-\Phi)^{-1}\Gamma + J$
Control – to – input	$\frac{\hat{i}_g(z)}{\hat{d}(z)} = P(z-\Phi)^{-1}\gamma$
Input admittance	$\frac{\hat{i}_g(z)}{\hat{v}_g(z)} = P(z-\Phi)^{-1}\psi$
Reverse current gain	$\frac{\hat{i}_g(z)}{\hat{i}_0(z)} = P(z-\Phi)^{-1}\Gamma$
where $\psi = BT_s$, $\Gamma = MT_s$	

3.6 Validation of Small Signal Transfer Functions

General formulations of small-signal models of multi-input converter topologies are discussed above, which involves state-space matrices. The state-space matrices are also derived above which are used to generate the frequency response of all the proposed converters and are shown in Fig. 3.2 to Fig. 3.17 with red labeling. The above performed mathematical analysis pertains to state-space models that are formulated for different modes ensures the principle of energy conservation. While this approach might not be prone to errors when modeling lower-order systems, there is a greater chance of errors while modeling higher-order systems. In order to identify such issue, it is essential to first validate the derived mathematical models before making an attempt to design any control strategy. To ensure this, a cross-validation methodology is necessary and therefore, a circuit simulator [PSIM] is adopted in this thesis for the same. Firstly, the circuit structure of the converter is transformed into the simulator for the parameters listed in Table IV. The perturbation is created individually in both d_1 and d_2 through a sinusoidal

source of 0.05 V magnitude with frequency sweep beginning from low range to half of the switching frequency, and AC sweep analysis is performed to generate the frequency response of the TICs as per the procedure reported in [50]. The same procedure has been extended to obtain all the desired frequency responses of all the topologies under investigation. These frequency response plots obtained from schematic simulations are compared by superimposing them (blue colored responses) in Fig. 3.2 to Fig. 3.17. The superimposed plots confirm the effectiveness of the mathematically modeled frequency responses.

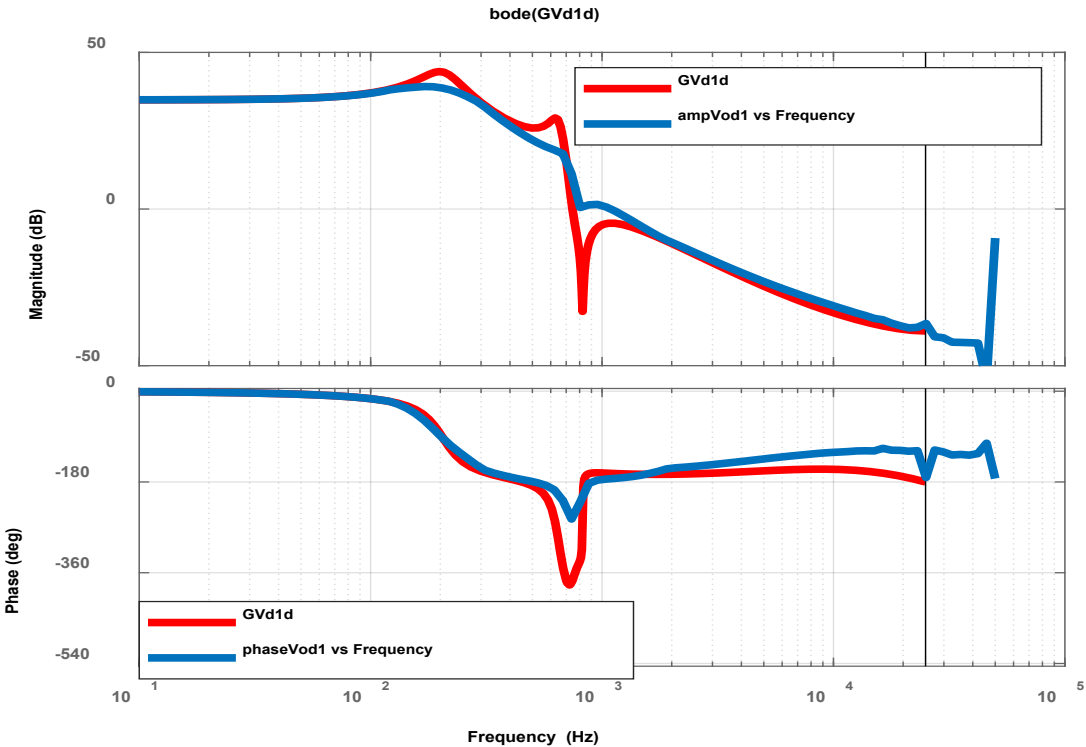


Fig. 3. 2 Control-to-output-Transfer Function-1 $\hat{v}_o(z)/\hat{d}_1(z)$

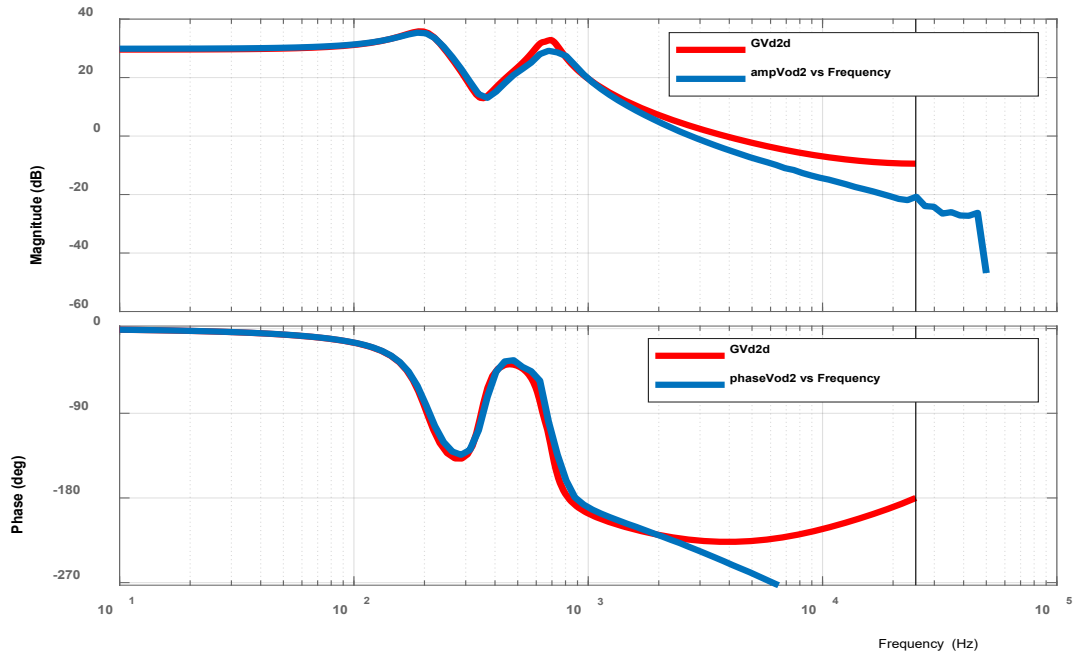


Fig. 3. 3 Control-to-output-Transfer Function-2 $\hat{v}_o(z)/\hat{d}_2(z)$

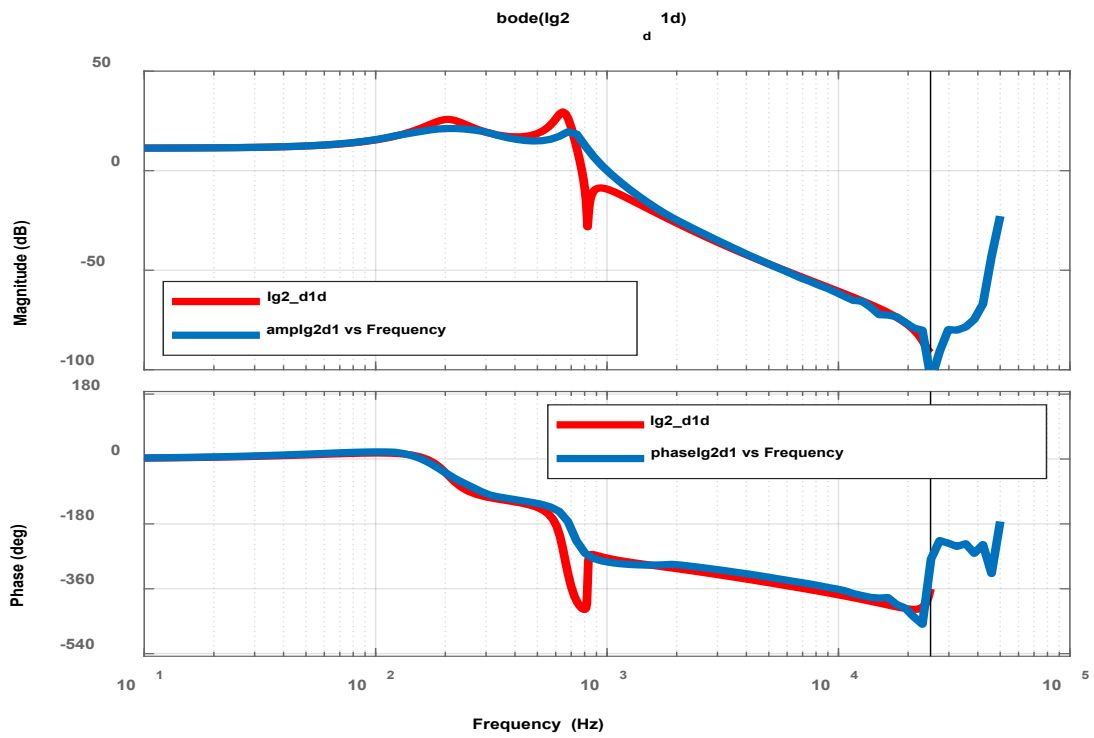


Fig. 3. 4 QBSTIC Control-to-Input-Transfer Function-1 $\hat{i}_{g2}(z)/\hat{d}_1(z)$

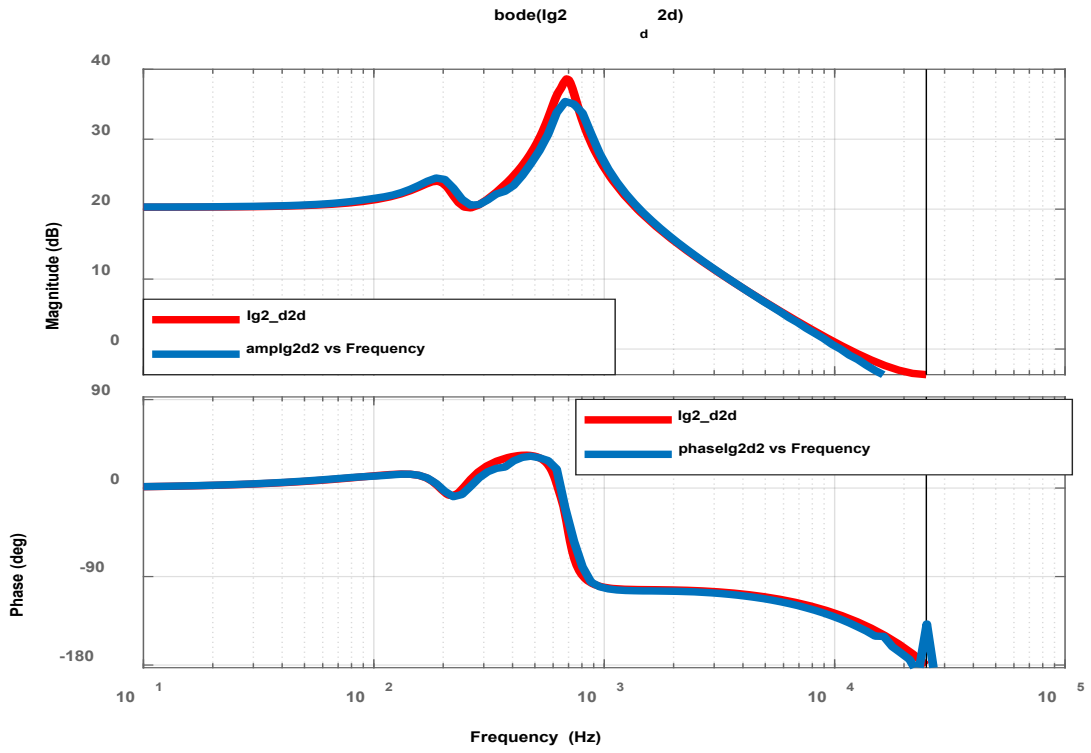


Fig. 3. 5 QBSTIC Control-to-Input-Transfer Function-1 $\hat{i}_{g2}(z)/\hat{d}_2(z)$

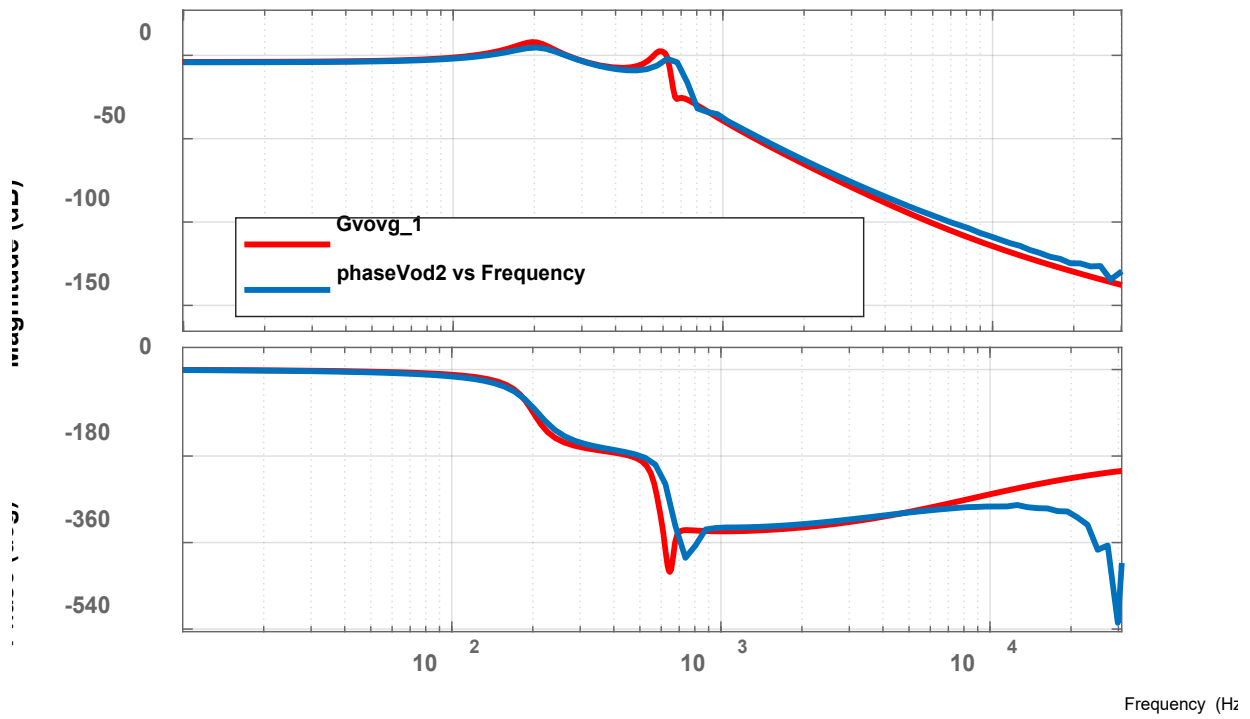


Fig. 3. 6 QBSTIC Audio-Susceptibility-1 $\hat{v}_o(z)/\hat{v}_{g1}(z)$

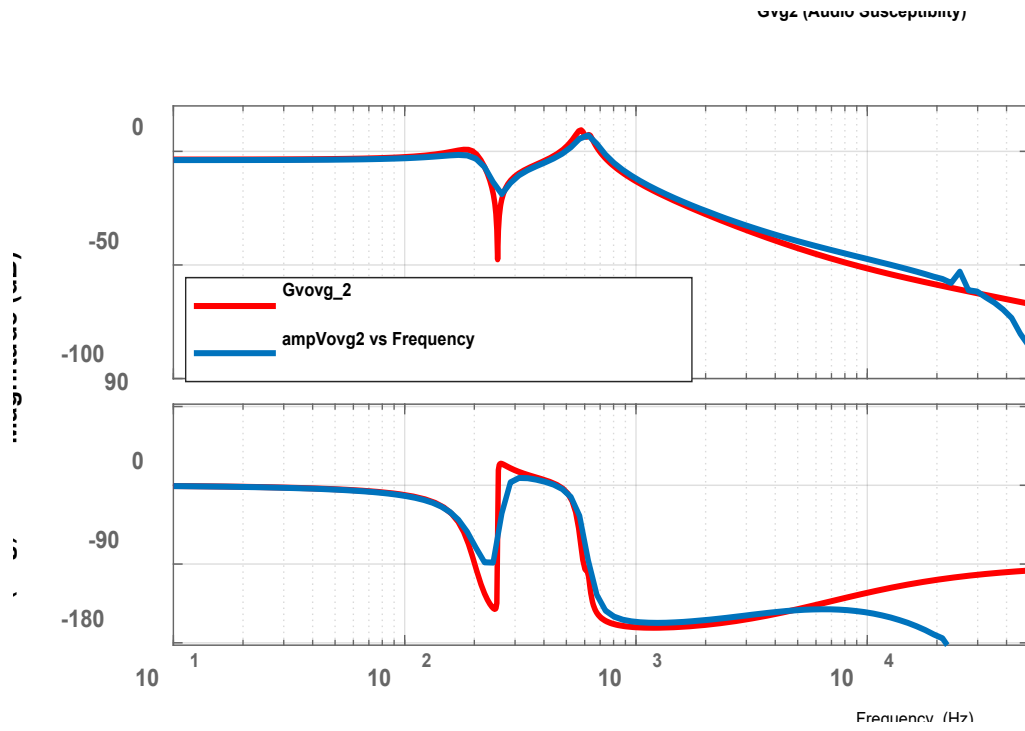


Fig. 3. 7 QBSTIC Audio-Susceptibility-2 $\hat{v}_o(z) / \hat{v}_{g_2}(z)$

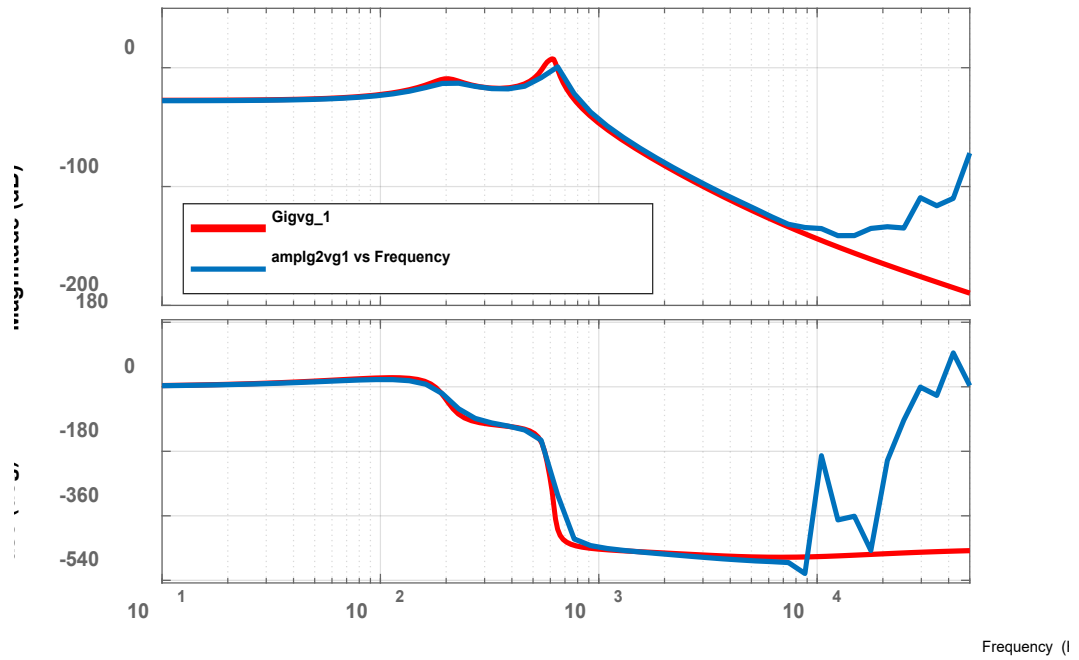


Fig. 3. 8 QBSTIC Audio-Susceptibility-2 $\hat{i}_{g_2}(z) / \hat{v}_{g_1}(z)$

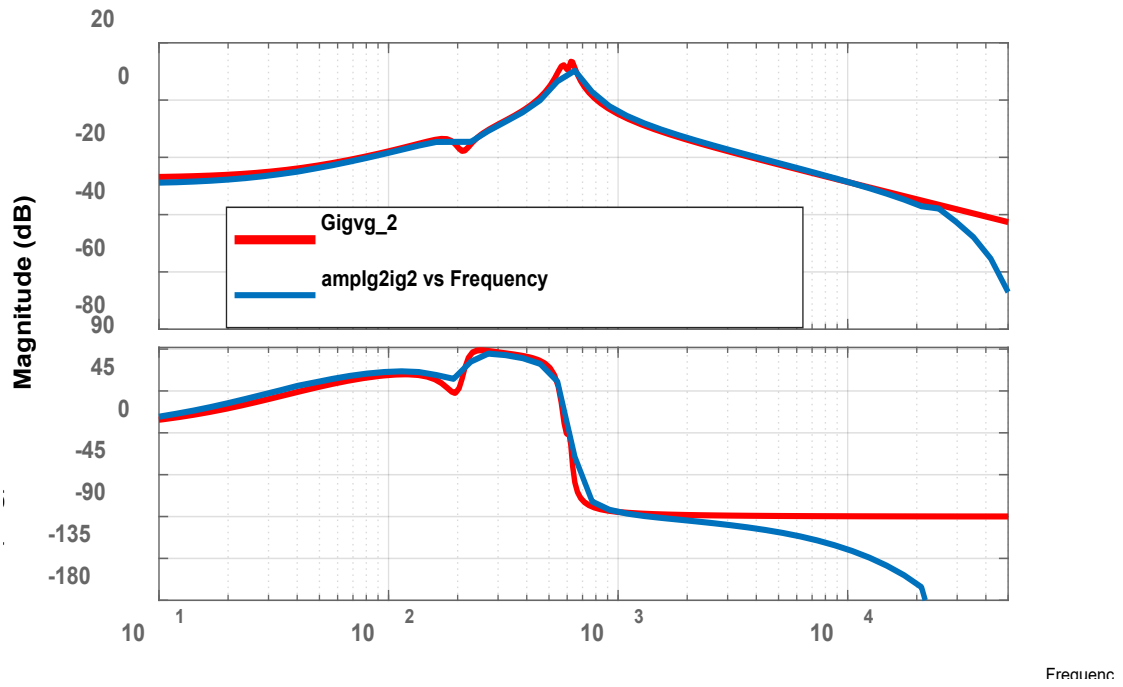


Fig. 3. 9 QBSTIC Audio-Susceptibility-2 $\hat{i}_{g2}(z)/\hat{v}_{g2}(z)$

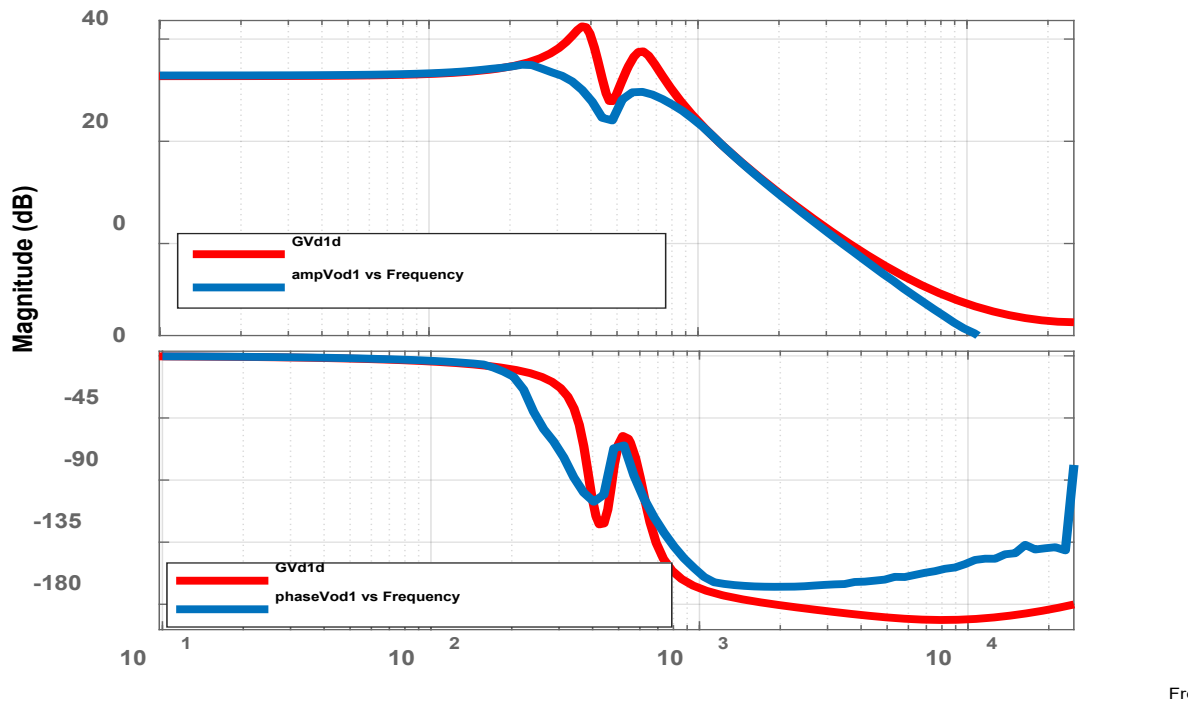


Fig. 3. 10 SIHBSTIC Control-to-output-Transfer Function-1 $\hat{v}_o(z)/\hat{d}_1(z)$ [83]

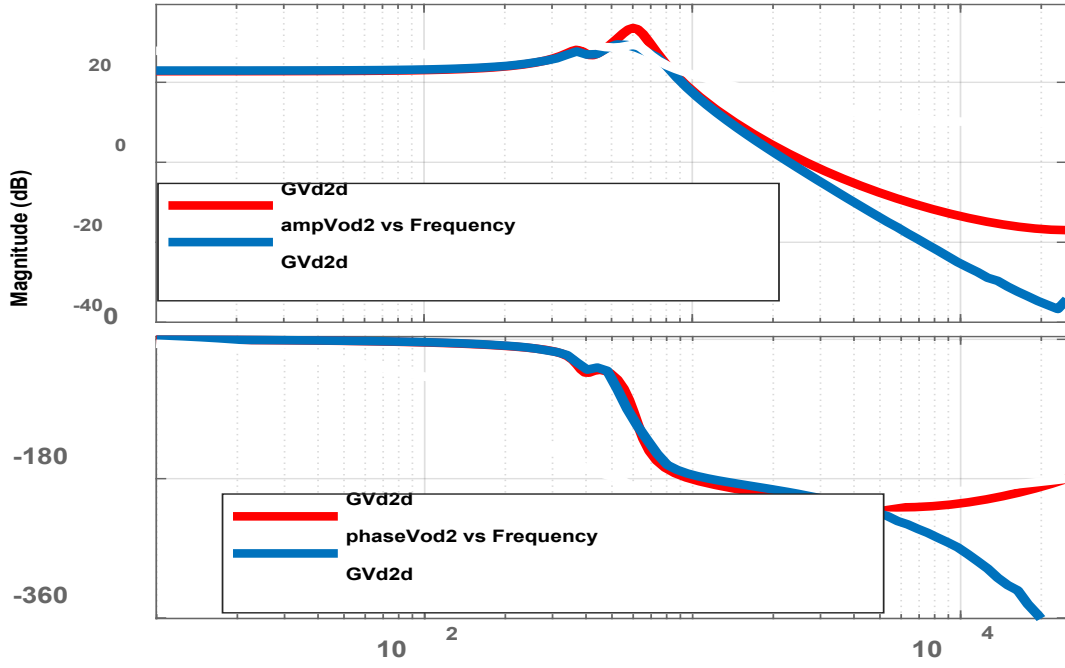


Fig. 3. 11 SIHBSTIC Control-to-output-Transfer Function-2 $\hat{v}_o(z)/\hat{d}_2(z)$

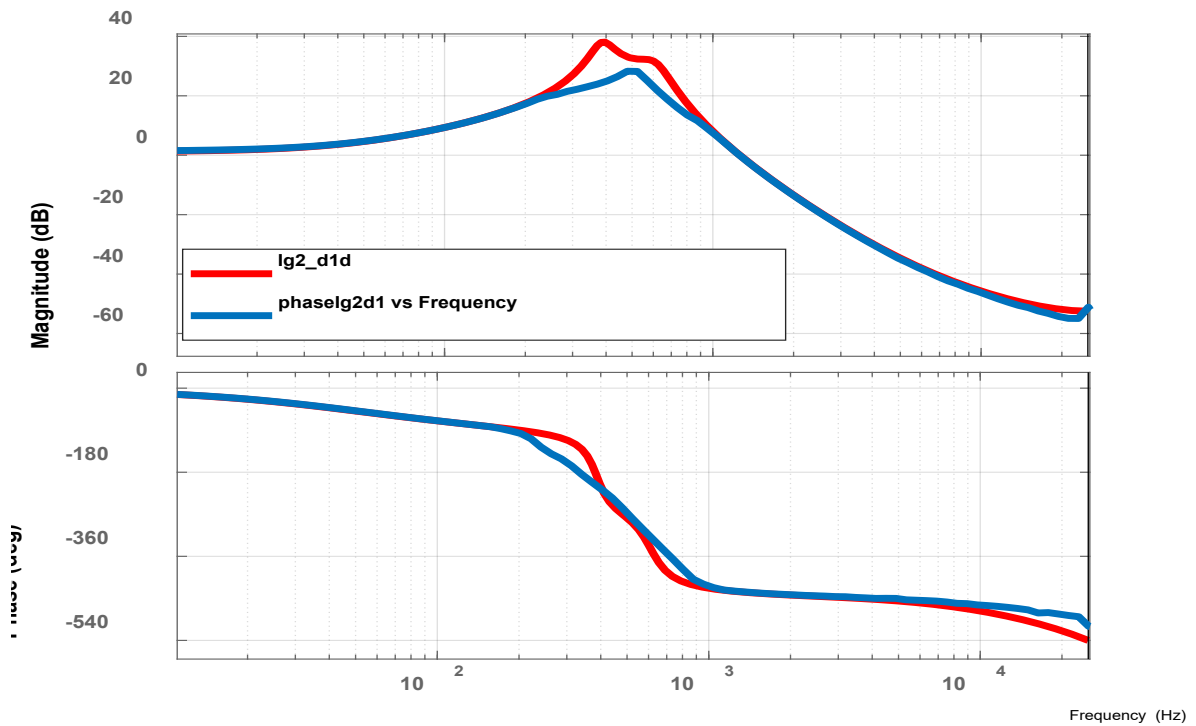


Fig. 3. 12 SIHBSTIC Control-to-Input-Transfer Function-1 $\hat{i}_{g2}(z)/\hat{d}_1(z)$

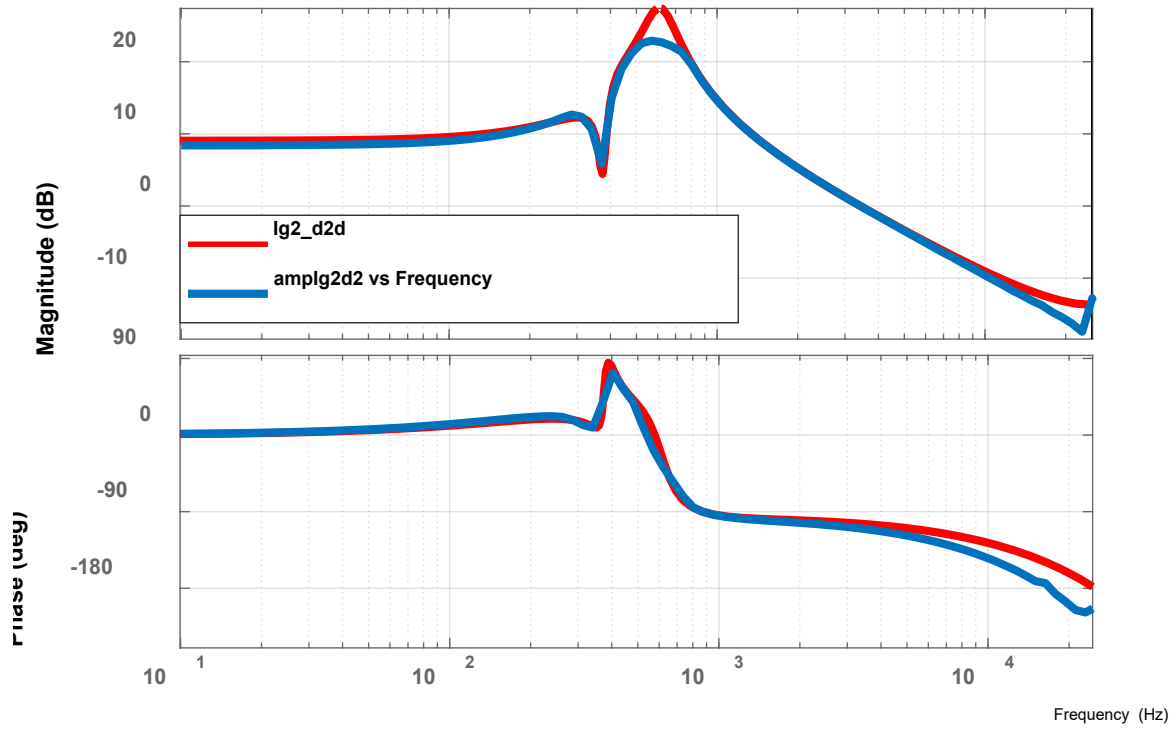


Fig. 3. 13 SIHBSTIC Control-to-Input-Transfer Function-1 $\hat{i}_{g2}(z)/\hat{d}_2(z)$

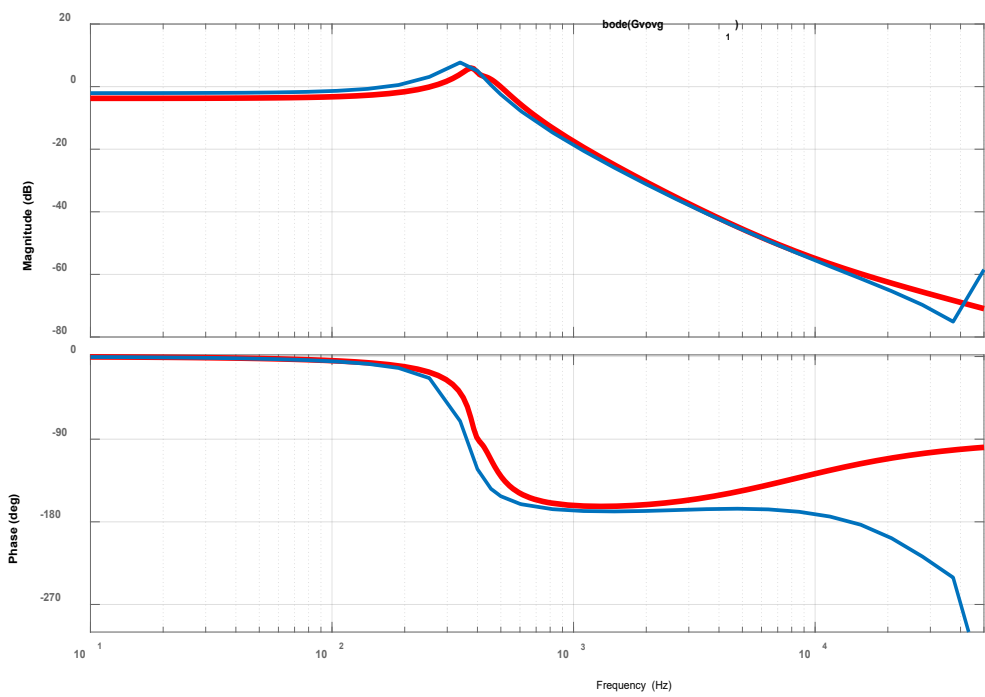


Fig. 3. 14 SIHBSTIC Audio-Susceptibility-1 $\hat{v}_o(z)/\hat{v}_{g1}(z)$

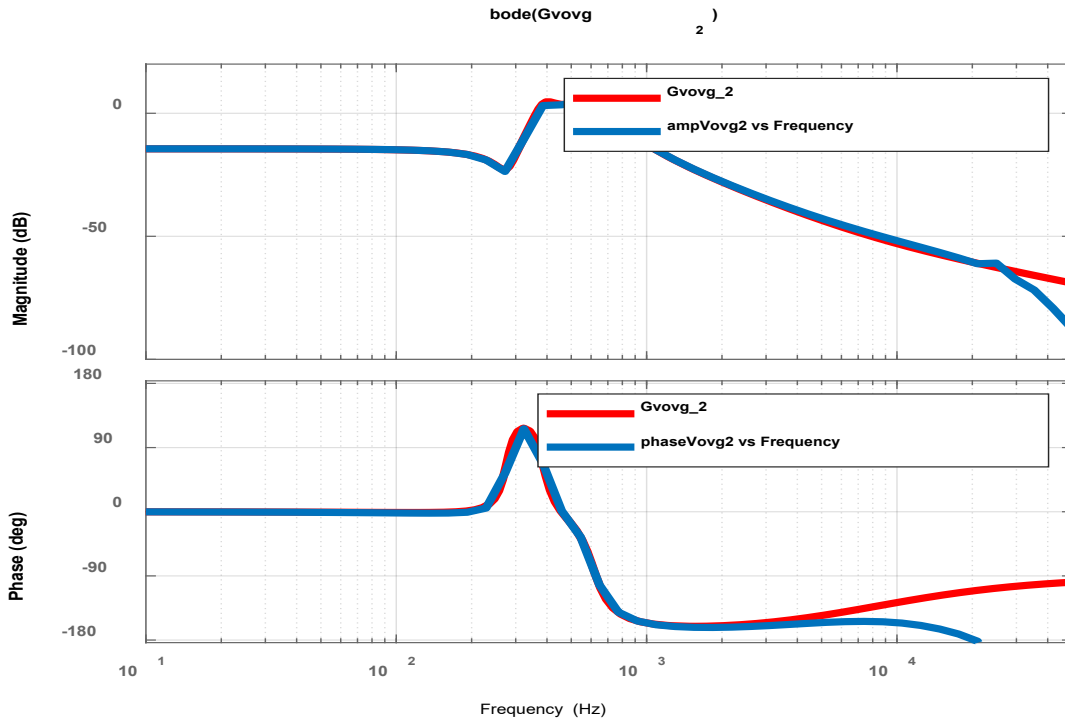


Fig. 3. 15 SIHBSTIC Audio-Susceptibility-2 $\hat{v}_o(z)/\hat{v}_{g_1}(z)$

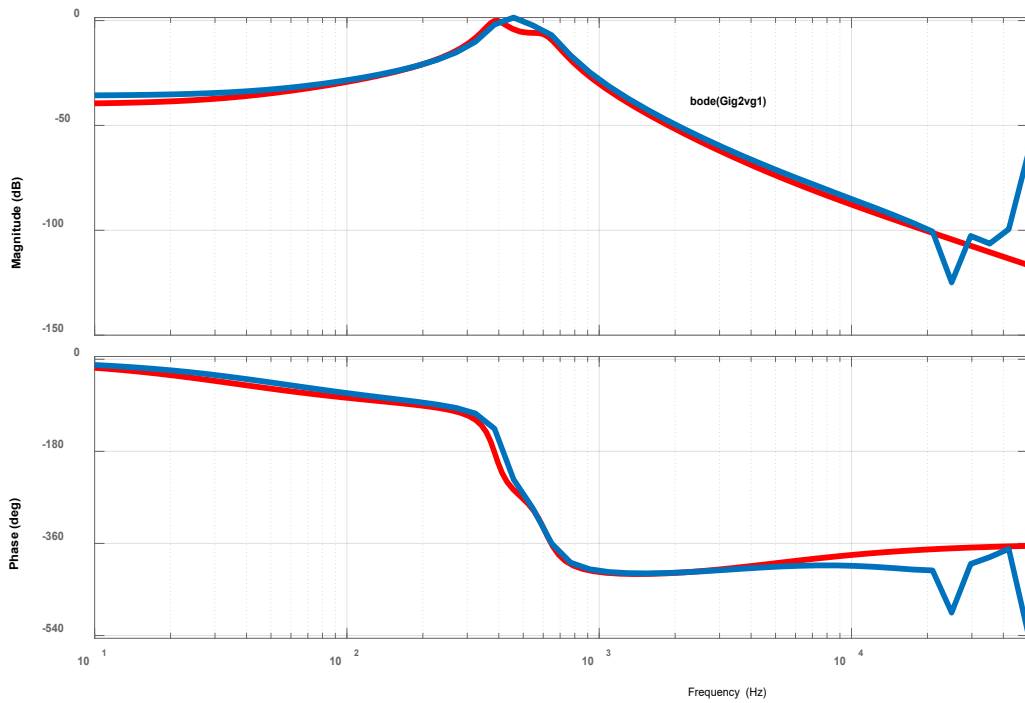


Fig. 3. 16 QBSTIC Audio-Susceptibility-2 $\hat{i}_{g_2}(z)/\hat{v}_{g_1}(z)$

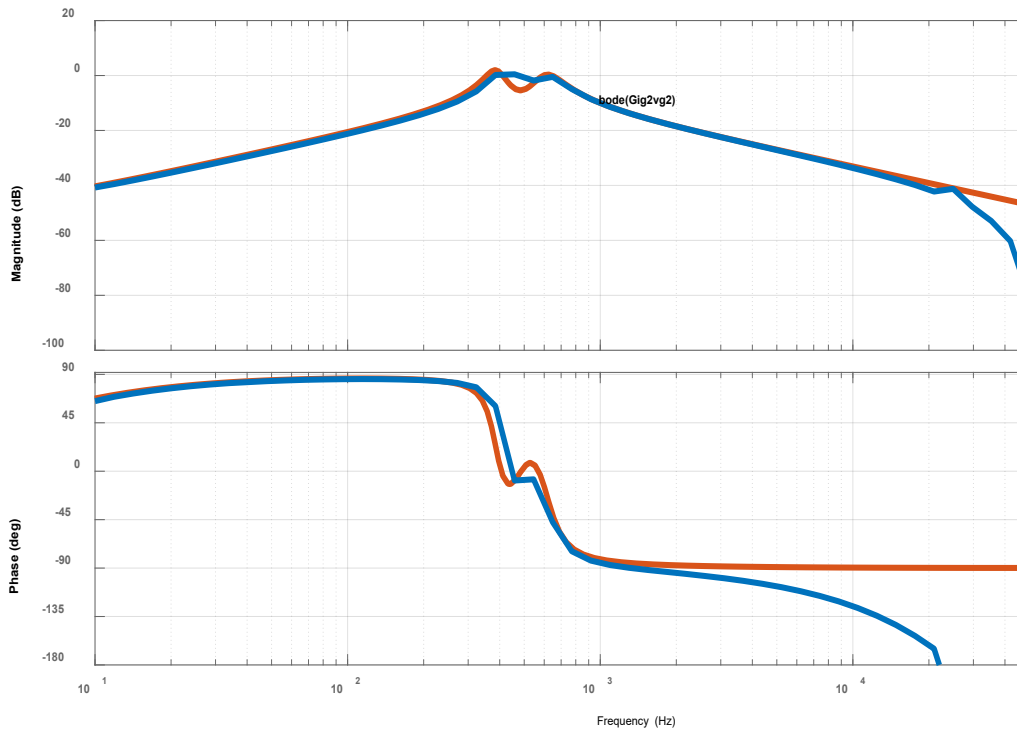


Fig. 3. 17 QBSTIC Audio-Susceptibility-2 $\hat{i}_{g2}(z)/\hat{v}_{g2}(z)$

3.7 Conclusion

In this chapter, the state-space analysis of the two-input dc-dc converter is reported. The state-space analysis was used to find the discrete-time small-signal transfer functions for the two-input dc-dc converter. The frequency responses of different TICs are compared using both the circuit simulator (PSIM) and coding program in MATLAB to make sure that the different transfer functions are valid. The results seem to be convincing. A difference in magnitude and phase response of a few waveforms for Figs. 3.10 and 3.12 was visible. The reason for this difference is that the order of the transfer functions is 5th, 6th, and 7th, and finding the inverse of such a higher-order transfer function and generating their frequency response through simulation is carrying longer simulation minutes. To reduce the time taken for simulation, the higher-order systems are reduced to second-order by order reduction commands (especially the red-colored responses generated using MATLAB), which led to mismatches of responses in a few cases, as all the reduced-order transfer function responses may not be identical with the original transfer function responses. The discrete time transfer functions derived in this chapter will be helpful in designing the controllers discussed in the subsequent chapter.

CHAPTER - 4

CONTROLLER DESIGN

4.1 Introduction

This thesis aims to investigate a multi-input integrated converter (MIC) with two input dc-voltage sources. The two-input integrated converter (TIC) draws power from these two sources and supplies it to the load output, which may be a dc-bus or a stand-alone dc load. Generally, integrated converters are composed of dedicated and intermittent sources. Here, the dedicated source is capable of supplying load demand all the time, and the intermittent power source shares its burden. This sharing of burden depends on the power-generating capability of the intermittent source, which varies depending on the type of source integrated as an intermittent source. For example, in the case of a photovoltaic plant, the power generated depends on environmental and weather conditions, seasonal changes, geographical location, etc. In such cases, the power is drawn from the intermittent source if it is capable of generating it during that time, or else the power is drawn from the dedicated power source. Here, load management becomes crucial as it has to choose between drawing power from either an intermittent or dedicated source. With TICs, the two main power management problems are balancing the input and output power streams and making sure that the power is distributed evenly between the two input voltage sources. The intermittent source supplies power to the load as long as it generates, while the dedicated source is responsible for supplying the rest of the demanded load power. Therefore, an appropriate control scheme must be established for varying power demands.

The dedicated source is the primary power source for the load, while the intermittent source assists the primary power source in supplying the fluctuating load demands. To meet the consistent load current demand continuously, suitable measures must be taken such that the input

current of the intermittent source is controlled to provide a maximum of its rated current. In contrast, the dedicated source will supply the difference between the two currents so that load demand is always met. Here, load management is an important task that has to be done continuously so that power generated by the intermittent source is optimally utilized.

4.1.1. Voltage and current mode control strategies for TIC

Integrated converters need to maintain a constant voltage at the dc-bus/load even if the multiple sources encounter the fluctuations. Also, bus/load voltage has to be maintained firmly even if the fluctuations occur in the load locally or due to downstream loads/converters. In order to achieve this task, a dedicated control strategy has to be formulated. In this thesis, a simple voltage-mode controller (VMC) is used to control the dc-bus/load voltage [51]. To realize this, the dc-bus/load voltage must be sensed on a continuous basis. The sensed load voltage should then be compared with the reference voltage ' V_{ref} ' and depending on the error voltage; the controller has to react so that the aim of constant bus voltage is achieved.

In an integrated converter, load management/sharing on the input dc-source is a crucial task. It can easily be achieved in the TIC by adopting a three-loop current control-strategy, of which two-loops are dedicated to the two sources while the third one aims at controlling the load current. Although this three-loop control scheme seems quite attractive as well effective in load monitoring and also load sharing on the input sources, from the control point of view, it induces many challenging problems in terms of complexity. The complexity in such systems can be minimized by limiting the number of sensing elements without compromising effective load management. Minimization of sensing elements may not be possible for all systems as it primarily depends on the type of system to be controlled. However, in this thesis, there is a scope for minimization of sensors in the case of TIC as only the intermittent source current needs to be controlled.

A single current control-loop is sufficient to achieve effective load sharing on the front-end side of TIC i.e. between the dedicated and intermittent sources. In this thesis, investigations are carried out for dc-bus voltage regulation along with load management on the input dc-sources. A single-loop voltage-mode controller is adopted for bus voltage regulation whereas a current control-loop ensures load management task.

In this current control scheme, the inductor current is sensed continuously and then the switch S_2 PWM control signal is adjusted to ensure the regulation. In this converter, the intermittent source has limited energy and thus to restrict current drawn from this source, a closed-loop current mode control is utilized. The two quantities which should be controlled are load voltage and source current, whereas the controlling quantities accessible are the switching devices duty ratio's d_1 and d_2 , which are utilized to perform the necessary control tasks as well as to generate desired PWM signals. These PWM signals are necessary to operate the TIC to obtain the voltage regulation and appropriate load sharing irrespective of source and load disturbances.

4.1.2 Controller design for the two-input DC-DC converter

In order to obtain optimal power flow control between the two sources and common load, designing of the appropriate controllers for the two-input integrated converters are necessary. The controllers' design for stand-alone single input DC-DC converters is well established, which primarily uses the linear control principles. These controllers can perform either current or voltage regulation or both but it is achieved with only one controlling duty ratio. In the case of TIC, controlling only one duty ratio is not adequate to perform the dual task of load management as well as bus voltage regulation. Since the proposed TIC's have two controlling quantities contrary to the single-input converters, the implementation of a multi-variable controller offers a promising solution for effective power management. Due to the integrated structure of the TIC's as well as the presence of common power flow paths there exist interactions. Further, these

interactions become more pronounced when the control-loop is closed. Hence, the implementation of a multi-variable control strategy becomes imperative for such systems.

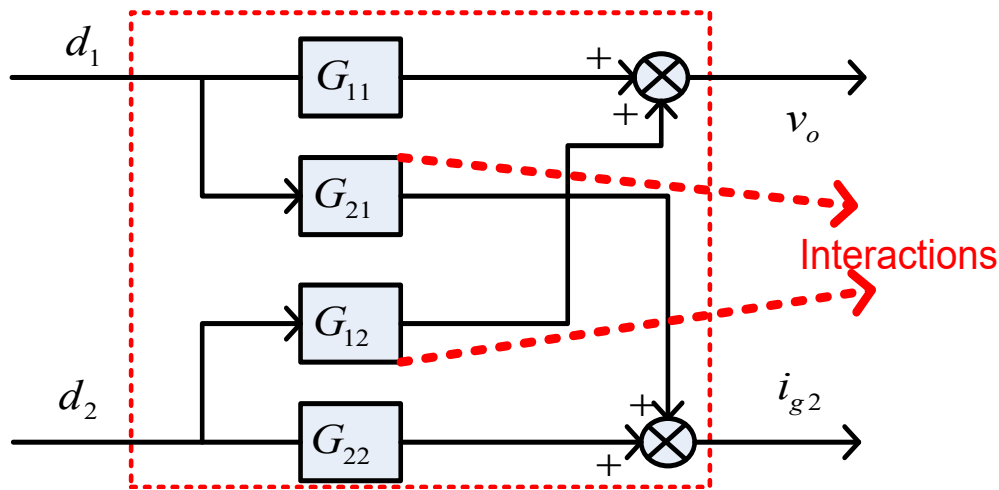
In the case of TIC's under investigation, there are two controlling quantities (d_1 and d_2) as outlined above. Also, these two controlling quantities (d_1 and d_2) are required to perform front-end side load management (i.e., source current regulation) as well as the back-end load voltage regulation. Due to the converter structure, which as discussed above, one controlled quantity is present at the input-port while the second quantity is present at the output port of the converter. When power flows from source end to load end via the intermediate TIC, interactions are bound to happen between the two controlling loops. All TIC's are capable of handling the power management task but vary in terms of achievable performance.

Because every TIC has a different set of controlling inputs and controlled outputs, the performance trade-offs are used to decide which TIC to use. Any pairing of controlling inputs and controlled outputs could provide stability problems for TIC and prove to be unfeasible. As a result, methodological solutions based on the principles of energy conservation and control theory are required. All the TICs examined in this thesis feature two switches that allow for the regulation of both source current (i_{g2}) and load voltage (V_o). As a result, managing power becomes an intriguing multi-variable control problem. The plant is characterized by a series of expressions which are mentioned below are functions of both the controlling and controlled variables.

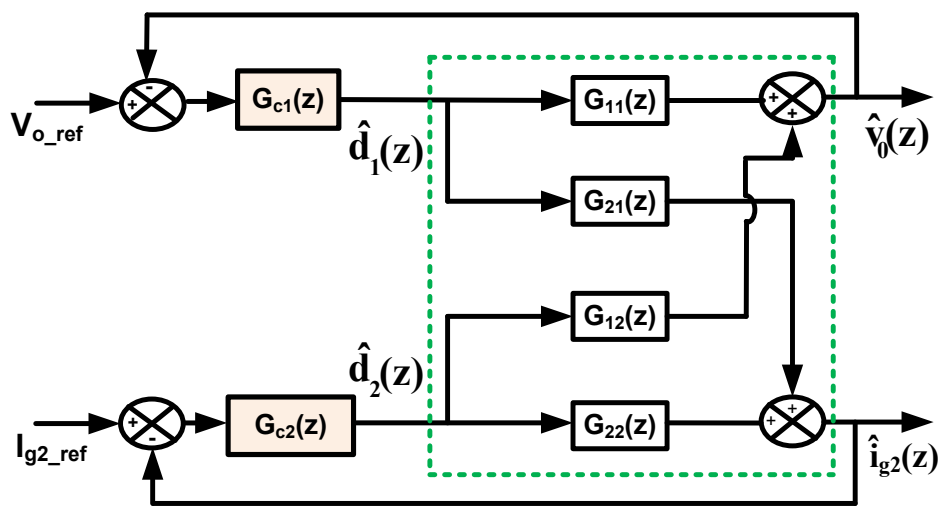
The equations given below are more general and are equally applicable for all the TIC's proposed in the thesis.

$$\begin{aligned} v_o &= f(d_1, d_2) \\ i_{g2} &= f(d_1, d_2) \end{aligned} \tag{4.1}$$

$$\begin{aligned} v_o &= G_{11}d_1 + G_{12}d_2 \\ i_{g2} &= G_{21}d_1 + G_{22}d_2 \end{aligned} \tag{4.2}$$



(a) Block Diagram representation of the two-input DC-DC converter



TIC – Small-signal model

Fig. 4. 1 (b) Closed loop Block Diagram representation of system with decentralized controllers

From the eq. (4.1) it can be said that the load voltage, as well as the source current, are dependent on both the switches duty ratio signals d_1 and d_2 . The possible control combinations are listed below.

- i) Load voltage regulation is obtained by controlling duty ratio 'd₁' and the current tracking by controlling duty ratio 'd₂'.
- ii) The same above can also be achieved by swapping the two duty ratio control signals.

Though the above-stated combinations may be possible, but their final selection depends on the nature of interactivity among the loops. To address such issues on mathematical grounds, different control strategies of MIMO systems are reported in the literature. Some control methods

reported deal with interactions while others are independent of interactions. If the degree of interactions is weak, the decentralized control structure is easily applicable [10]. Alternatively, to minimize the interactions a de-coupler along with a decentralized controller methodology can be adopted [25]. In case the interactions are predominant, a higher number of controllers (more than decentralized controllers) are needed to stabilize the plant [26-29]. Several classical controller design techniques such as linear quadratic gaussian (LQG), individual channel design (ICD) methods, robust H_∞ controller design methods, sequential MIMO non-diagonal controller designs, frequency-based quantitative feedback theory (QFT) loop shaping methods are belonging to robust control design strategy [61]-[74]. All these methods are evolved to cater to the needs of a variety of systems, be it either SISO or MIMO. However, the selection of methodology depends on the specific goals pertaining to the system and the applicability of the specific method. The majority of the controller design methods use weight functions and their construction for a specific system is a tedious task.

Further, the H_∞ type designs invariably result in higher-order controllers as discussed in [47]. However, the difficulties which are posed by the methods involving weight functions have been overcome using a frequency domain based open-loop shaping with QFT approach for robust control design of switched-mode power supplies (SMPS). This established QFT methodology has been widely applied for SISO systems and its philosophy is now extended to the proposed two-input integrated converter systems. The work presented here has been focused mainly on developing multi-variable controllers design based on QFT approach. Firstly, MIMO QFT based controller designs is discussed for the QBSTIC system and are followed by decoupled-decentralized MIMO controller design for SIHBSTIC.

The general block diagram representing the TIC's belonging to the MIMO system is shown in Fig. 4.1. In this block-diagram, the transfer functions G_{12} and G_{21} represent the interactions existing in the TIC. These two transfer functions primarily give the degree of interaction. If either of the transfer functions or both are zero, then it indicates minimal interactions exist in the

corresponding TIC. If the transfer functions G_{12} and G_{21} are zero, it indicates that the corresponding MIMO system is diagonal, and it is called the decoupled system. For the decoupled system, only the diagonal control strategy is sufficient, else individual controllers must be designed based on all the transfer functions shown in the block diagram.

The following factors must be considered while building MIMO closed loop converter controllers: (i) stability; (ii) capability to track the reference signal; (iii) rejection of external disturbances at plant output; (iv) rejection of external disturbances at plant input; (v) minimization of noise-related impacts, etc. ([57], [58]). Transfer functions are used to analyze, impose limits, and take corrective action for each of the aforementioned problems in order to achieve the intended system response throughout the entire range of uncertainty.

4.2 Pairing of control Inputs and Outputs

Fig. 4.1 shows the general block diagram of the TIC's wherein a pair of controlling and controlled variables. One method that can be used to suggest pairings by measuring the degree of coupling or interaction in a system is known as the Relative Gain Array (RGA) [52]. This method is an analytical tool used to determine the possible input-output variable pairings for a multi-input-multi-output (MIMO) system. Several similar quantitative techniques are available to assist in this pairing selection process, but RGA is sufficient enough to identify the best pairing combination for the proposed TIC's. Each element in the RGA matrix is a measure of the relative gain of that particular control loop. The relative gain is the ratio between the open-loop gain and the closed-loop gain.

The relative gain array (RGA), $R(s)$, is useful for establishing the best input-output control pairings for use in the control of a multivariable system [8]. The array $R(s)$ is defined as the element-by-element product of the transfer-function matrix $G(s)$ and the transpose of the inverse of this matrix. Typically, the relative gain array is calculated by evaluating the plant transfer function at zero frequency, and its mathematical expression is given by

$$RGA = G(0) * (G^T(0))^{-1} . \quad (4.3)$$

This technique is based upon the open-loop steady-state gains of the process and is relatively simple to interpret. The only information needed for the calculation of the relative gain array is the steady-state gain matrix $G(0)$. The RGA of a non-singular (2x2) square complex matrix is defined as

$$A = G(0) * (G^{-1}(0))^T = \begin{bmatrix} \lambda_{11} & \lambda_{12} \\ \lambda_{21} & \lambda_{22} \end{bmatrix} = \begin{bmatrix} \lambda_{11} & I - \lambda_{11} \\ I - \lambda_{11} & \lambda_{11} \end{bmatrix} \quad (4.4)$$

$$\text{where } \lambda_{11} = \left(I / \begin{bmatrix} I - \frac{G_{12}G_{21}}{G_{11}G_{22}} \end{bmatrix} \right)$$

Relative-gain interpretation is discussed in ([52],[18]). The plant is decoupled if the RGA is near the identity matrix; if not, interactions must be assumed to be present. In order to prevent instability problems, pairings on negative RGA elements should be avoided. Instead, pairings corresponding to RGA elements should be selected near to '1' or higher value. Furthermore, higher RGA-element values indicate a very sensitive process. As a result, managing such a plant becomes challenging. Table 4.1 lists the RGA matrices that were derived for QBSTIC, SIHBSTIC, SCHBSTIC Topology-1, and SCHBSTIC Topology-2. It also suggests the optimal control-loop pairings that might be made for each TIC.

Table 4. 1 RGA Matrices of TIC Topologies

TIC Topologies	SIHBSTIC	QBSTIC	SCHBSTIC-1	SCHBSTIC-2
RGA	$\begin{bmatrix} 1.1371 & -0.1371 \\ -0.1371 & 1.1371 \end{bmatrix}$	$\begin{bmatrix} 1.128 & -0.128 \\ -0.128 & 1.128 \end{bmatrix}$	$\begin{bmatrix} 1.257 & -0.257 \\ -0.257 & 1.257 \end{bmatrix}$	$\begin{bmatrix} 1.0364 & -0.0364 \\ -0.0364 & 1.0364 \end{bmatrix}$
Control-loop pairings	$(v_o \rightarrow d_1)$ $(i_{g2} \rightarrow d_2)$	$(v_o \rightarrow d_1)$ $(i_{g2} \rightarrow d_2)$	$(v_o \rightarrow d_1)$ $(i_{g2} \rightarrow d_2)$	$(v_o \rightarrow d_1)$ $(i_{g2} \rightarrow d_2)$

4.3 Realization of MIMO systems with Single loop equivalents

A challenging issue with multivariable systems is the impact of interactions and their presence, which gets reflects when the control-loops are closed which can easily be seen by way influencing the dynamics of different states. Therefore, the coupling information is needed to design and apply some of the SISO controller design methods to MIMO controller designs. It also gives the scope of applying the procedures of sequential loop closing methods, individual channel design method ([53], [54]), sequential diagonal/non-diagonal MIMO QFT design procedures etc,. The main contribution of this thesis is to apply and design the controllers using QFT based approach to the proposed TICs. The individual channel design (ICD) based technique is also outlined for getting insight into the multi-variable controller designs.

4.3.1 Applying ICD technique to TICs

The ICD technique is one of the controller design tools available for power supply designers [52], in this thesis it is applied to design controllers for SIHBSTIC topology. This is the easiest way to get multi-variable controllers employing which the given TIC can be controlled [18]. The ICD technique is a framework wherein frequency response (Bode/ Nyquist) techniques are applied directly to the independent channels under all circumstances, including when cross-coupling is substantial [69]. Here, the multivariable system which may have either strong or weak interactions is decomposed into an equivalent set of single-input single-output (SISO) systems and are called as individual channels. To illustrate the controller design principle, the block diagram shown in Fig. 4.1 is considered and is used to establish the following analysis.

$$Y(z) = G(z)d(z) \tag{4.5}$$

$$\begin{bmatrix} y_1(z) \\ y_2(z) \end{bmatrix} = \begin{bmatrix} G_{11}(z) & G_{12}(z) \\ G_{21}(z) & G_{22}(z) \end{bmatrix} \begin{bmatrix} d_1(z) \\ d_2(z) \end{bmatrix}$$

where G_{11} , G_{12} , G_{21} , G_{22} given by equations 3.67, 3.68, 3.69, 3.70.

The diagonal controller is given by

$$d(z) = G_c(z)e(z) \quad (4.6)$$

$$\begin{bmatrix} d_1(z) \\ d_2(z) \end{bmatrix} = \begin{bmatrix} k_{11}(z) & 0 \\ 0 & k_{22}(z) \end{bmatrix} \begin{bmatrix} e_1(z) \\ e_2(z) \end{bmatrix} \quad (4.7)$$

$$\text{where } e_i = r_i - y_i \quad ; \quad i = 1, 2 \quad (4.8)$$

The channel can be defined as

$$C_i(z) = k_{ii}g_{ii}(z)(1 - \gamma(z)h_j(z)) \quad (4.9)$$

where $i \neq j$ and $i, j=1, 2$

$$h_i(z) = \frac{k_i(z)g_{ii}(z)}{1 + k_{ij}(z)g_{ji}(z)} \quad \text{and} \quad \gamma_a(z) = \frac{G_{12}(z)G_{21}(z)}{G_{11}(z)G_{22}(z)} \quad , \quad \gamma_b(z) = \frac{G_{11}(z)G_{22}(z)}{G_{12}(z)G_{21}(z)} \quad \text{are a complex valued}$$

function, is referred to as multi variable structural function (MSF) of diagonal and off-diagonal controllers.

Substituting the values of Tables 2.5, and 2.6 in eq's. 3.67 to 3.70 the following transfer functions mentioned in eq.s 4.10a to 4.10d were obtained for SIHBSTIC.

$$G_{11} = \frac{1.351z^3 - 3.408z^2 + 2.792z - 0.73141}{z^4 - 3.871z^3 + 5.64z^2 - 3.665z + 0.8963} \quad (4.10a)$$

$$G_{12} = \frac{-0.06468z^3 + 0.0768z^2 + 0.01403z - 0.02608}{z^4 - 3.871z^3 + 5.64z^2 - 3.665z + 0.8963} \quad (4.10b)$$

$$G_{21} = \frac{0.6008z^3 - 1.434z^2 + 1.079z - 0.2445}{z^4 - 3.871z^3 + 5.64z^2 - 3.665z + 0.8963} \quad (4.10c)$$

$$G_{22} = \frac{1.448z^3 - 4.25z^2 + 4.165z - 1.363}{z^4 - 3.871z^3 + 5.64z^2 - 3.665z + 0.8963} \quad (4.10d)$$

The general form of MSF and its specific form for diagonal controller respectively are

$$\gamma_a(s) = \frac{g_{12}(s)g_{21}(s)}{g_{11}(s)g_{22}(s)} \quad (4.10e)$$

$$\gamma_a = \frac{-0.01986z^{14} + 0.2247z^{13} - 1.159z^{12} + 3.588z^{11} - 7.384z^{10} + 10.52z^9 - 10.38z^8 + 6.696z^7 - 2.12z^6 - 0.6091z^5 + 1.105z^4 - 0.6246z^3 + 0.1966z^2 - 0.03437z + 0.002618}{z^{14} - 13.2z^{13} + 80.85z^{12} - 304.7z^{11} + 788.9z^{10} - 1485z^9 + 2094z^8 - 2249z^7 + 1847z^6 - 1155z^5 + 540.9z^4 - 184z^3 + 42.95z^2 - 6.16z + 0.4093}$$

(4.10f)

The MSF for the off-diagonal controller is given by

$$\gamma_b(s) = \frac{g_{11}(s)g_{22}(s)}{g_{12}(s)g_{21}(s)} \quad (4.10g)$$

$$\gamma_b = \frac{-50.35z^{14} + 664.6z^{13} - 4071z^{12} + 1.534e04z^{11} - 3.972e04z^{10} + 7.476e04z^9 - 1.055e05z^8 + 1.132e05z^7 - 9.302e04z^6 + 5.816e04z^5 - 2.724e04z^4 + 9264z^3 - 2163z^2 + 310.2z - 20.61}{z^{14} - 13.2z^{13} + 80.85z^{12} - 304.7z^{11} + 788.9z^{10} - 1485z^9 + 2094z^8 - 2249z^7 + 1847z^6 - 1155z^5 + 540.9z^4 - 184z^3 + 42.95z^2 - 6.16z + 0.4093} \quad (4.10h)$$

As this transfer function is proper, numerator order is equal to the denominator order; for both γ_a and γ_b functions. To investigate further the selection of gamma functions, the bode and Nyquist plots are plotted for gamma'a' and gamma'b' functions which are shown in figures below.

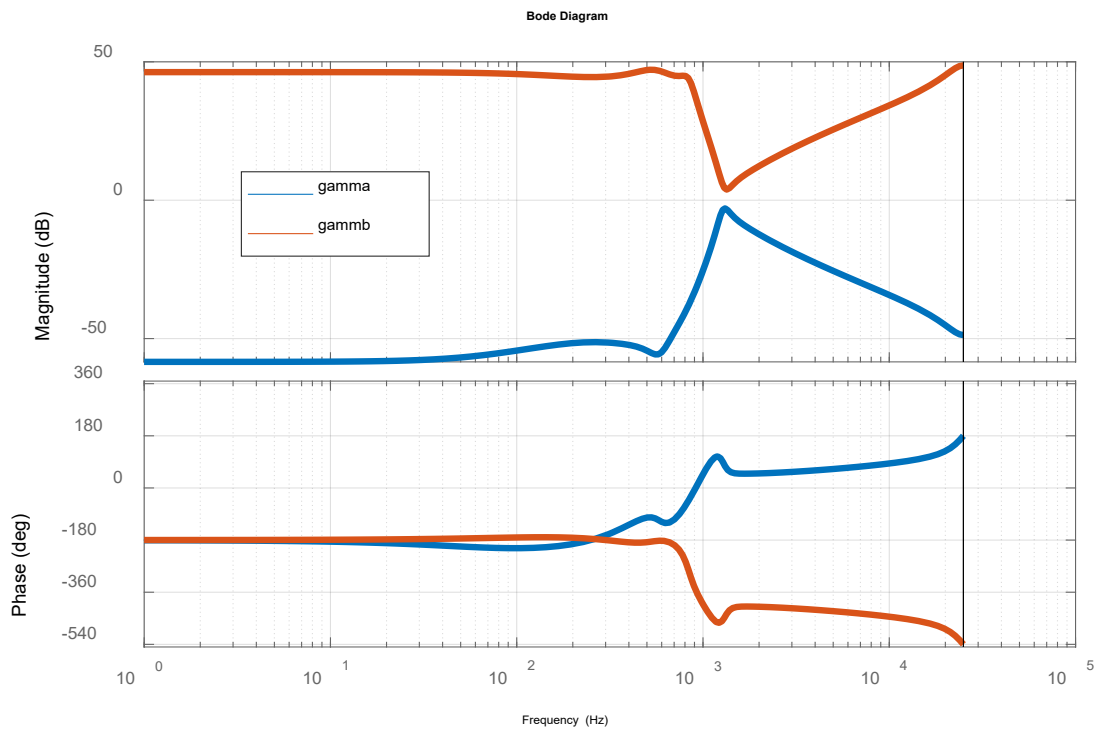


Fig. 4. 2 (a) Bode plot of Gamma Functions

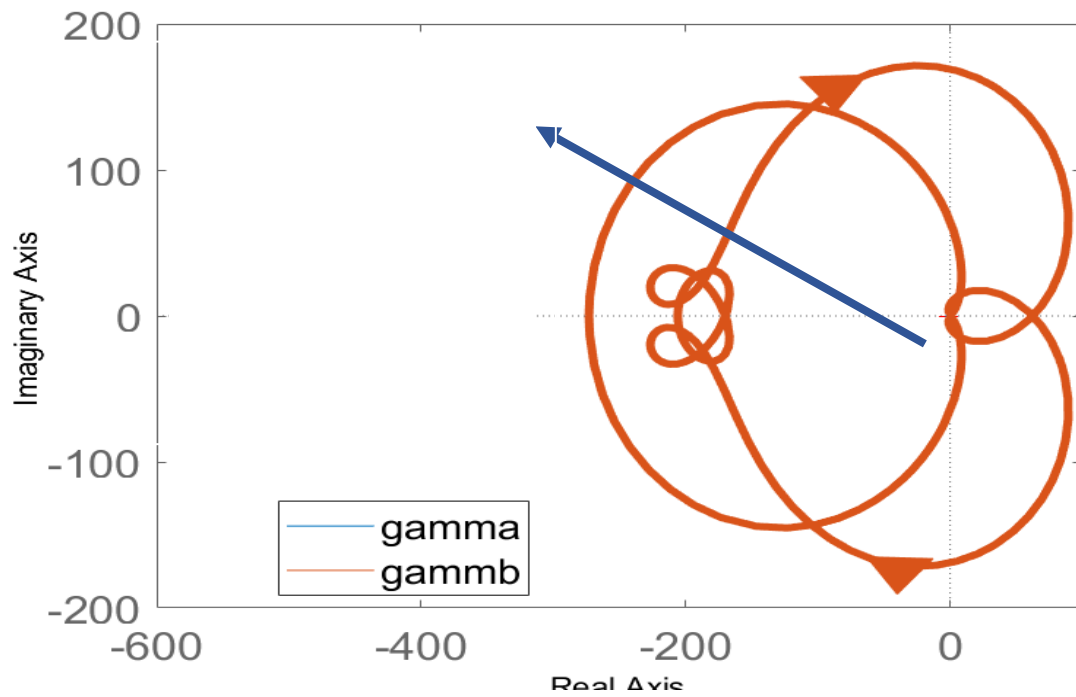


Fig. 4. 2 (b) Nyquist plot of Gamma Functions

It is evident from the above transfer function (γ_b) is having inappropriate gain and its Nyquist plot is also complex so the off-diagonal controller is not suitable for closed-loop operation for the proposed converter, on the other hand the responses of the (γ_a) is quiet good and the characteristics were found to be feasible so the diagonal controller were chosen for closed-loop operation for the proposed SIHBSTIC.

Understanding of the MSF gives a clear physical insight of the TIC systems and allows the possibility of establishing the design of diagonal stabilizing controllers for multivariable plants, even for highly coupled systems.

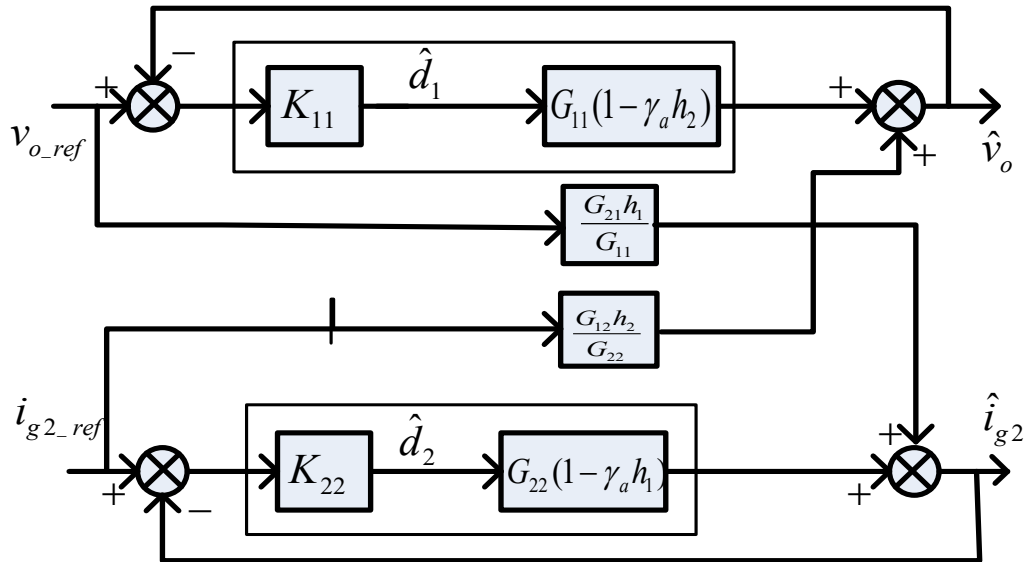


Fig. 4. 3 Channel representation of TIC system [52].

The interaction or cross-coupling between the channels can be evaluated through a transfer function. For instance, the influence of the j^{th} channel on the i^{th} channel is

$$u_i(z) = \frac{G_{ij}(z)}{G_{jj}(z)} h_j(z) r_j(z) \tag{4. 11}$$

$$G_{ci}(z) = \frac{G(z)K_i(z)}{(I+G(z)K_i(z))} \tag{4. 12}$$

If the channel is defined by eq. 4.9 indicates stability, then the closed-loop system described by eq. 4.12 is stable. Individual channel representations of the plant, along with interaction equivalent, are shown in Figs. 4.3 and 4.4.

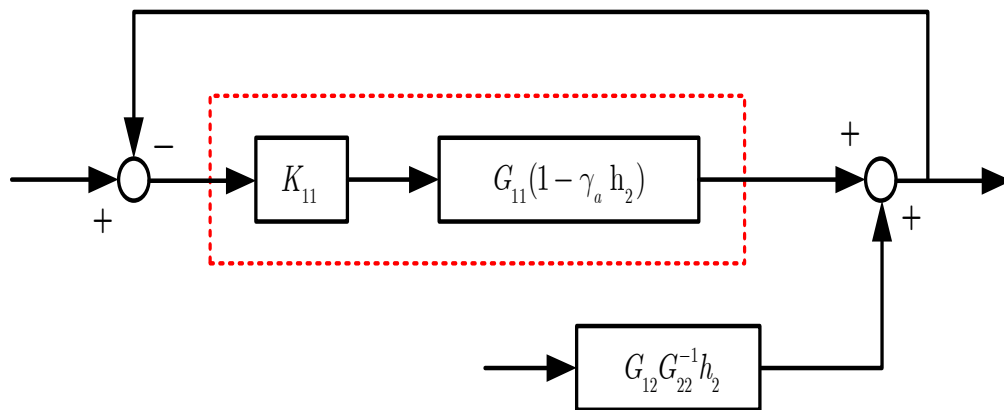


Fig. 4. 4(a) Equivalent channel-1 representation of the TITO control system [52].

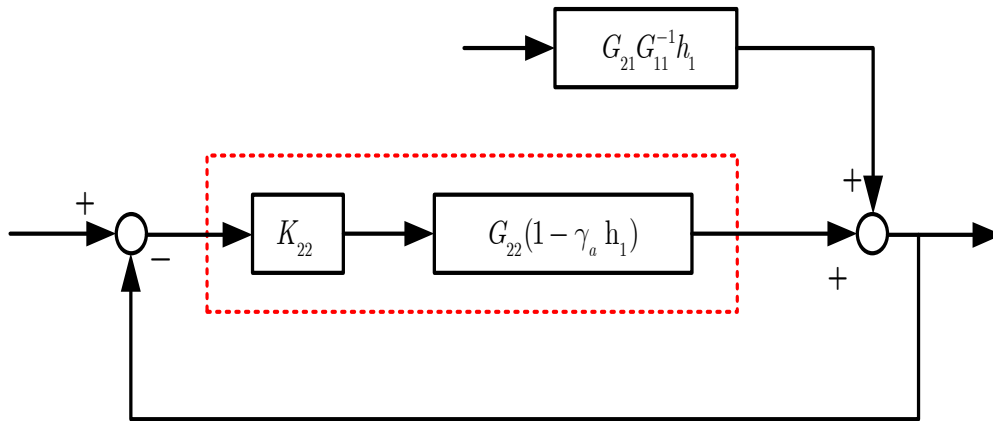


Fig. 4. 4 (a,b) Equivalent channel-1, 2 representation of the TITO control system [52].

The robustness of the channels can be established in terms of gain and phase margins as the Nyquist plot of the function $\gamma_a(z)h_i(z)$ does not enclose the critical point $(-1+j0)$. For the system under consideration, the controllers are designed using this approach. The Nyquist plots for MSF ($\gamma_a(z)$) and $\gamma_a(z)h_2(z)$ $\gamma_a(z)h_1(z)$ are shown in Fig. 4.5. In this figure, the Nyquist plot for all the three transfer functions does not enclose the critical point $(-1+j0)$. Hence, the respective channels, as well as the closed-loop system, are stable.

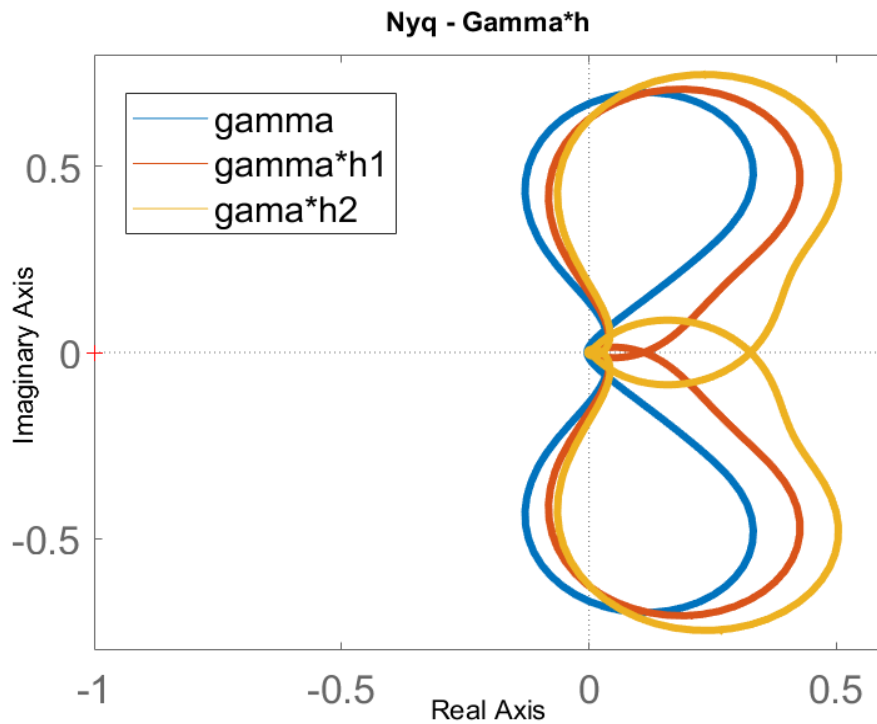


Fig. 4. 5 Structural robustness assessment for $\gamma_a(z)$, $\gamma_a(z)h_1(z)$, $\gamma_a(z)h_2(z)$.

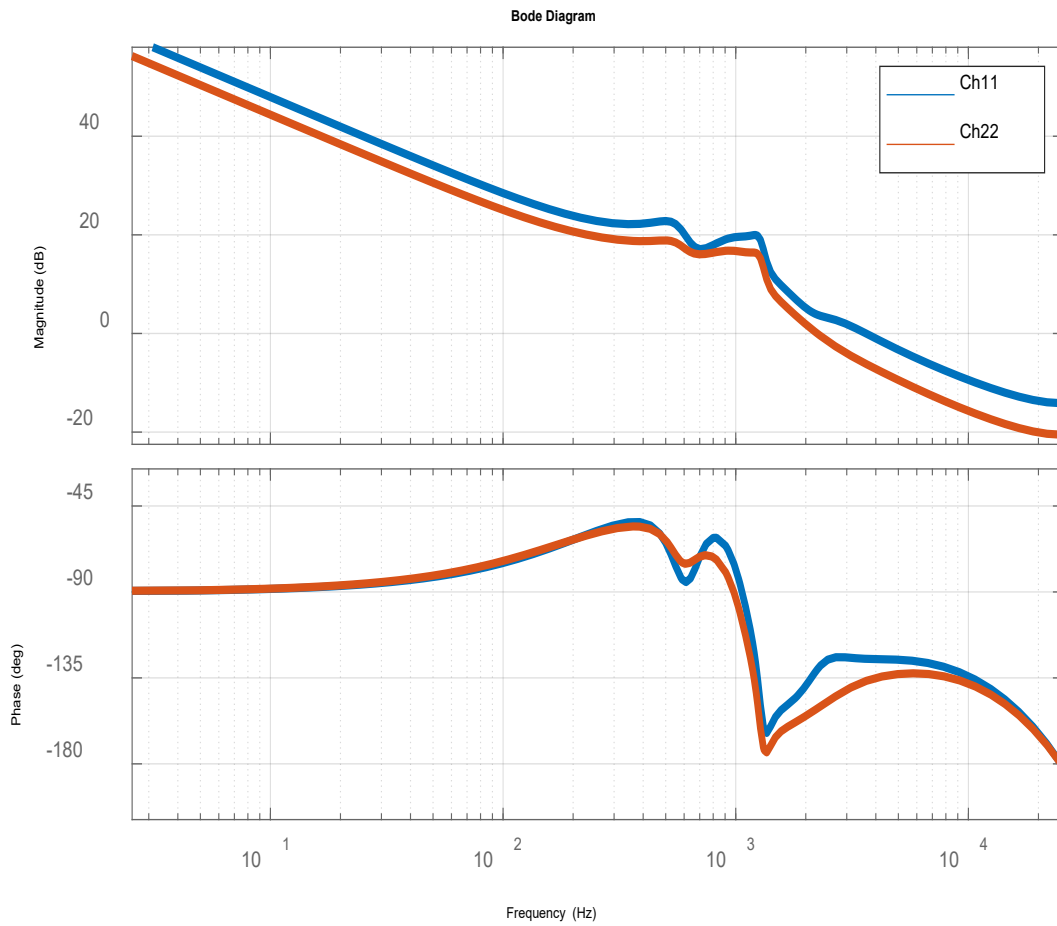


Fig. 4. 6 Bode plots of channel-1 and channel-2.

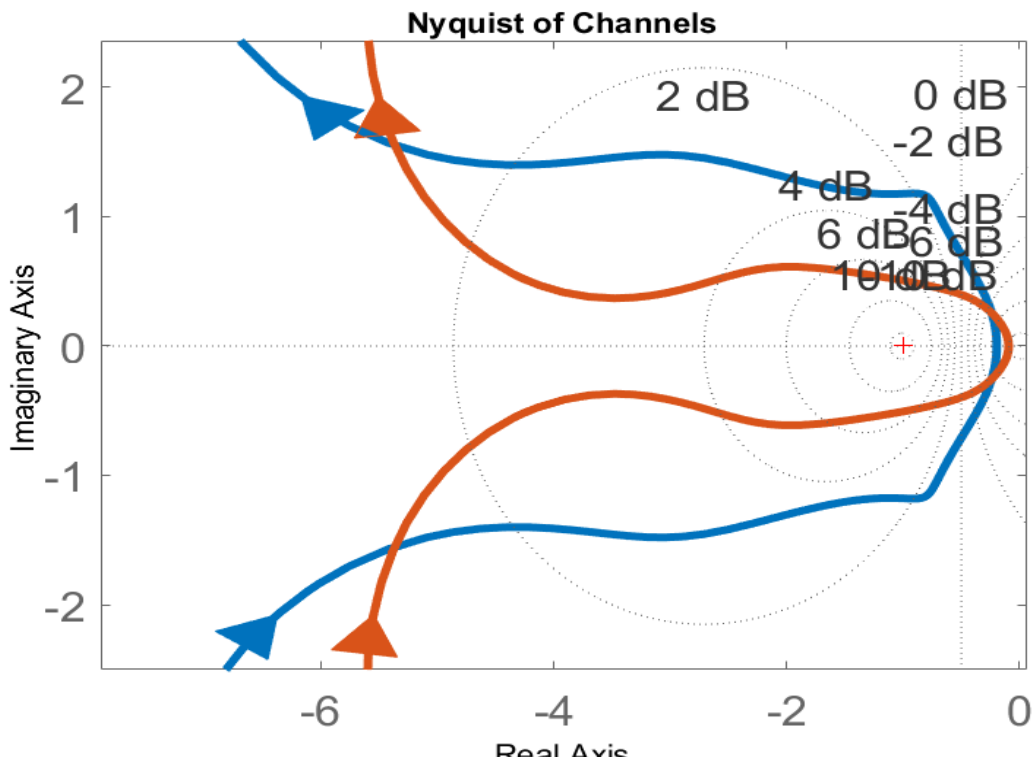


Fig. 4. 7 Nyquist plots for channel-1 and channel-2.

Making use of the above outlined ICD procedure and based on individual channel formulations, the controllers for the proposed system are designed and are given below.

$$K_{11} = \frac{0.32(z-0.9612)(z-0.7331)}{(z-1)(z-0.8611)} \quad (4.13)$$

$$K_{22} = \frac{0.15(z-0.7523)(z-0.8614)}{(z-1)(z-0.9322)} \quad (4.14)$$

Using these controllers, bode plots and Nyquist plots are plotted for the channels CH₁, CH₂, and loop gains and the corresponding gain and phase margins of the channels, as well as the loops, are tabulated in Table 4.2.

Gain and phase margins of two channels and two loops are tabulated in the Table 4.2.

Table 4. 2 Gain and phase margins and bandwidths of channels and loop gains.

Parameter	Channel-1	Channel-2
Gain margin (dB)	14.1	20.5
Phase margin (deg)	52.8	48.9

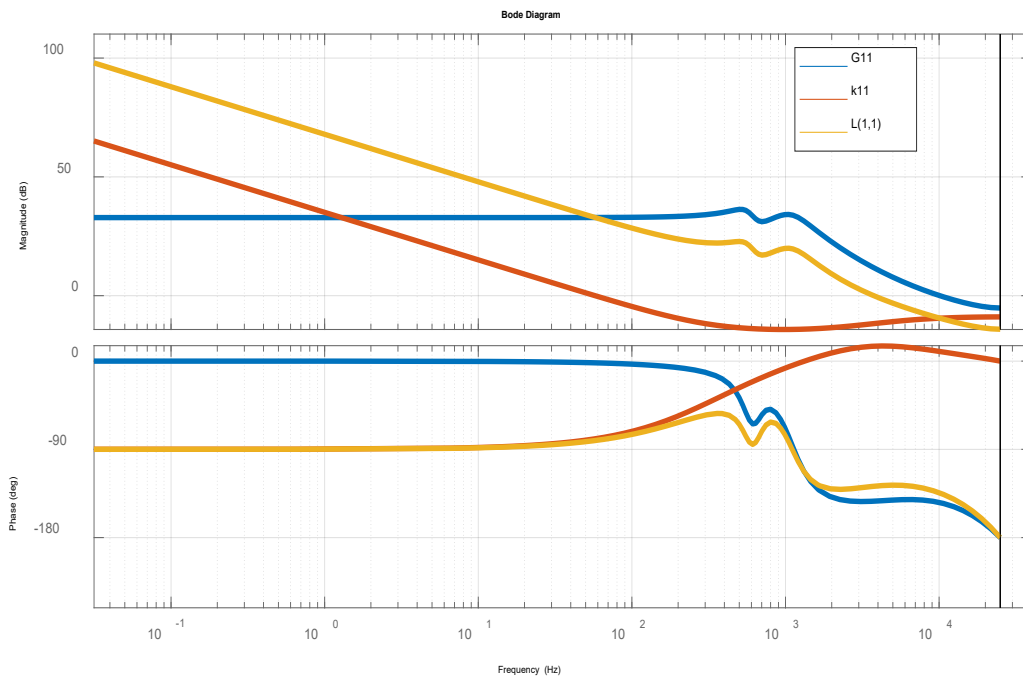


Fig. 4. 8 Bode plot of the G₁₁, K₁₁, loopgain-1

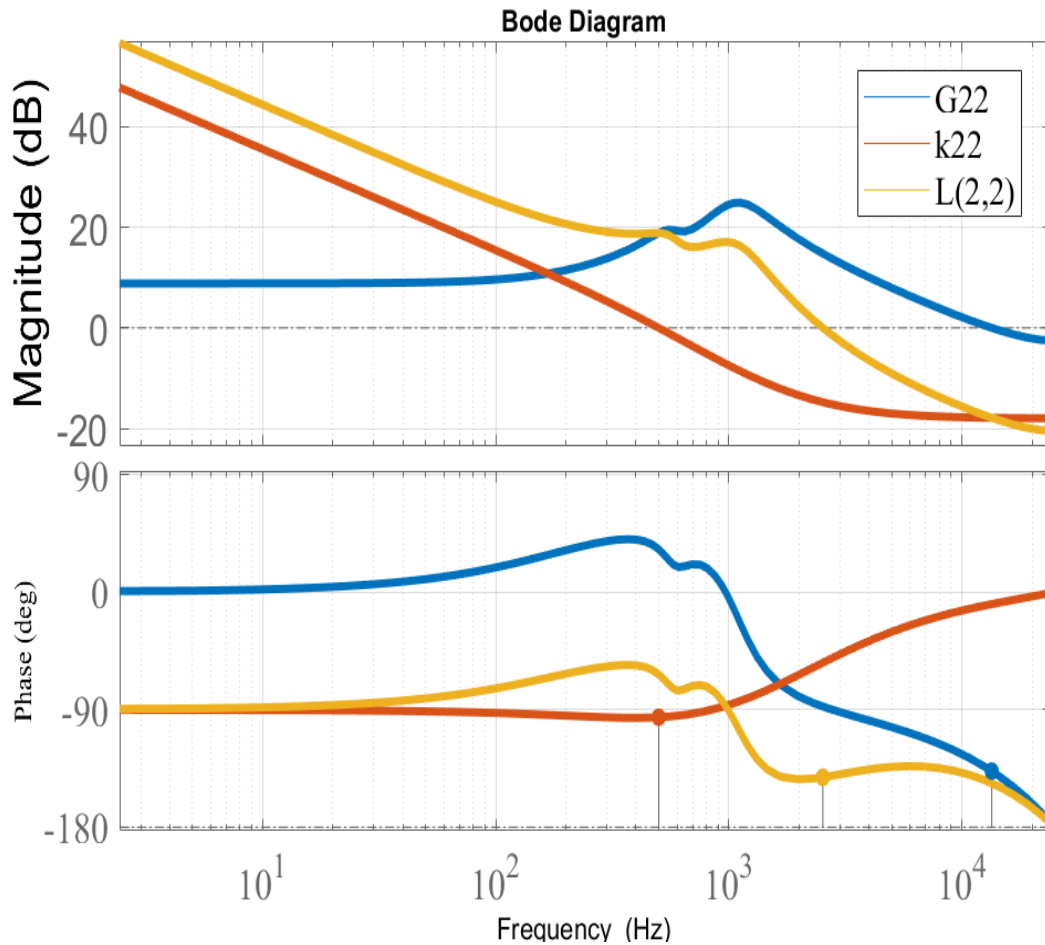


Fig. 4. 9 Bode plot of the G_{22} , K_{22} , loopgain-2

As the system is decentralized and the controllers are synthesized independently to one another, the two channels are treated as individual SISO systems, so the Table 4.2 gives the gain and phase margins of such individual channels, the gain and phase margins exhibited here are having values greater than the minimum specifications of gain margin greater than 6 dB and phase margin greater than 45 degrees.

In both cases, the controller is providing necessary compensations both in magnitude and phase to the corresponding loops. Further, the loop-gain frequency responses give evidence of the system stability.

4.3.2 Closed-loop TIC system stability analysis

The closed-loop system signal flow graph (SFG) is shown in Fig.4.10 which is of immense help in analyzing the closed-loop system stability. As the TIC's structure is complex, the block-

diagram approach may not provide quicker solutions while formulating the desired transfer functions [40].

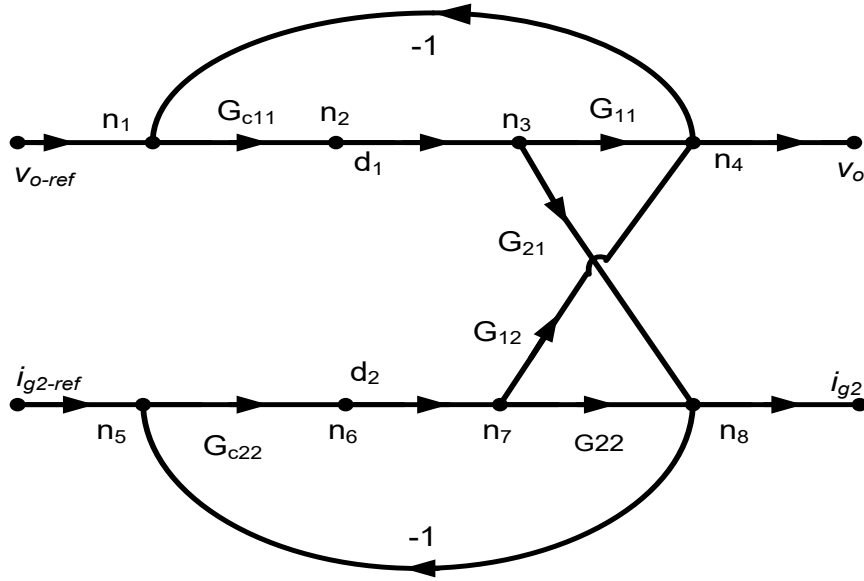


Fig. 4. 10. SFG of the closed-loop system with decentralized controllers.

Here the SFG method is used to obtain the below mentioned expressions (using Mason's gain formula) which are used to assess the closed-loop system stability.

$$v_o = Q_{11}v_{o_ref} + Q_{12}i_{g2_ref} \quad (4.15)$$

$$i_{g2} = Q_{21}V_{o_ref} + Q_{22}i_{g2_ref} \quad (4.16)$$

$$Q_{11} = \frac{[G_{c11}G_{11}(1 + G_{22}G_{c22}) - G_{12}G_{21}G_{c11}G_{c22}]}{\Delta} \quad (4.17)$$

$$Q_{12} = \frac{G_{12}G_{c22}}{\Delta} \quad (4.18)$$

$$Q_{21} = \frac{G_{21}G_{c11}}{\Delta} \quad (4.19)$$

$$Q_{22} = \frac{[G_{c22}G_{22}(1 + G_{11}G_{c11}) - G_{12}G_{21}G_{c11}G_{c22}]}{\Delta} \quad (4.20)$$

$$\Delta = [1 + G_{c11}G_{11} + G_{22}G_{c22} + G_{c11}G_{c22}(G_{11}G_{22} - G_{12}G_{21})] \quad (4.21)$$

For the closed-loop system to be stable, the roots of ‘ Δ ’ should lie within the unit circle. The pole-zero map for the system with decentralized controllers given in Fig. 4.11 satisfies the condition of poles lying within the unit circle.

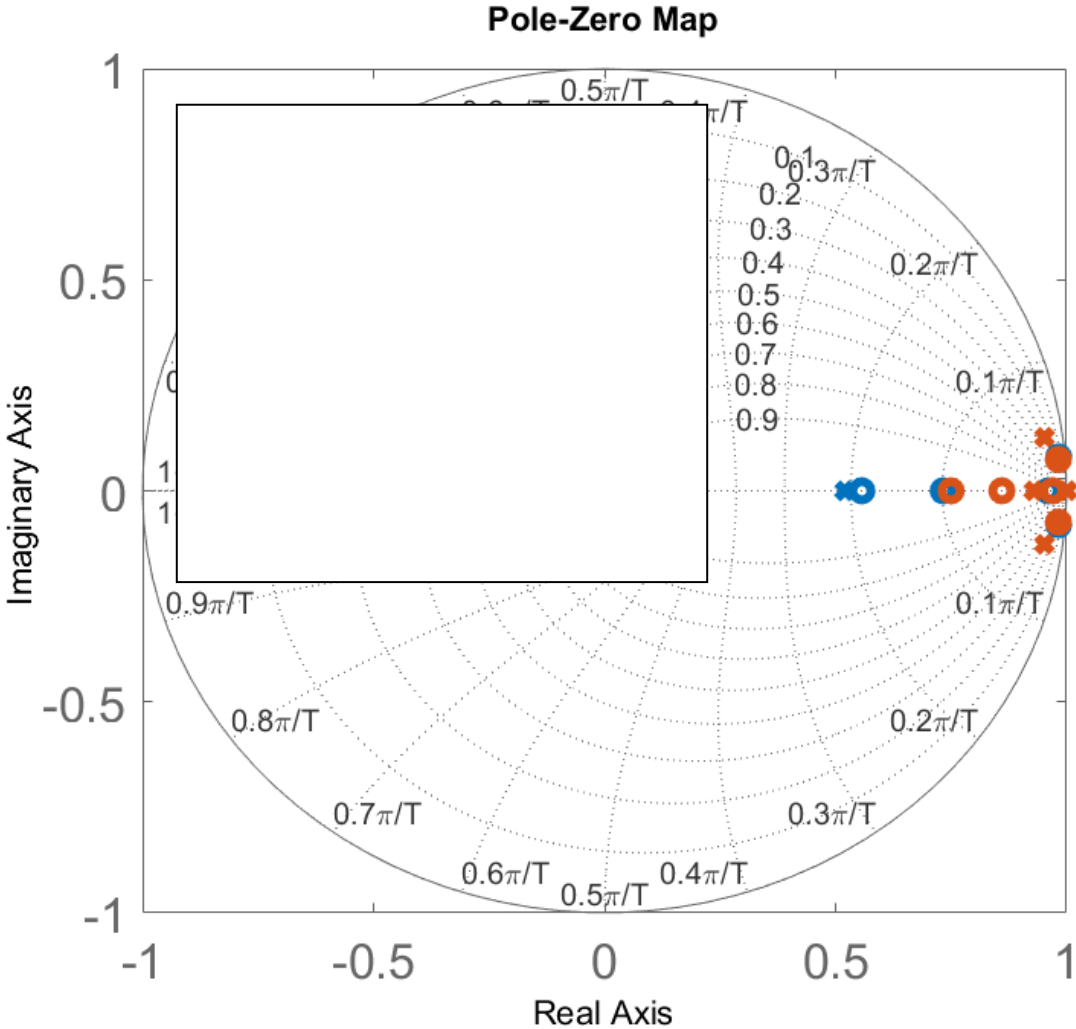


Fig. 4. 11. Pole-zero plot of closed-loop transfer functions with decentralized controllers.

From the step response (Fig. 4.12), it can be noticed that as the step responses of OFF-diagonal terms (interactions) are going towards zero while the step responses of diagonal terms are moving towards unity. The existence of the interactions is clearly seen in the step responses of OFF-diagonal terms which becomes more prominent in the initial stages while their influence later subsides. The magnitude of these step responses varies depending on the TIC system and the respective control strategy used. In order to mitigate the impact of OFF-diagonal terms which are responsible for delay time response, a centralized controller consisting of four controllers has

to be incorporated. Keeping in view of the above issues, the non-diagonal (full matrix) controller design method needs to be formulated and is discussed in the subsequent sections.

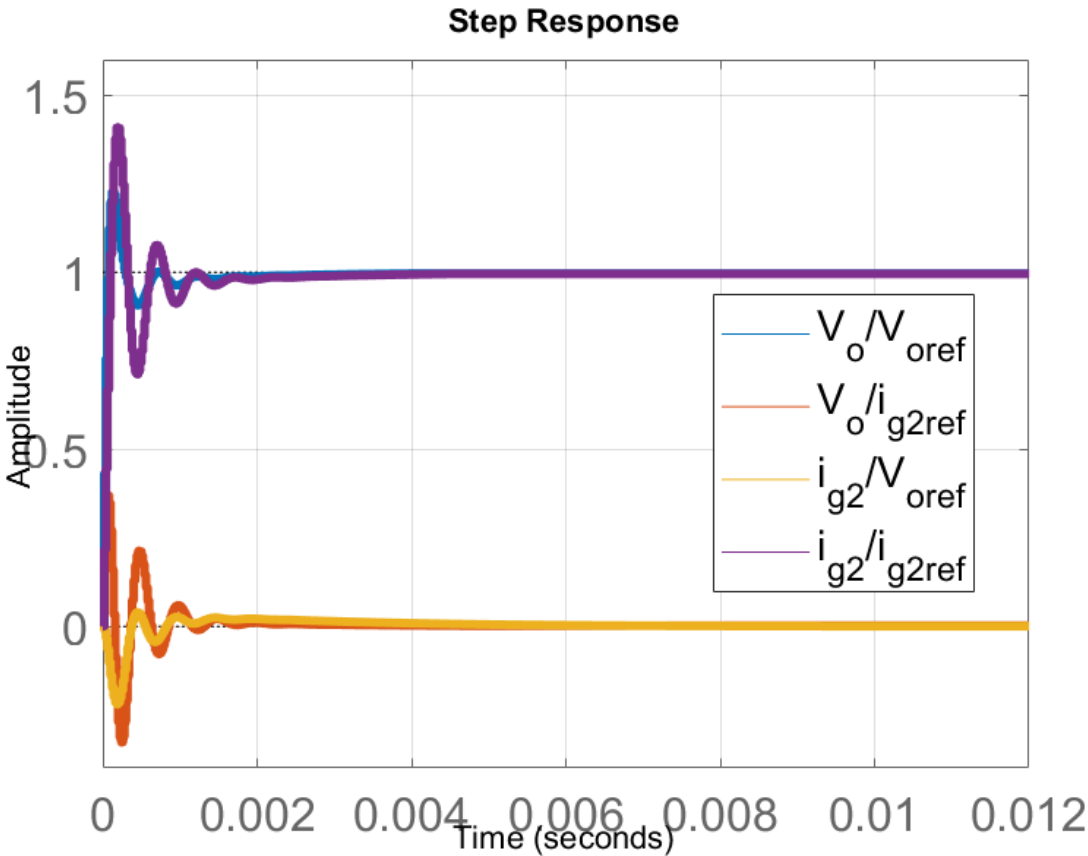


Fig. 4. 12. Step responses of the system with de-centralized controllers.

4.4 Quantitative feedback Controller design for TICs

The voltage variations at the input of the converter, the fluctuating loads at the output and parametric variations all of these collectively termed uncertainties that degrade the performance of the system and bring the destabilizing effects on the system. TICs operation always has to ensure the voltage and current regulation amidst various uncertainties need a robust control technique which ensures stable operation.

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ensure the voltage and current regulation amidst various uncertainties need a robust control technique which ensures stable operation.

The QFT is a robust control design technique is a transparent technique revealing the tradeoff between performance specifications and parameter uncertainties, it takes account the plant's quantitative information of the variability, robust specifications, amplitudes of approximate disturbance, requirements of attenuation, specifications of tracking performance etc., with an assurance to meet the rejection of the disturbances, ensuring stability, and robustness. QFT is Nichols chart-based design technique which gives fine parting of control problem and bids the two degrees of freedom structure where the feedback controller which tackles the disturbances and feedforward controller to deal with plant uncertainties which are either structure or unstructured. The block diagram for the MIMO QFT controller is shown in Fig. 4.7, for voltage and current mode control loops. QFT adapts the startup response and disturbance rejection response of the converter autonomous to each other ([58], [61-61], [71-74]). The literature reports about the QFT technique is used to design controllers for the buck and boost DC-DC converters mentioned in ([55], [49], [56], [57]...). The robust QFT controller design technique is applied for fourth-order boost converter and reported in [48], the QFT technique is aimed to design controllers for highly uncertain LTI systems, and it was reported that the same can be extended to MIMO systems [55]. So, an attempt was made to extend the work of applying the MIMO-QFT technique to TICs, which is one of the salient features of this thesis. The design and procedure are restricted to the MIMO QFT control design.

4.4.1 Sequential MIMO-QFT-Based Robust controller Design of QBSTIC

A fully populated matrix-based compensator offers more design flexibility in the regulation of MIMO systems, rather than classical diagonal controllers. SMQFT breaks the QBSTIC into 2-equivalent tracking and disturbance rejection single-loop equivalent systems. The SMQFT formulates the classical definition of MIMO specifications by designing a new set of loop-by-loop QFT bounds on the Nichols Chart with necessary and sufficient conditions [58]. The small-signal block diagram of MIMO closed-loop control of a 2DOF QBSTIC equivalent is shown in Figs.4.13. The block diagrams of Decoupled small-signal single-loop equivalents (DSSSLEs) of the QBSTIC along with the input and output disturbances for voltage loop and current loop are shown in the Figs. 4.14, 4.15.

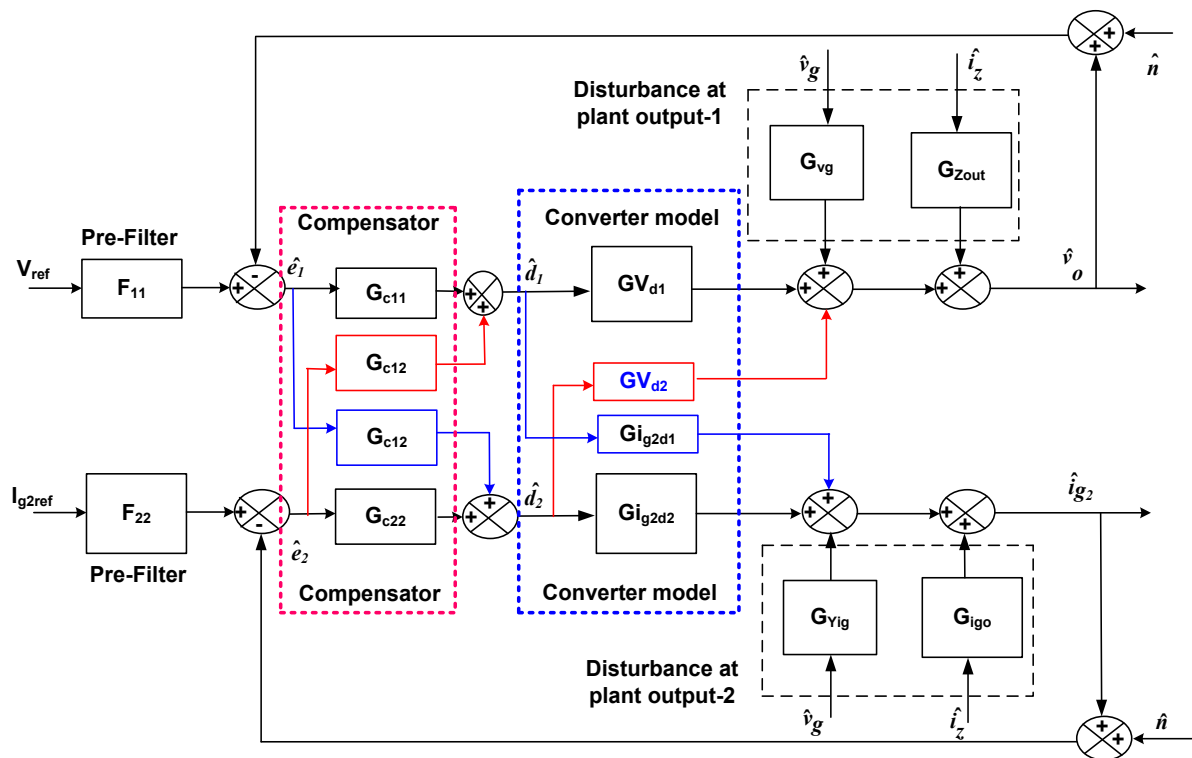


Fig. 4. 13 Small-Signal block diagram of closed-loop control of a 2DOF TITO QBSTIC.

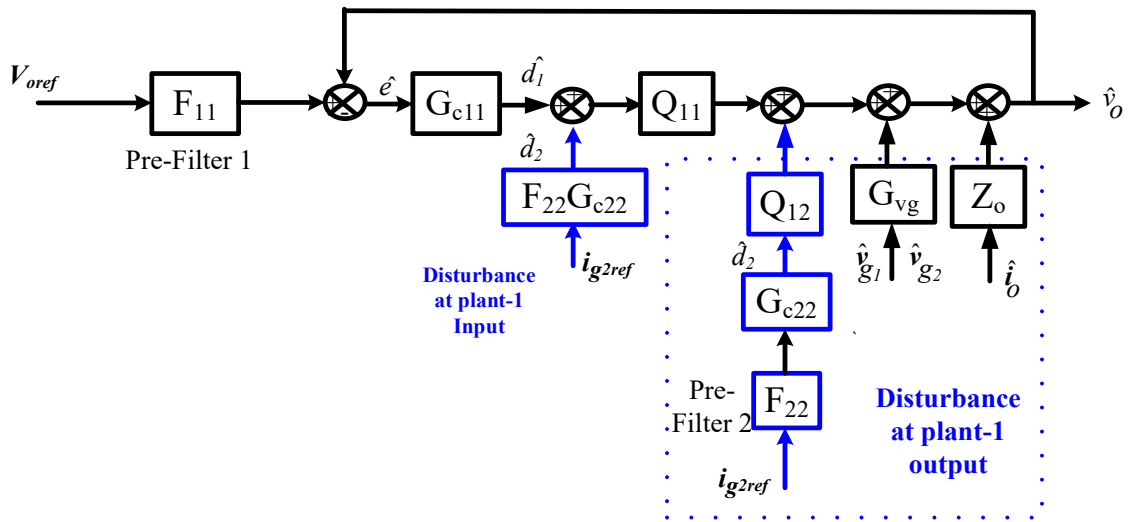


Fig. 4. 14 Decoupled small-signal SISO equivalents of loop-1 of QBSTIC, with internal and external disturbances.

In the above figure, the blocks shown in blue color are the disturbances of loop-2 coming and interacting with loop-1, while the disturbances of loop-1 interacting with loop-2 are shown in red color in the figure below.

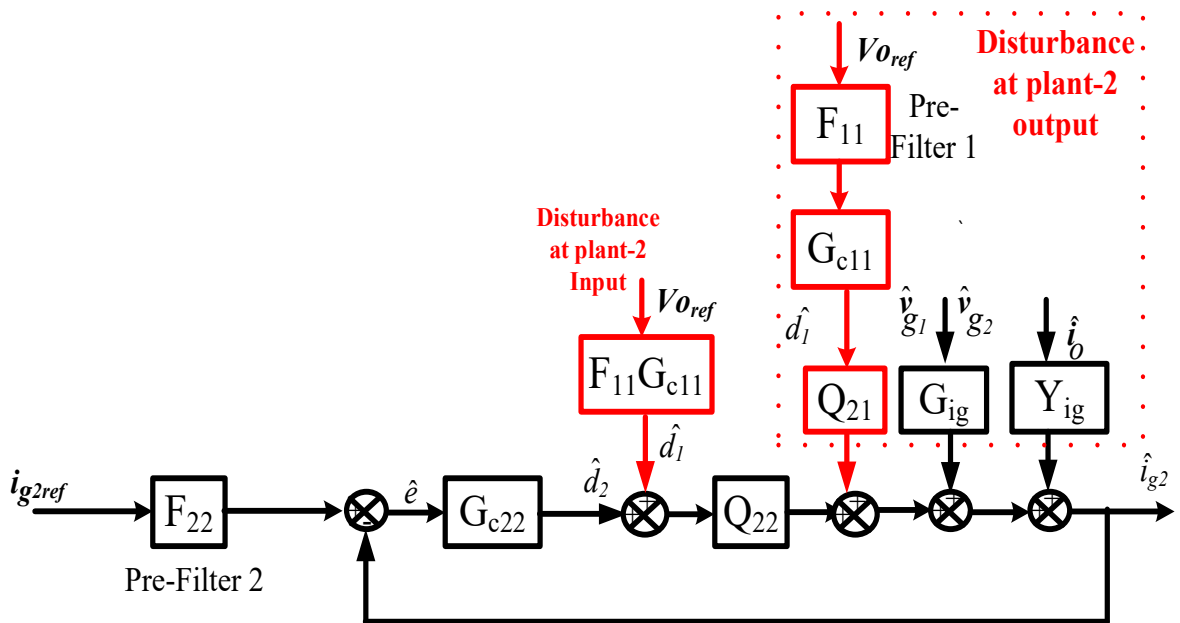


Fig. 4. 15 Decoupled small-signal single-loop equivalents (DSSLEs) of loop-2 of QBSTIC, with internal and external disturbances.

The design of controllers of a MIMO system poses specific challenges, contrary to SISO system; the MIMO systems comprise (i) internal-channels which link the inputs and outputs in more than one paths, thereby introduces challenging interactions (ii) the pairing problem (ii) gain of the system over a frequency range, etc. ([58], [60], [61]). To address the above issues proper control to output transfer functions are to be identified, for comfortable design, the following preliminary requirement is to be considered:

The $[G^*]$ matrix is the inverse of transfer function matrix which is indicated by $[P]$, and the $[Q]$ matrix is obtained by inverting each element of $[P]$. As an initial step, the inverse of the plant matrix $[Q]$ is obtained to check whether the plant is singular. If the plant is singular, the system is uncontrollable, so this condition is checked first.

Table 4. 3 Plant, Inverse Plant and Effective Plant transfer functions

Matrix	Description
$[G] = \begin{bmatrix} G_{11}(z) & G_{12}(z) \\ G_{21}(z) & G_{22}(z) \end{bmatrix} = \begin{bmatrix} GV_{d1} & GV_{d2} \\ GI_{g2d1} & GI_{g2d2} \end{bmatrix}$	The plant transfer function Matrix represented in Eq. 4.2
$[P] = [G]^{-1}$	The inverse of Plant transfer function matrix
$[Q] = \begin{bmatrix} Q_{11} & Q_{12} \\ Q_{21} & Q_{22} \end{bmatrix} = \begin{bmatrix} 1/p_{11}^* & 1/p_{12}^* \\ 1/p_{21}^* & 1/p_{22}^* \end{bmatrix}$	The effective plant transfer function Matrix $q_{ij} = \frac{1}{p_{ij}} = \frac{\det[P]}{\text{adj}_{ij}[P]}$

$$[Q] = \begin{bmatrix} Q_{11} & Q_{12} \\ Q_{21} & Q_{22} \end{bmatrix}; \text{ here } Q_{11} = QV_{d1}; Q_{12} = QV_{d2}; Q_{21} = QI_{g2d1}; Q_{22} = QI_{g2d2}. \quad (4.22)$$

Where

$$Q_{11} = \frac{0.1256z^4 - 0.4689z^3 + 0.6539z^2 - 0.4037z + 0.09303}{z^5 - 4.947z^4 + 9.789z^3 - 9.686z^2 + 4.792z - 0.9485} \quad (4.23)$$

$$Q_{12} = \frac{0.9462z^4 + 3.531z^3 - 4.925z^2 + 3.041z - 0.7007}{z^5 - 4.641z^4 + 8.574z^3 - 7.872z^2 + 3.589z - 0.6491} \quad (4.24)$$

$$Q_{21} = \frac{0.835z^4 - 3.116z^3 + 4.346z^2 - 2.683z + 0.6184}{z^5 - 4.923z^4 + 9.702z^3 - 9.565z^2 + 4.718z - 0.9316} \quad (4.25)$$

$$Q_{22} = \frac{1.317z^4 - 4.916z^3 + 6.856z^2 - 4.233z + 0.9755}{z^5 - 4.718z^4 + 8.897z^3 - 8.378z^2 + 3.94z - 0.7398} \quad (4.26)$$

Based on matrix [Q] in eq. (4.22) and the corresponding transfer functions are presented from eq.s 4.23 to 4.26, the verification of diagonal dominance plot, singular values plot, and condition number plots shown in Figs. 4.16 to 4.18 are plotted.

(i) Diagonal Dominance of TFM: A check is performed to observe the Diagonal Dominance (DD) of TFM of QBSTIC the magnitude of the product of the diagonal terms and the off-diagonal terms are obtained and the bode plot is plotted. Here, P11P22 (blue) is the product of the magnitude of diagonal elements of TFM-[G], and the off-diagonal product is P12P21 (red), it is clear that for all the frequency range the diagonal term product is higher than the off-diagonal term product.

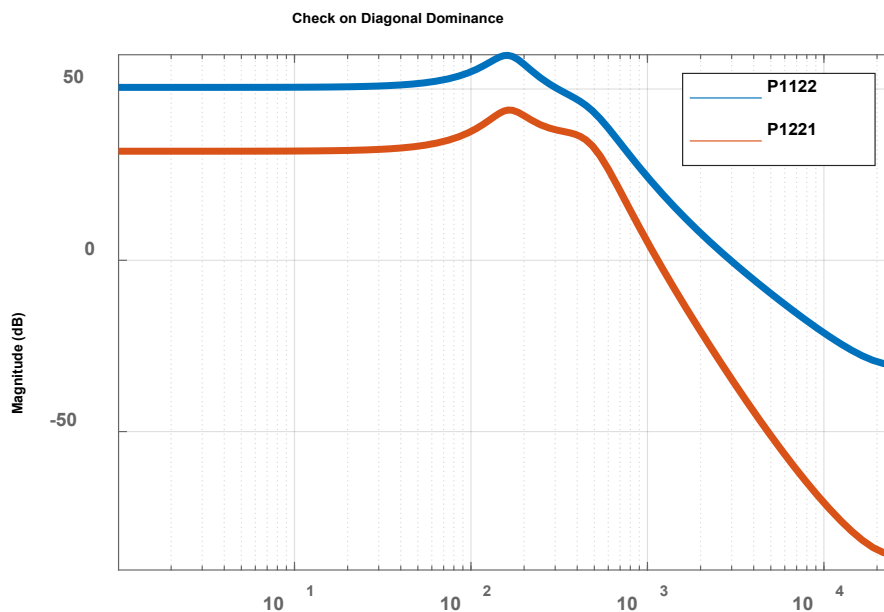


Fig. 4. 16 Verification of diagonal dominance condition

(ii) The gain of QBSTIC: Based on [Q] given in eq. 4.22, and its individual transfer functions mentioned in eq. 4.23 to 4.26, the nominal plant capacity of the channels for signal transmission is needed. Singular Value Decomposition (SVD) provides us the information of maximum and minimum gains of the TFM over the frequencies of interest, the SVD of QBSTIC is plotted and the range of gain variation for a frequency of 1Hz to half of switching frequency 25KHz is shown in Fig. 4.15.

If system is a single-input, single-output (SISO) model, then the singular value plot is similar to its Bode magnitude response, only one curve will be indicated. If system is a multi-input, multi-output (MIMO) model with ‘Nu’ inputs and ‘Ny’ outputs, then the singular value plot shows minimum (Nu,Ny) lines on the plot corresponding to each singular value of the frequency response matrix. As the control structure of TIC is of two input and two output type, two lines are shown in the log magnitude plot.

In log frequency scale, the plot shows two branches for models with real coefficients, the one shown above is the variation of real coefficients of vectors of plant moving in clockwise rotation (upper curve), and another for counterclockwise rotation (lower curve).

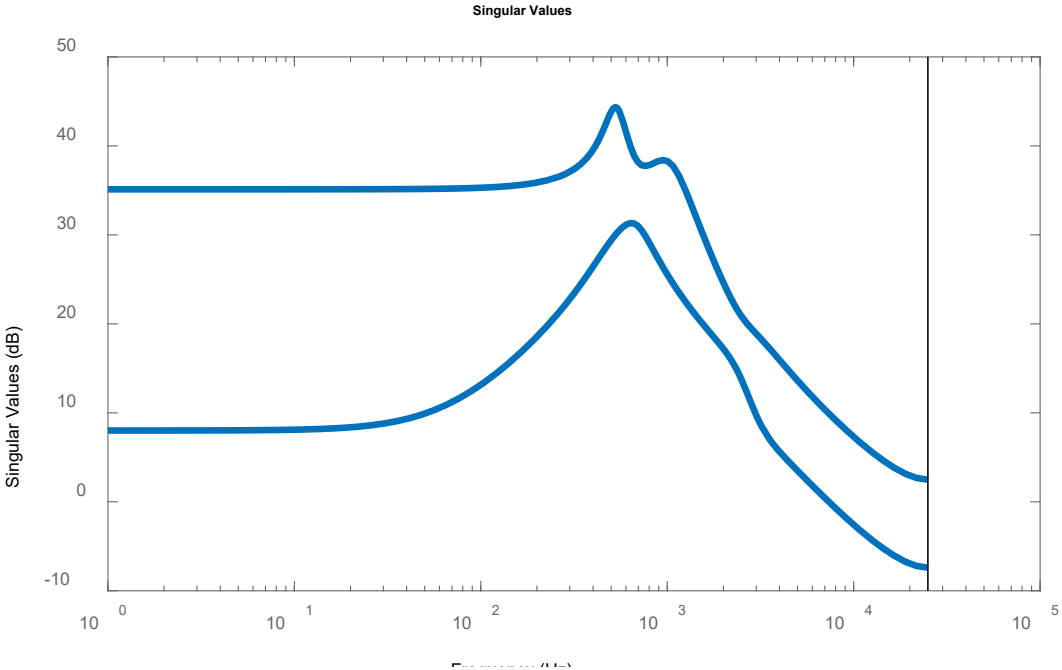


Fig. 4. 17 Singular values of TFM

(iii) Disturbance condition number variation: All the loops of the system are not equally affected by disturbances; some may be rejected easily and others maybe not [62].

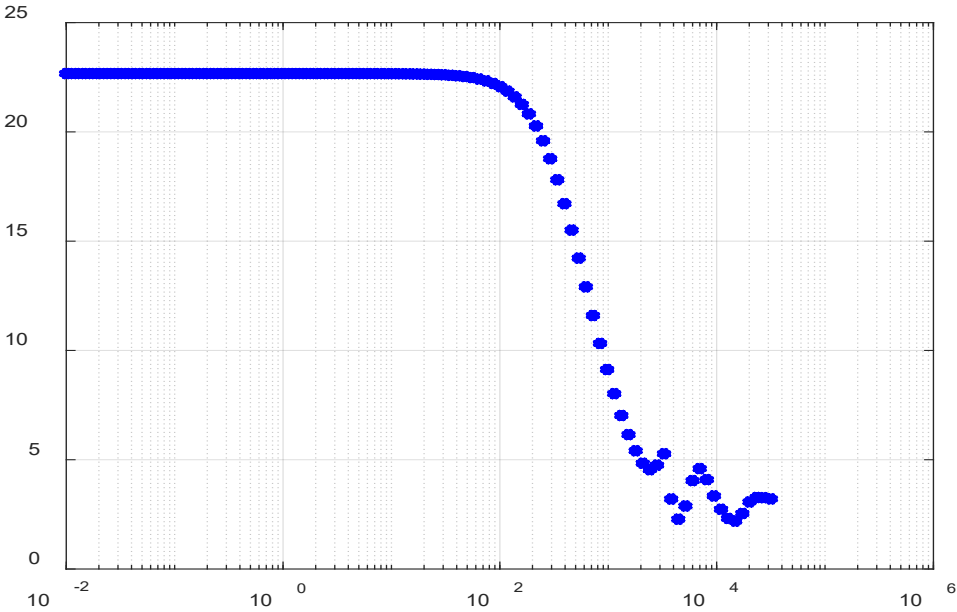


Fig. 4. 18 QBSTIC Condition Number

The Disturbance Condition Number (DCN) measures the change of the output magnitude for a small variation in input excitation, the higher the DCN indicates that the systems are ill-conditioned. The DCN variation is plotted and is shown in Fig. 4.16. The DCN of QBSTIC is 8dB which is found to be low [63], [64].

(iv) The upper limit on PM: while designing a controller, choosing an inappropriate order of loop arbitrarily, may result in a non-existent of solution [62], which may occur if the solution process is based on satisfying the upper limit of phase margin frequency for both loops, the loop having smallest bandwidth is chosen as the first loop. The diagonal elements of [Q] which are the inverse of [G], are plotted as shown in Fig. 4.19, so $Q_{11}=1/P_{11}^*$ is identified as the first loop (voltage loop). The lower bandwidth element of the inverted TFM is the one with broader BW in the original plant TFM. In the case, if Q_{22} was found to be of lower BW, Q_{11} is to be replaced by Q_{22} .

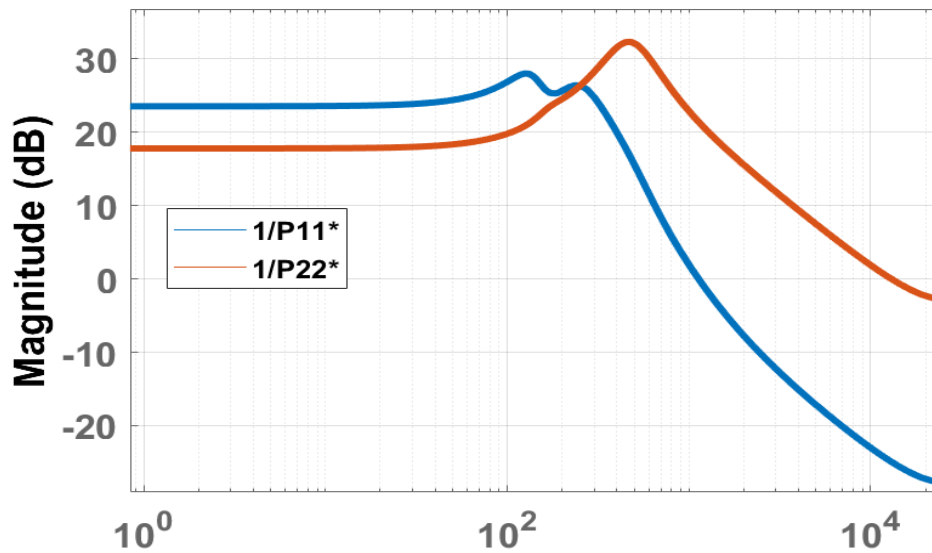


Fig. 4. 19 Bandwidth Constraint

By performing the above checks, the elements of TFM are fixed, and a comparative overview of variation of system gain, and the reflection of the effect of source disturbance on the system is roughly known. The control pair confirmation is obtained, which helps design the QFT MIMO controller, discussed in the next section.

4.4.2 Controller design procedure

A fully populated matrix-based compensator offers more design flexibility in the regulation of MIMO systems, rather than classical diagonal controllers. SMQFT breaks the QBSTIC into 2-equivalent tracking and disturbance rejection single loop systems shown in Figs. 4.12, 4.13. The SMQFT performs the design of a controller on a loop-by-loop basis for de-coupled single loop equivalents, the constraints, and specifications of SISO for each loop are applied. When the loop controllers attain equilibrium among the individual loops, the interaction present between the loops just becomes a trade-off. The flow chart of the SISO design procedure is shown in Fig. 4.21, and that of the MIMO design procedure is shown in Fig. 4.22, the decoupled SISO equivalents of the QBSTIC along with the input and output disturbances for voltage and current loops are shown in Figs. 4.12 and 4.13.

The QFT control design works on the frequency response converting the constraints placed on the plant into what is called bounds. It takes the quantitative information of plant's uncertainty, tracking performance, disturbance amplitude and its attenuation into account, in order to synthesize the controller. Initially, all the pre-filters and controllers are assumed as unity to proceed to design. The stability of the controller is ensured loop-by-loop; the diagonal controllers are designed first and, in a sequence, the other column controllers are designed from their respective diagonal controllers shown in the figure below.

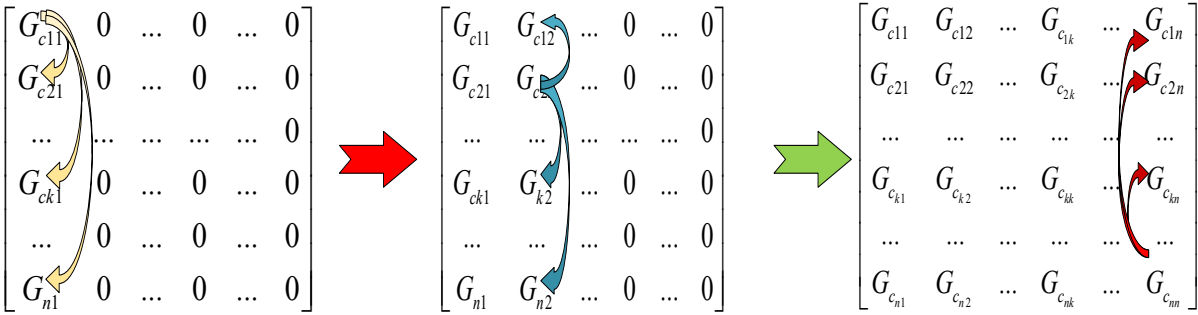


Fig. 4. 20 Sequential controller design methodology [61]

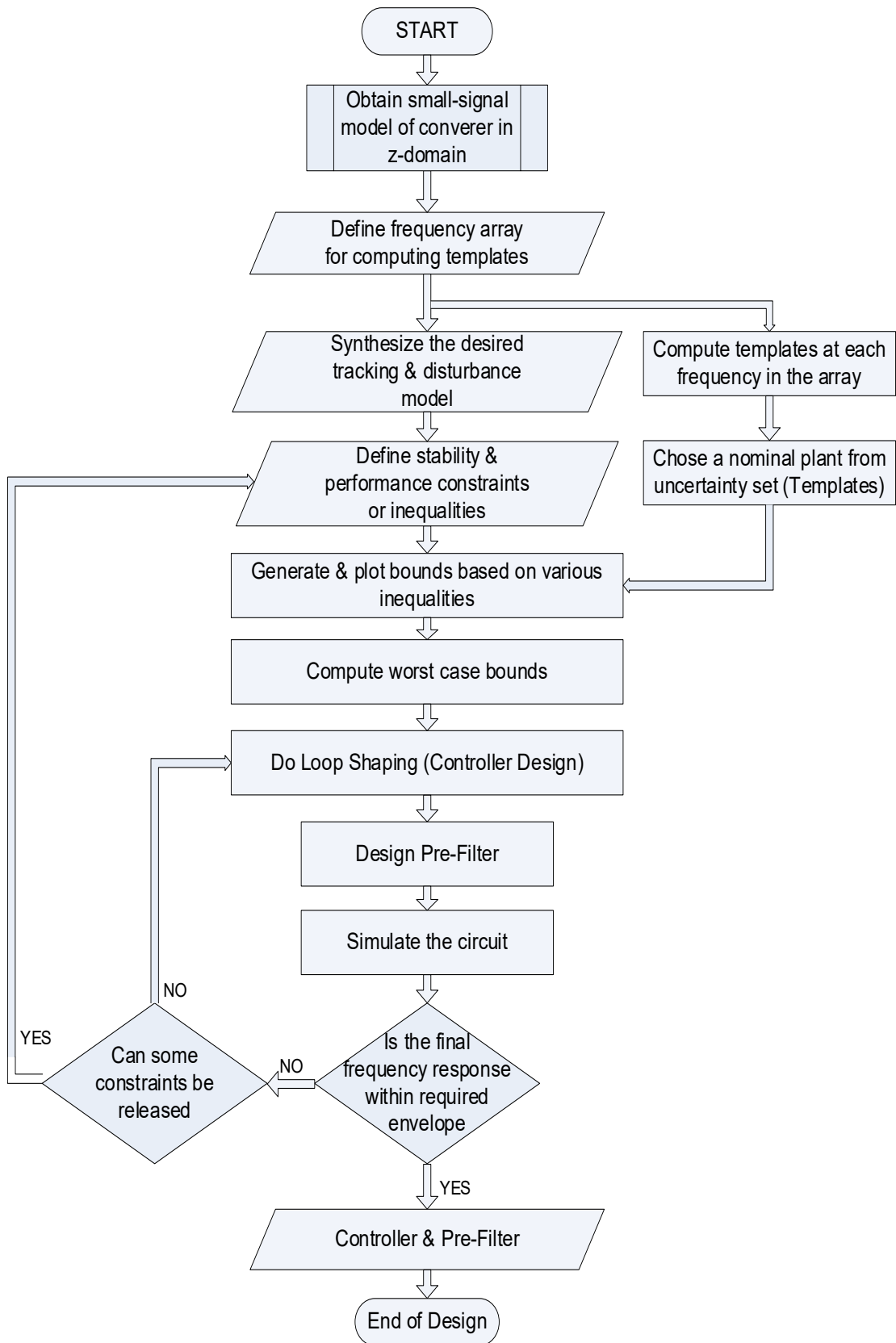


Fig. 4. 21 Flowchart of implementation of SISO QFT [65]

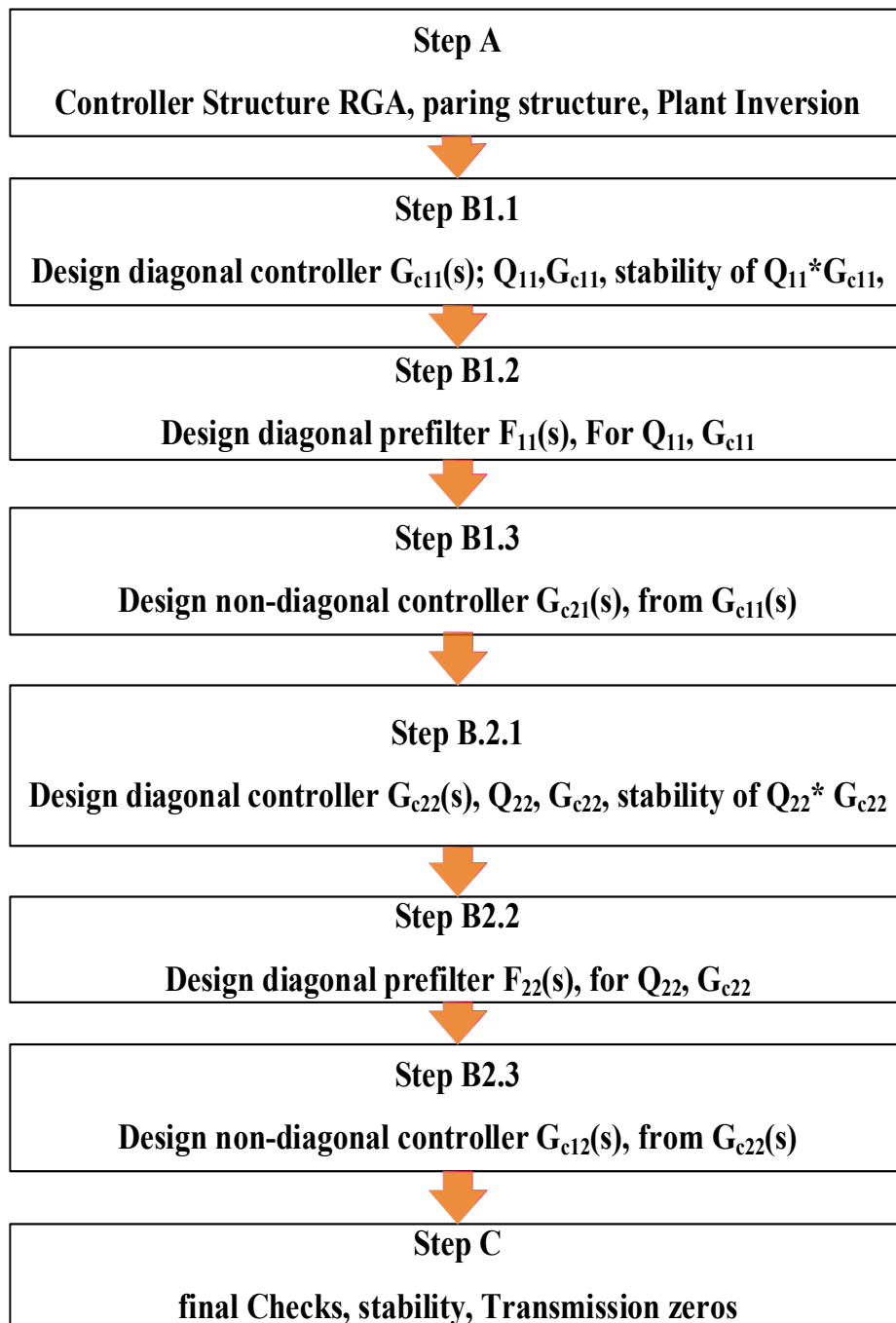


Fig. 4. 22 Flowchart of implementation of SMQFT

4.4.3 Diagonal Controllers design of QBSTIC

The ratings mentioned in Table 2.3 and Table 2.10 and the small-signal transfer functions obtained from chapter-3 are used to design the controllers. In order to generate the uncertainty templates, the source, load Resistor 'R', are varied, as listed in Table 4.4 below.

Table 4. 4 Uncertainty set

Parameter	Rating
V_{g1}	36V±10%
V_{g2}	12V±10%
R	10Ω±50%

The duty ratio d_1 is varied from 0.6 to 0.74 and the duty ratio-2 is obtained by solving the voltage

gain expression of QBSTIC expressed by $d_2 = \frac{V_o - V_{g1}d_1^2}{V_o + V_{g2}}$.

The uncertainty mentioned in the above set is used to observe the variation of all the small-signal transfer functions listed in Table 3.1 and the variations are stored as an array in the MATLAB. To conduct the design process the toolboxes mentioned in [66], [67] are used combinedly at various stages of simulation of controllers.

After decoupling the MIMO system into DSSSLEs, the procedure of synthesizing the SISO controllers is used in the process of designing the diagonal controller first and later using the Sequential method the off-diagonal controllers are designed.

4.4.3.1 Selection of frequency array (FA)

To complete the controller design, it is crucial to choose the appropriate FA. FA can be chosen from plant templates for parametric variations and contain the frequencies at which disturbances affect the TIC output. The following FA is selected for QBSTIC.

$$w=2*\pi*[1\ 10\ 50\ 100\ 200\ 300\ 400\ 500\ 700\ 800\ 1e3\ 1.5e3\ 2e3\ 5e3\ 10e3\ 20e3\ 25e3];$$

4.4.3.2 Selection of Nominal Plant

QFT design is carried out using the simple control to output transfer function corresponding to the rated source voltage and load value. Based on the variation in these parameters, the nominal transfer function is obtained and used for loop shaping.

4.4.3.3 Uncertainty Template Generation

The uncertainty templates represent the gain and phase variations of all the plants TFs at a particular frequency. These templates are plotted at all the frequencies of FA. The templates for stipulated variation in V_g and R for QBSTIC are plotted in Fig. 4.23. Where it is seen that the shape of the templates at some frequencies is disturbed thereby indicating that the effect of uncertainties is more dominating at those frequencies. The uncertainty templates for Q12, Q21 and Q22 are plotted in Figs. 4.24, 4.25, 4.26, respectively.

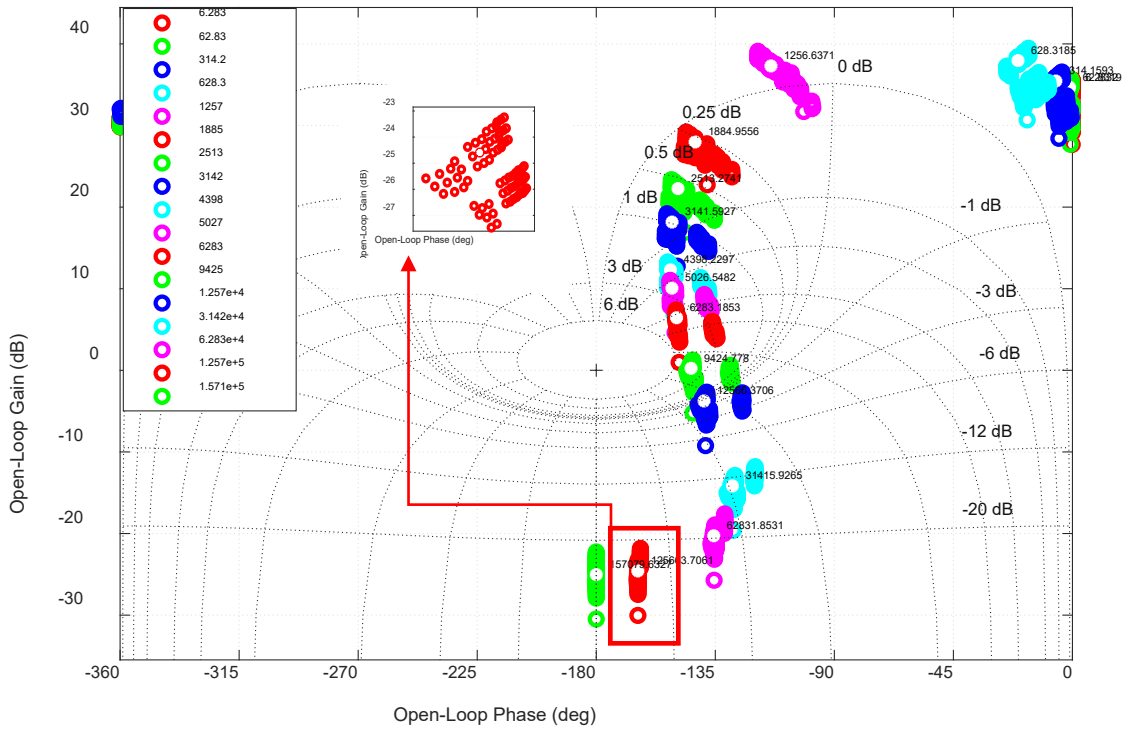


Fig. 4. 23 Uncertainty Template Plot of Q₁₁

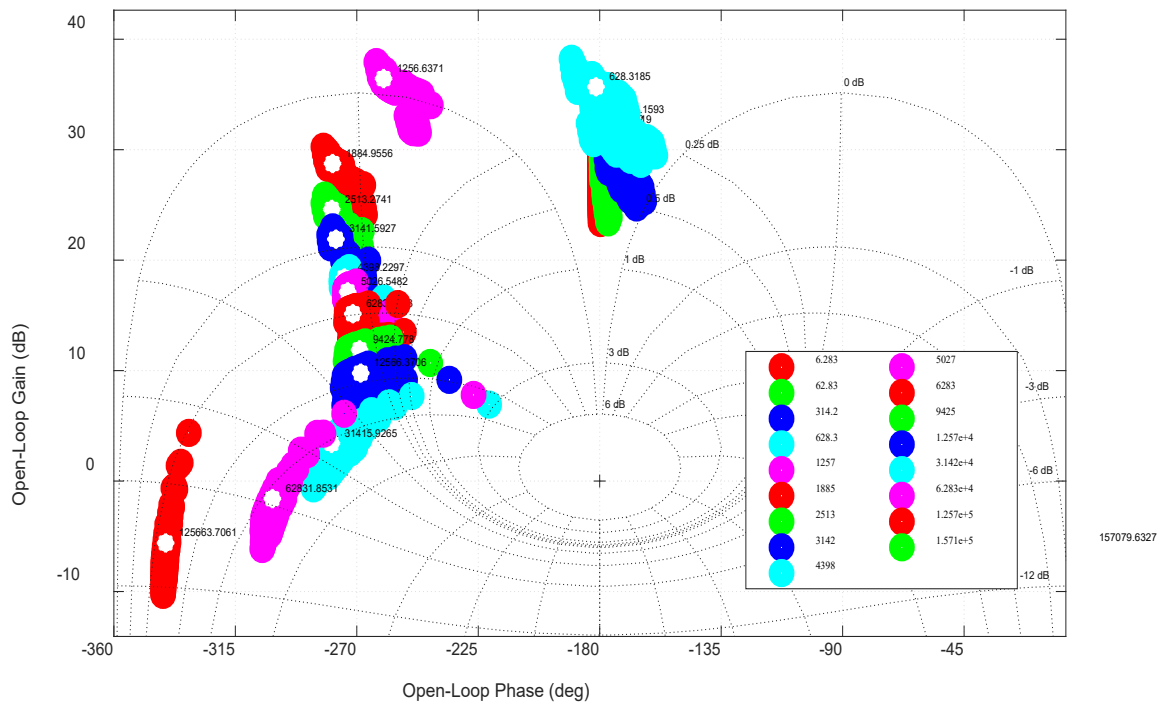


Fig. 4. 24 Uncertainty Template Plot of Q₁₂

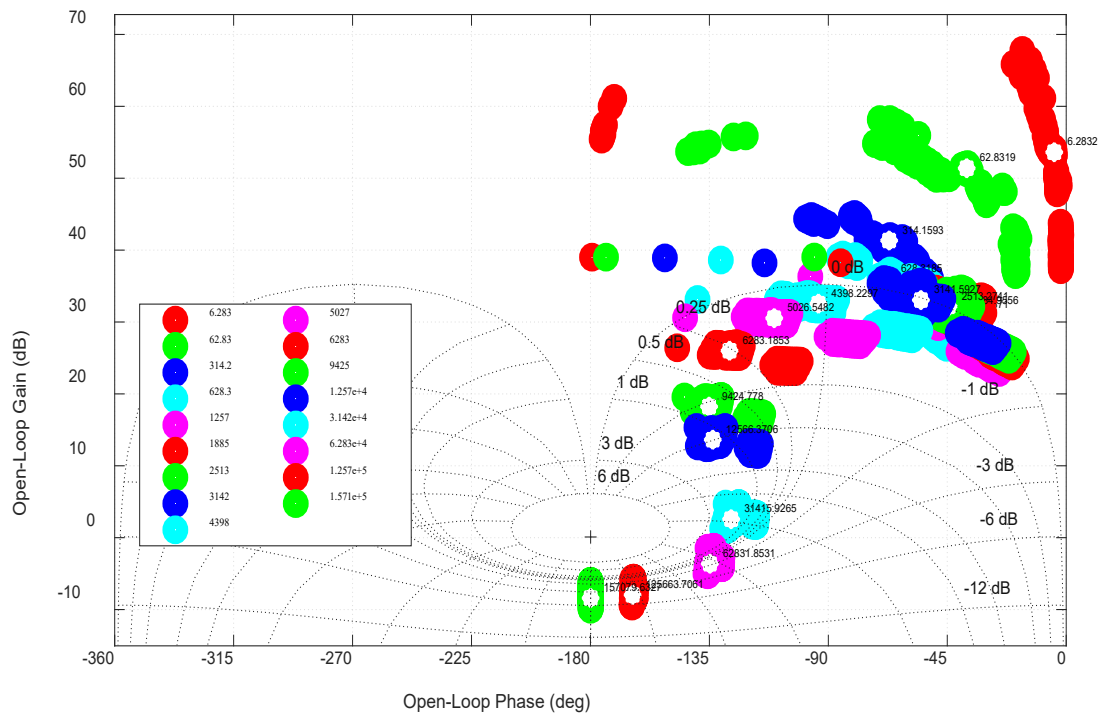


Fig. 4. 25 Uncertainty Template Plot of Q₂₁

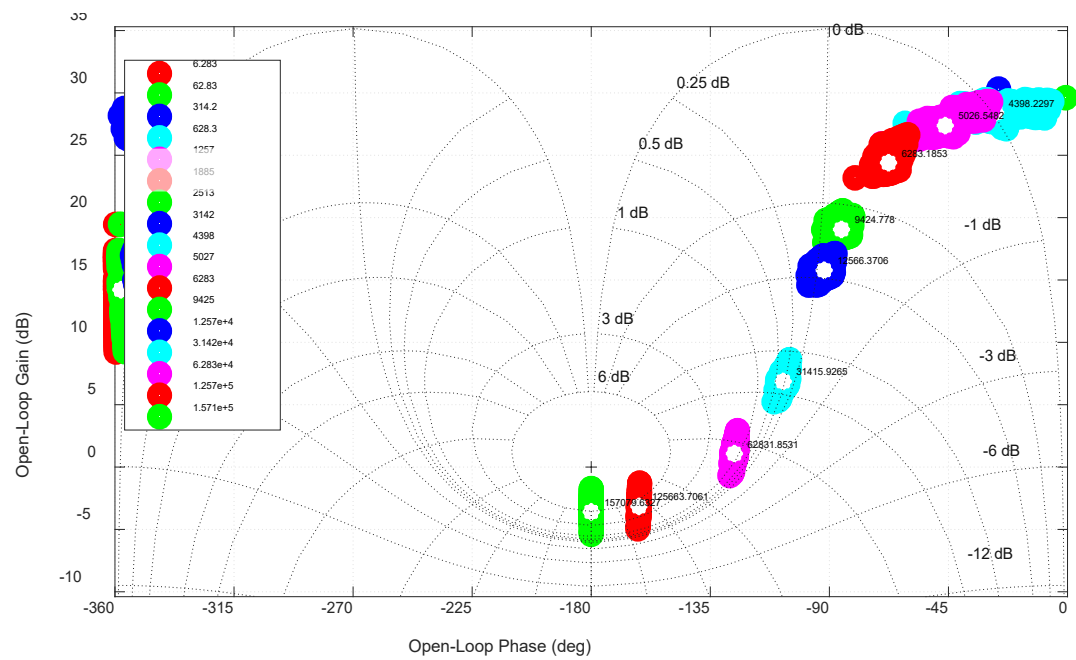


Fig. 4. 26 Uncertainty Template Plot of Q₂₂

It is observed that the templates generated from the control-to-output transfer functions of Q₁₁ and Q₂₂ indicate the lower effect of uncertainties as compared to that of Q₁₂ and Q₂₁.

4.4.3.4 Control loop design and formulation of bounds formation

The design specifications for the control loop are defined well in advance and then converted into suitable bounds, which are then used during the controller design. Apart from above, other specifications like disturbance rejection at the load caused due to sources and variation of the load Resistance ‘R’ are also to be considered. The design specifications are placed as inequalities on design loop gain, as inequalities on loop gain ‘G’, sensitivity function ‘S’, and the complementary sensitivity function ‘T’, at each frequency of the frequency array. The bounds placed on the loop gain and of the nominal plant of QBSTIC should ensure that all the plants corresponding to each operating point of the converter in the uncertainty set should satisfy these design specifications. The QFT places uncertainties and specification on them as inequalities in the form of closed-loop specifications given in Table-4.4, for both the loops:

Table 4. 5 Robust stability specifications

Specification	Inequality
Sensitivity	$\frac{1}{1+L(z)} \leq \delta_s$
Complementary sensitivity ‘T’	$T = \frac{L}{1+L} \leq \sigma_{GM}$
Tracking	$T_L(z) \leq \frac{L}{1+L} \leq T_U(z)$
Modulus Margin (MM)	$1/MM = 1/ 1+L _{\min} = S _{\max} \leq 2$

Where δ_s is the constraint on sensitivity, T_L , T_U is the upper and lower bounds specifications expressed either in constants/Transfer Functions/Arrays which will be dealt with in the subsequent sessions.

4.4.3.5 Formulation of Gain and Phase margin Bound

The constraint on gain margin (GM) and phase margin (PM) are placed as bounds on NC. From the specifications of Table-4.2 for a GM of 10dB and PM of 45°, the gain and phase margin bounds are obtained using the equations 4.22, 4.23, as $\sigma_{GM}=0.65$ which corresponds 8dB GM, and $\sigma_{PM} = 1.25$ for 45° PM ([61], [68], [69]).

$$GM=20 \log_{10} \left\{ \frac{\sigma+1}{\sigma} \right\} \text{ dB} \tag{4.27}$$

$$PM=2 \sin^{-1} \left\{ \frac{1}{2\sigma} \right\} \text{ deg} \tag{4.28}$$

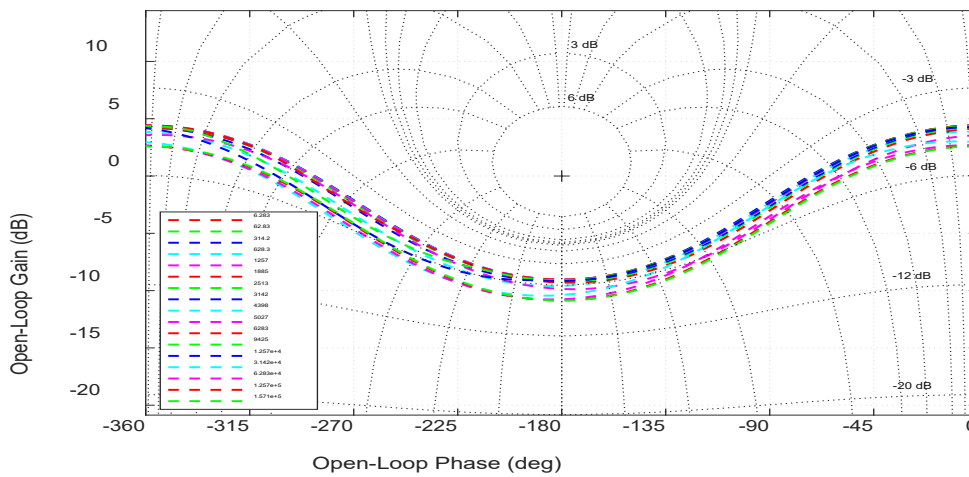


Fig. 4.27 Gain Margin Bounds

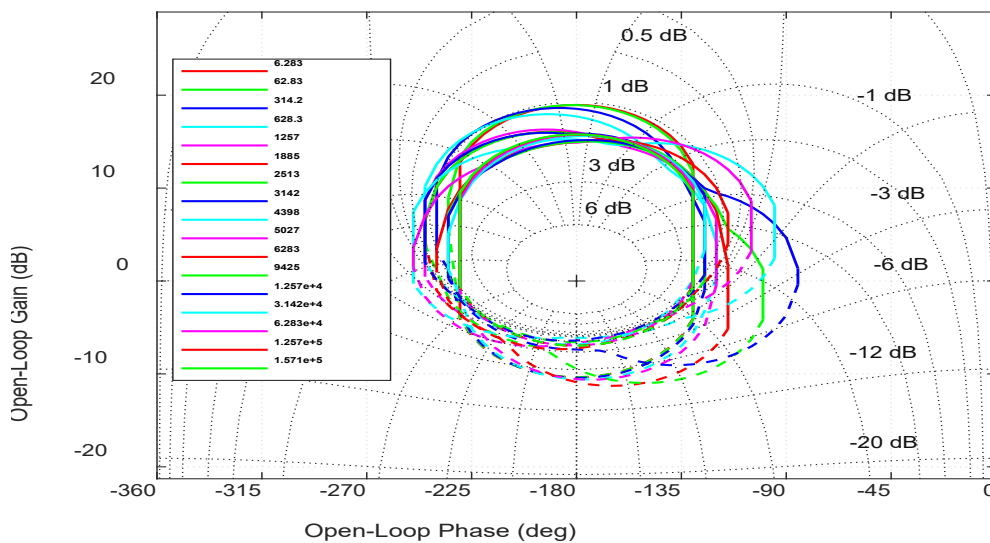


Fig. 4.28 Phase Margin Bounds

4.4.3.6 Formulation of Bandwidth Bound

The settling time of the closed-loop response is inversely proportional to the bandwidth of the loop gain. Hence, the controller bandwidth of QBSTIC is restricted due to the presence of RHP zeros in the off-diagonal control-to-output transfer functions. Therefore, a bandwidth bound of a minimum of 100Hz is placed during controller design to ensure that all the plants in the uncertainty range have a bandwidth higher than 100Hz. The bandwidth bounds are shown in Fig. 4.29.

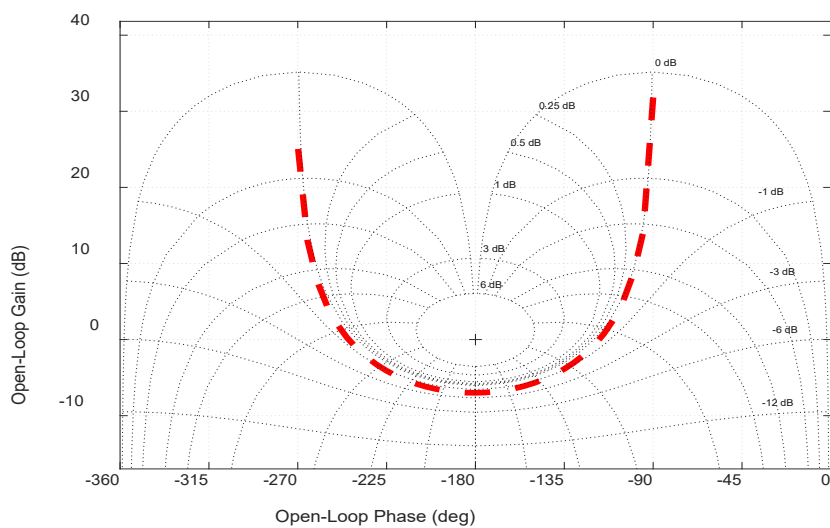


Fig. 4. 29 Bandwidth Bounds

4.4.3.7 Formulation of Reference Tracking Bound

Some of the applications demand that the start-up response of the controller must lie within a certain specified range. The start-up response of QBSTIC for all parametric variations can be maintained within the desired range by designing a pre-filter. Therefore, the requirement of the upper and lower startup response is placed as reference tracking bounds at the design time itself. The TF representing the startup response of QBSTIC is given by eq. 4.24. The step response corresponding to these transfer functions is shown in Fig. 4.30 while the reference tracking bounds are plotted in Fig. 4.31. These bounds are the requirements of the plant output to follow the given desired reference; due to the uncertainty in plants, the desired output is to be bounded

between the upper and lower time/frequency specifications mentioned in eq. 4.24, their step responses are shown in Fig. 4.30 where all the uncertainty set should lie [62].

$$T_U = \frac{0.024892 (z-0.9987) (z-0.779)}{(z-0.9982) (z-0.9881) (z-0.6756)} \quad (4.29)$$

$$T_L = \frac{7.4474e-08 (z+3.704) (z+0.2659)}{(z-0.9977) (z-0.9863) (z-0.9859)}$$

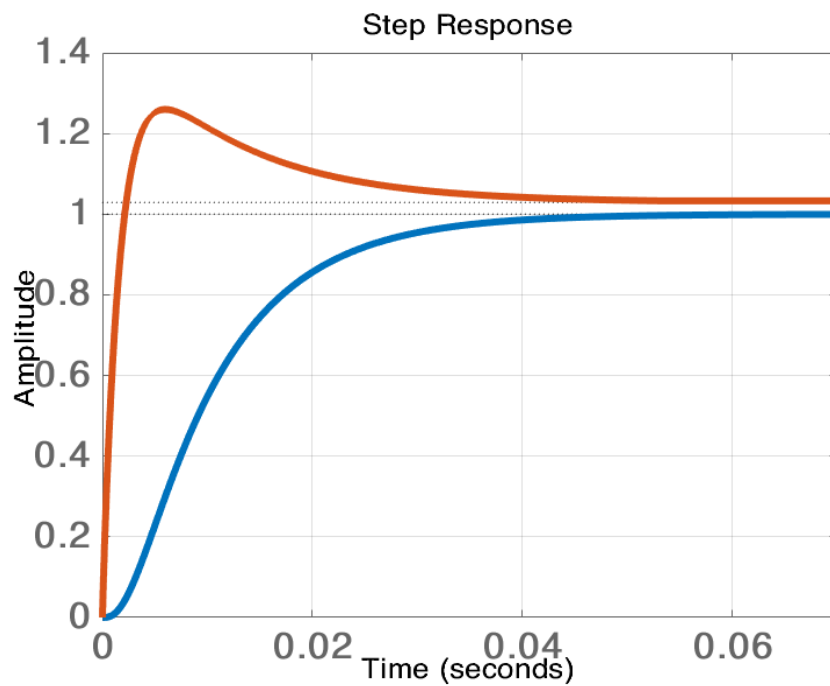


Fig. 4. 30 Step Response of the upper and lower tracking TFs T_U, T_L

For the T_U, T_L mentioned in eq. 4.24, the plant type-7 is selected to plot the reference tracking bounds, shown in Fig. 4.31.

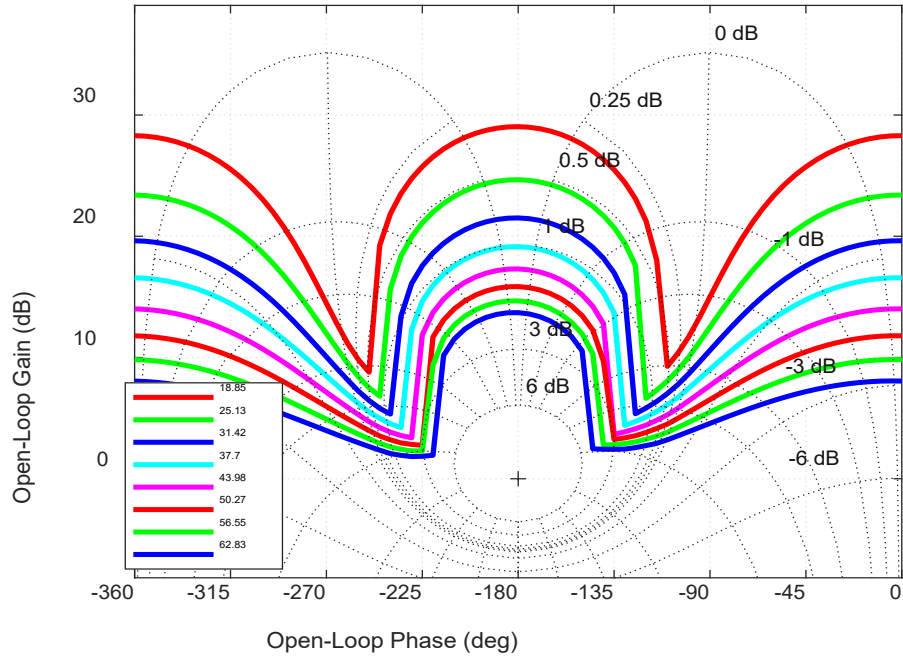


Fig. 4. 31 Tracking bounds of QBSTIC

4.4.3.8 Formulation of Sensitivity Bound

The output disturbance parameters for QBSTIC are to source voltage, load and the effect of the second controller loop. These disturbances affect the output in accordance with the closed-loop output impedance and closed-loop audio-susceptibility and (one more similar term for loop interaction). Therefore, these disturbances can be attenuated by placing bound on the magnitude of sensitivity function ‘S’ such that inequality is given by eq. s 4.30 is satisfied. The sensitivity bound is obtained using a first-order filter approximation equation given by eq. 4.30, which is reported in

$$|S| = \left| \frac{1}{1 + Q_{11}G_{c11}} \right| \leq \delta_s = \frac{1.7932(z-1)}{(z-0.9969)} \quad (4.30)$$

Let the Q_{11} and G_{c11} are written in polar form:

$$Q_{11} = qe^{j\theta}; G_{c11} = g_c e^{j\phi}$$

$$|S| = \left| \frac{1}{1 + Q_{11}G_{c11}} \right| \leq |\delta_s|$$

$$\left| \frac{1}{1 + Qe^{j\theta}G_c e^{j\phi}} \right| \leq |\delta_s| \quad (4.31)$$

$$1 + Qe^{j\theta}G_c e^{j\phi} \geq |\delta_s^{-1}|$$

Squaring on both sides, and rearranging the final expression is obtained as

$$Q^2 G_c^2 + 2Q^2 G_c^2 \cos(\theta + \phi) + 1 - \delta_s^{-1} \geq 0 \quad (4.32)$$

The sensitivity bounds are shown in Fig. 4.32

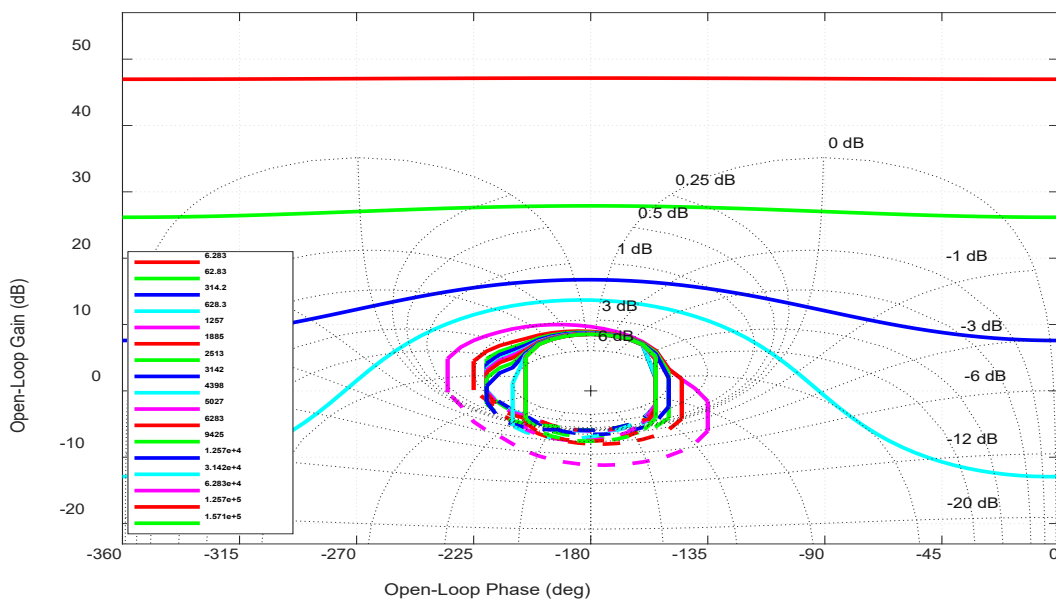


Fig. 4. 32 Sensitivity bound plot of loop-1

4.4.3.9 Formulation of Modulus Margin Bound (MMB)

The modulus margin is the minimal distance between the critical point $[-1, j0]$ and the Nyquist plot of the open-loop transfer function. The closed-loop system is considered to be robustly stable if the condition of eq. 4.33 is met, the response of controllers will be fast if $MM < 2$;

$$MM = |1 + L|_{\min} > 0.5 \text{ or } 1/MM = 1/|1 + L|_{\min} = |S|_{\max} < 2 \quad (4.33)$$

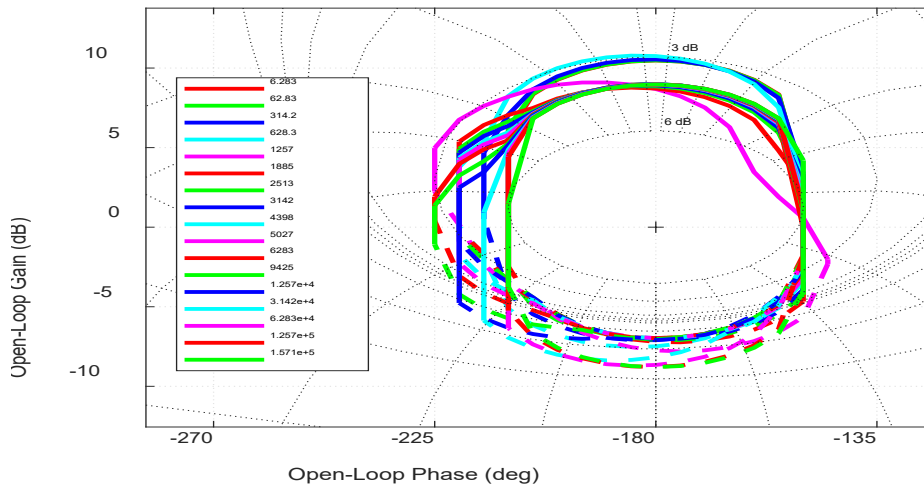


Fig. 4. 33 Modulus margin bound

4.4.3.10 Formulation of Composite Bound

The composite bounds are framed from the individual bounds corresponding to each constraint. These bounds are plotted at each frequency element of FA by choosing the outer envelope of each bound. If the composite bound is satisfied, it indicates that all the constraints corresponding are also satisfied. The composite bound is shown in Fig. 4.34.

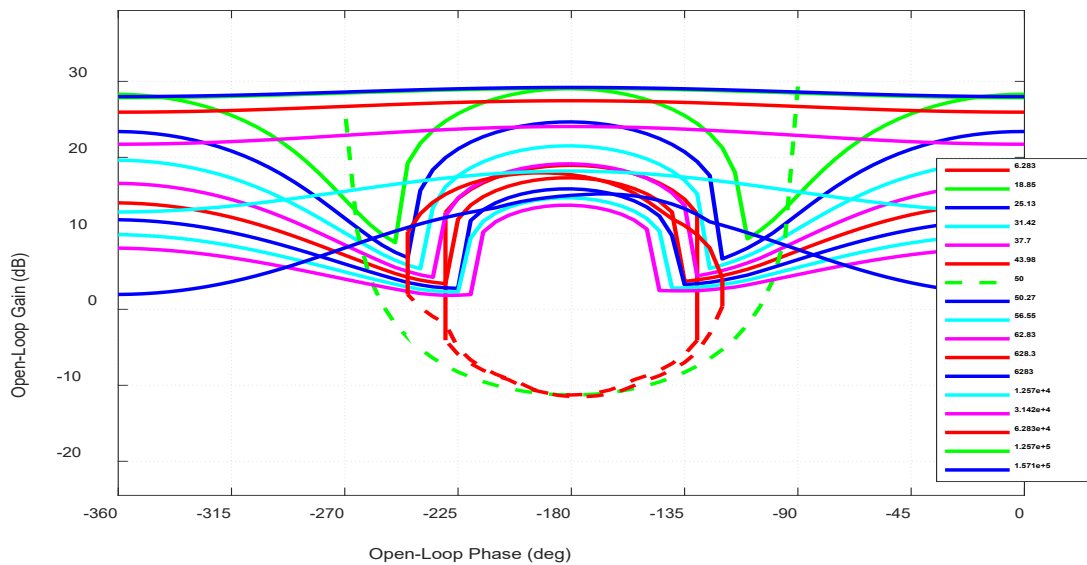
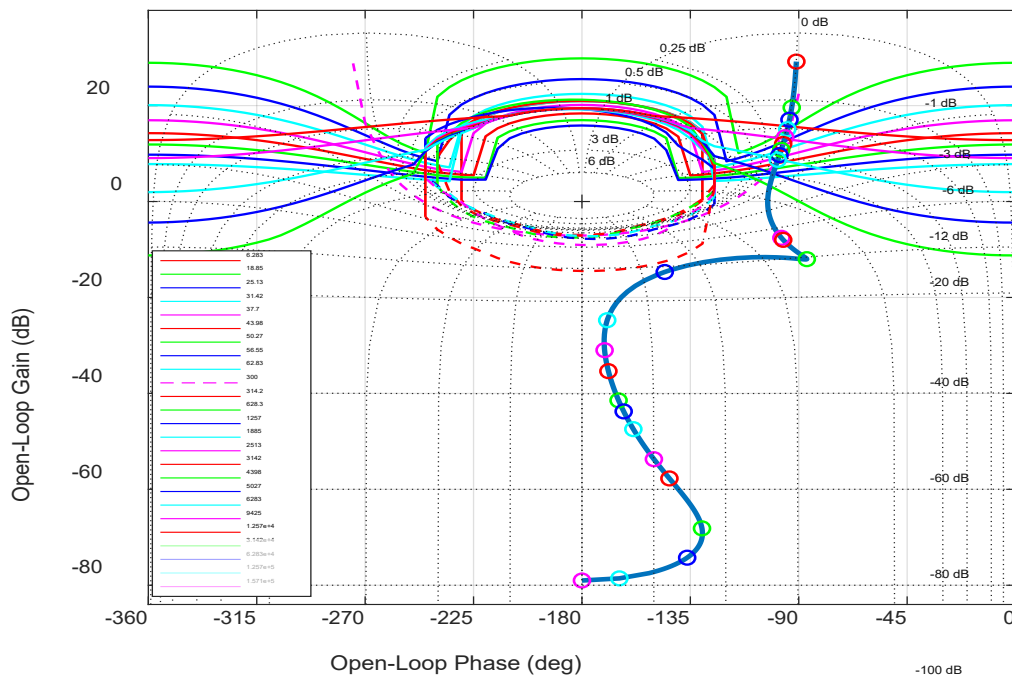


Fig. 4. 34 Composite bounds of loop-1

4.4.3.11 Controller design by Loop-Shaping (LS)

QFT toolbox offers the GUI based platform for manually designing of the controller such that an open-loop TF of Loop $L(z)$ satisfies all the specifications and constraints mentioned previously and ensures the stability and robustness. The poles and zeros of the controller adjusted in such a way that the shape of the loop is moved in all the four directions of the NC plane to a get into such a shape that satisfies all the bounds. The loop-gain plot along with the composite bounds at each frequency in FA, is shown in Fig. 4.26, the loop gain lies above the upper bounds and below the lower bounds so that it ensures the loop gain satisfies at all the bounds. The robust controller obtained after loop shaping is given in eq. 4.34. The frequency responses of loop-gain, S, T are shown in Fig. 4.36.

$$G_{c11} = \frac{0.003787 (z-0.9937)(z-0.9814)}{(z-1) (z-0.997)} \quad (4.34)$$



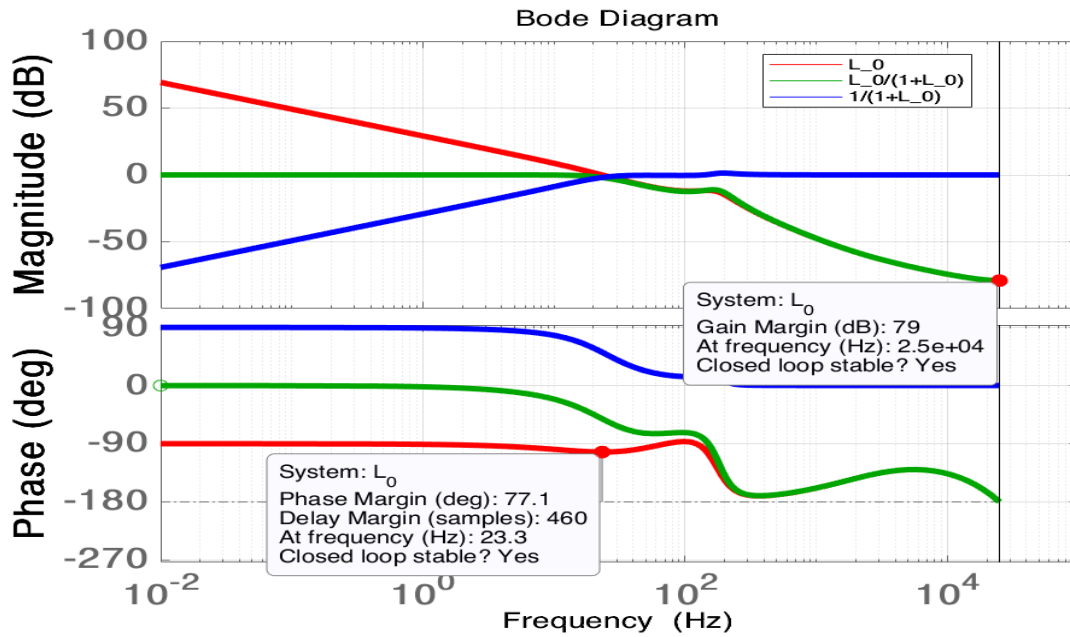


Fig. 4. 36 Bode plot of Loop gain ($G_{c11} * Q_{11}$) (red), complementary sensitivity (T), Sensitivity (S) of voltage control loop.

4.4.3.12 Prefilter (F) design

Once the controller is designed, pre-filter is also designed using the GUI which allows the placement of poles and zeros of pre-filter at desired locations so that the uncertainty set plants and the step and frequency responses of QBSTIC are brought within the desired upper and lower limits, shown in Fig. 4.37 and the corresponding F is shown in eq. 4.35, And the frequency response of the uncertainty plants set is shown in Fig. 4.37 (blue and green lines), it was found to be within the mentioned limits.

$$F_{11} = \frac{0.6714 (z-0.9829)}{(z-0.9885)} \quad (4.35)$$

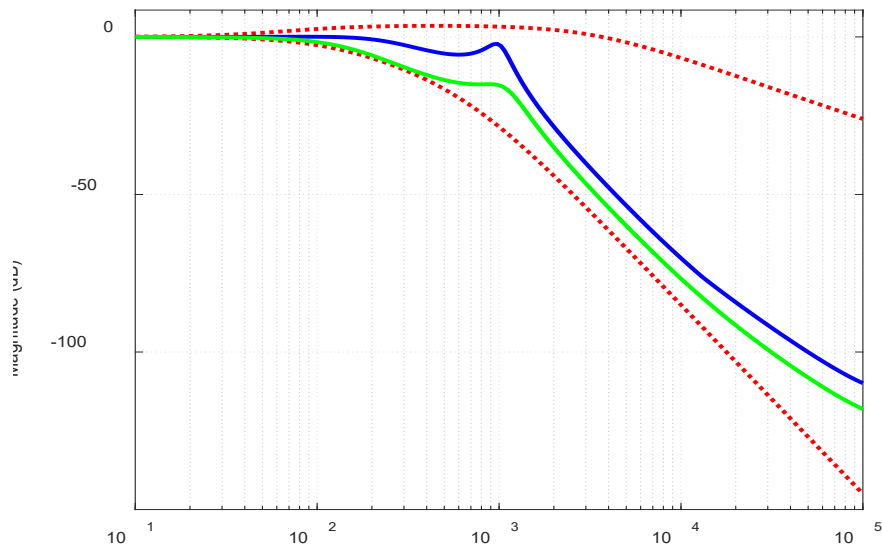


Fig. 4. 37 Pre-filter (F1) design of Loop-1

4.4.3.13 Performance Validation of Loop-1

In order to check whether the loop gain is satisfying all the constraints/bounds the composite bound is compared with the constraint.

(i) Verification of GM and PM bound: After completion of the design of the controller and pre-filter, the robust stability of the controller is to be verified in the time-domain as well as frequency domains. The constraint on the magnitude on $|T|$ is to check by plotting the robust stability plot shown in Fig. 4.38, it may be observed that the closed-loop (CL) frequency Response (FR) is well below the safety margin ' $\gamma=1.3$ ' (blue dotted line) [66]. This indicates that the loop-gain at all operating points has $GM > 6$ dB and $PM > 40^\circ$, which validates the robust stability check. For addressing the Robust Stability in terms of bounds on the nominal loop, two aspects are considered [66]:

- (1) stability of the nominal system (corresponding to nominal plant)
- (2) the Nyquist envelope does not intersect the critical point (which is the $(-180^\circ, 0$ dB) in Nichols chart or the $(-1, 0)$ point in the complex plane).

In a Nichols chart it is equivalent to placing a magnitude constraint on the complementary sensitivity function which is

$$|T_1| = \frac{L_{g1}}{1+L_{g1}} \leq \infty$$

Therefore, the above condition is typically replaced by the margin condition

$$|T_1| = \frac{L_{g1}}{1+L_{g1}} \leq \gamma > 1 \quad \forall p \in P, w > 0$$

Where γ which is termed as a safety factor calculated using the following equations:

$$GM = 20 \log_{10} \left\{ \frac{\gamma + 1}{\gamma} \right\} \text{ dB}$$

$$PM = 2 \sin^{-1} \left\{ \frac{1}{2\gamma} \right\} \text{ deg}$$

So, in this context the GM of 8dB and Phase margin of 45° were selected to obtain the γ to be 2, which was kept as safety margin. To ensure stability the log magnitude plot is plotted using the QFT toolbox [66] shown below:

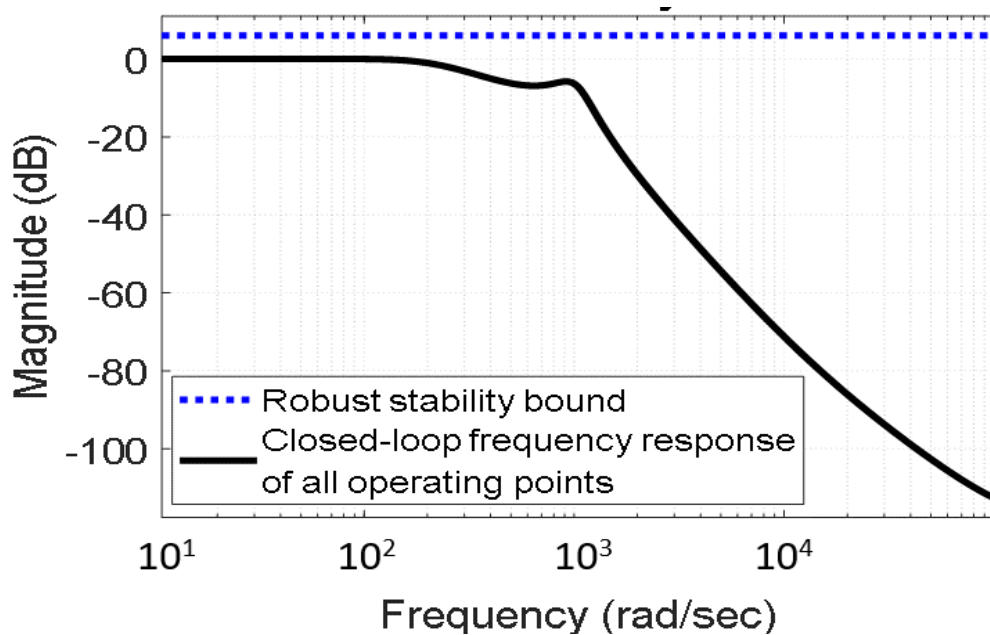


Fig. 4. 38 Robust stability check for Loop-1

(ii) Verification of Modulus margin bound: Modulus margin bound discussed the previous section is the bound on the closed-loop system stability and the condition is mentioned in eq. 4.33, so for $MM < 2$, a check on stability is performed and plotted in Fig. 4.39, it is observed that the peak of the envelope of the sensitivity function at all operating points is less than the modulus margin, which satisfies check-2.

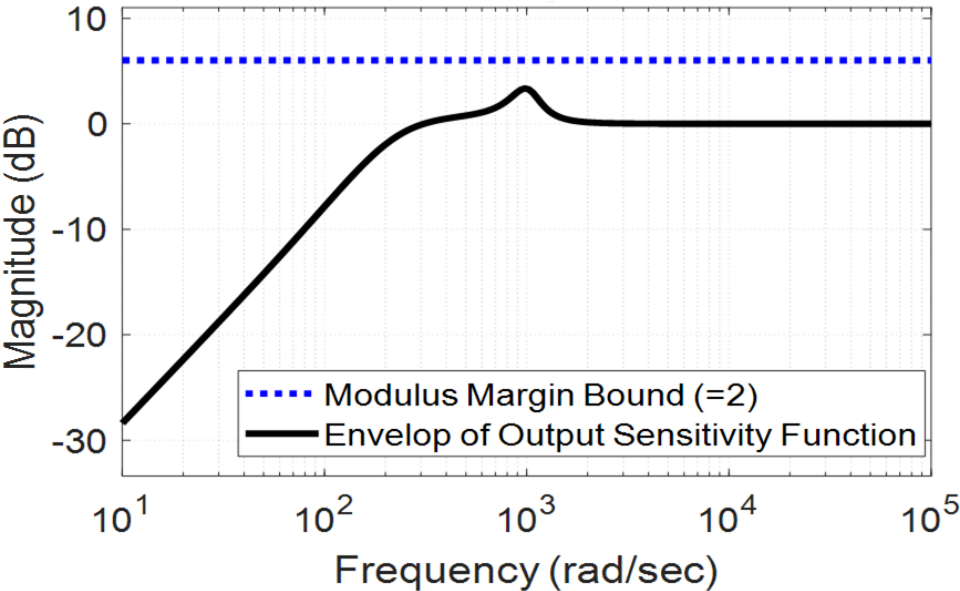


Fig. 4. 39 Closed-loop system stability check of Loop-1

(iii) Verification of Sensitivity bound: The envelope of the output sensitivity function for all operating points in the uncertainty set and the disturbance rejection is plotted in Fig. 4. 40 is found to be less than δ_s , which is the closed-loop sensitivity mask, shown in the blue dotted line. This indicates that the disturbances arising due to rejection of all plants in uncertainty set.

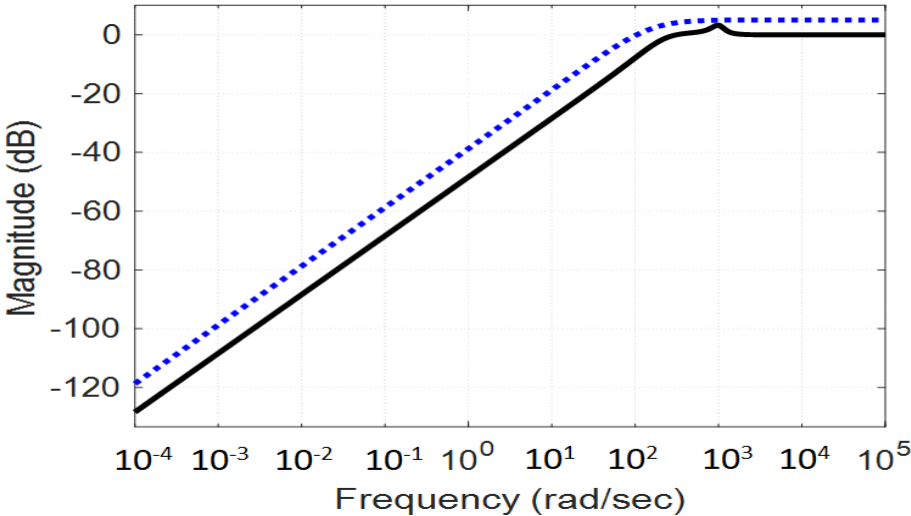


Fig. 4. 40 Sensitivity bound check.

(iv) Verification of the startup response bound: The start-up response is checked by plotting unit step of closed-loop tracking response of QBSTIC at all the operating points of the uncertainty shown in Fig. 4.41, it is observed that the start-up responses of the most operating points (yellow lines) are within the acceptable lower (red line) and upper bounds (blue line), the QFT-GUI dedicated tool of ‘pfshape’ of pre-filter is used to observe and plot these responses.

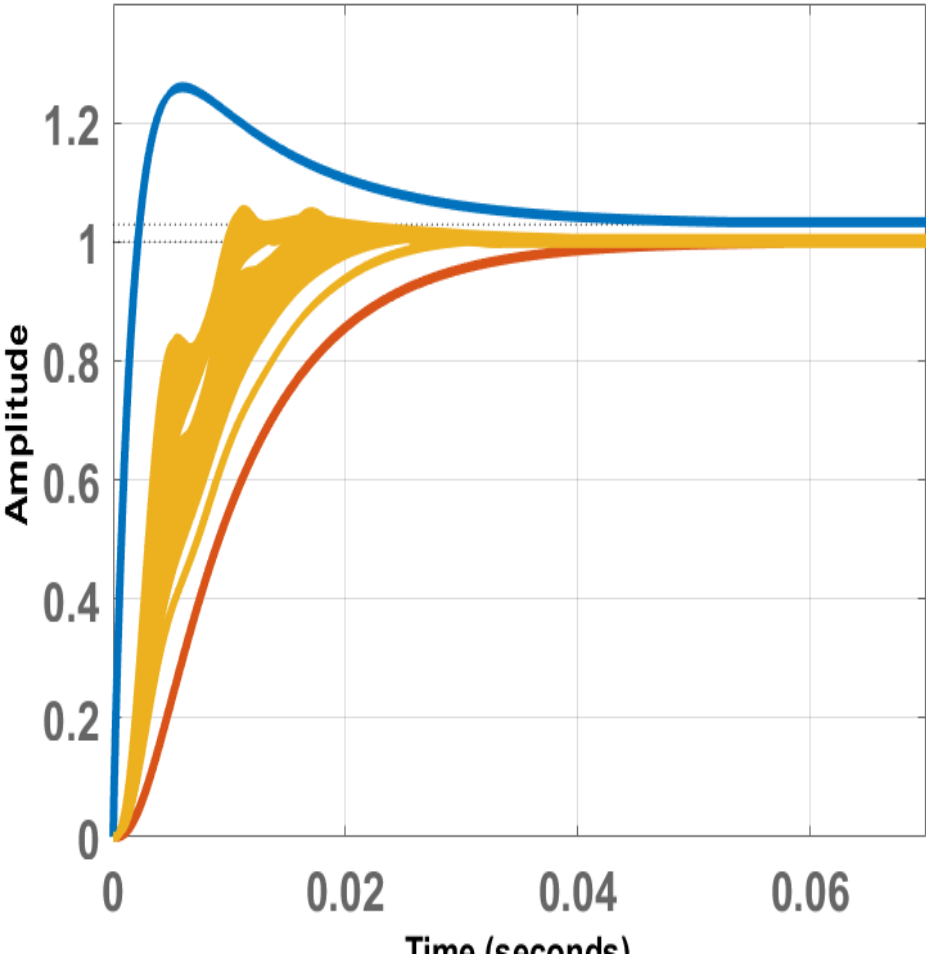


Fig. 4. 41 Step response of the uncertainty set

This concludes the performance validations of loop-1. In the same guidelines, the design procedure is applied for loop-2, the following bounds were obtained, shown in Figs. 4.42, 4.43. The corresponding bounds of the current loop are mentioned below:

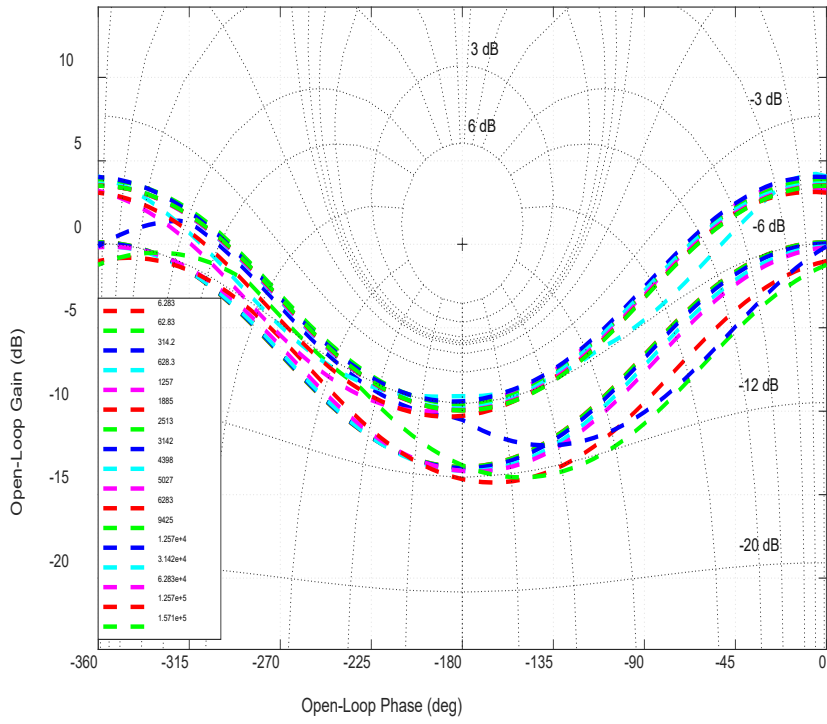


Fig. 4. 42 Phase margin Bound of Current controller of QBSTIC

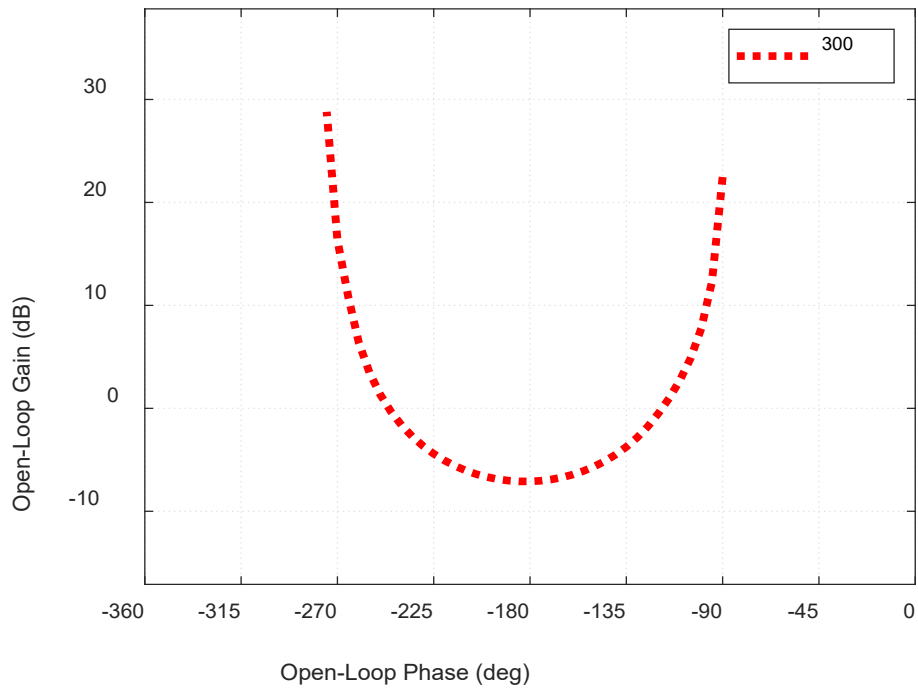


Fig. 4. 43 Bandwidth Bound of Current controller of QBSTIC

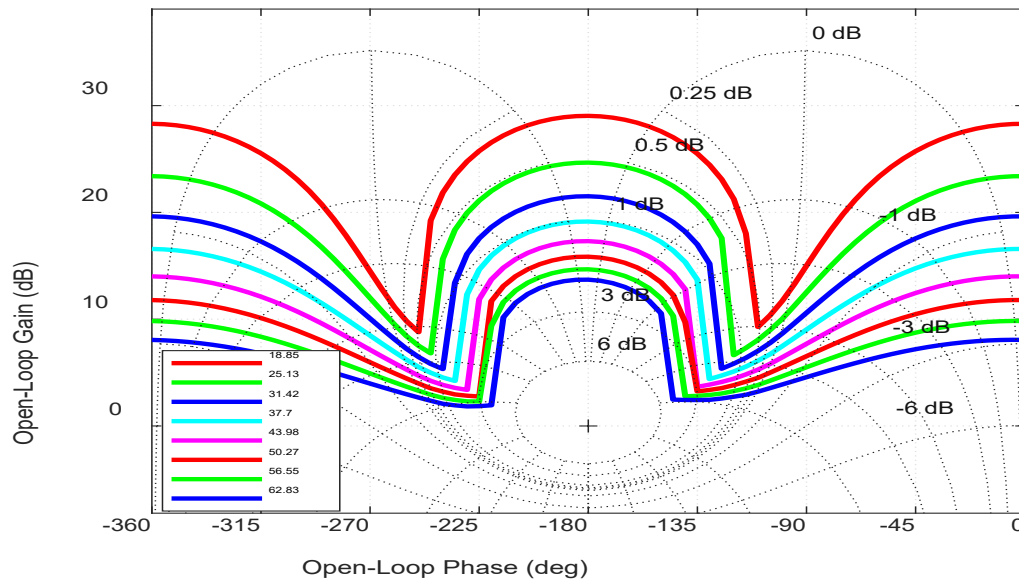


Fig. 4. 44 Tracking bound of Current controller of QBSTIC.

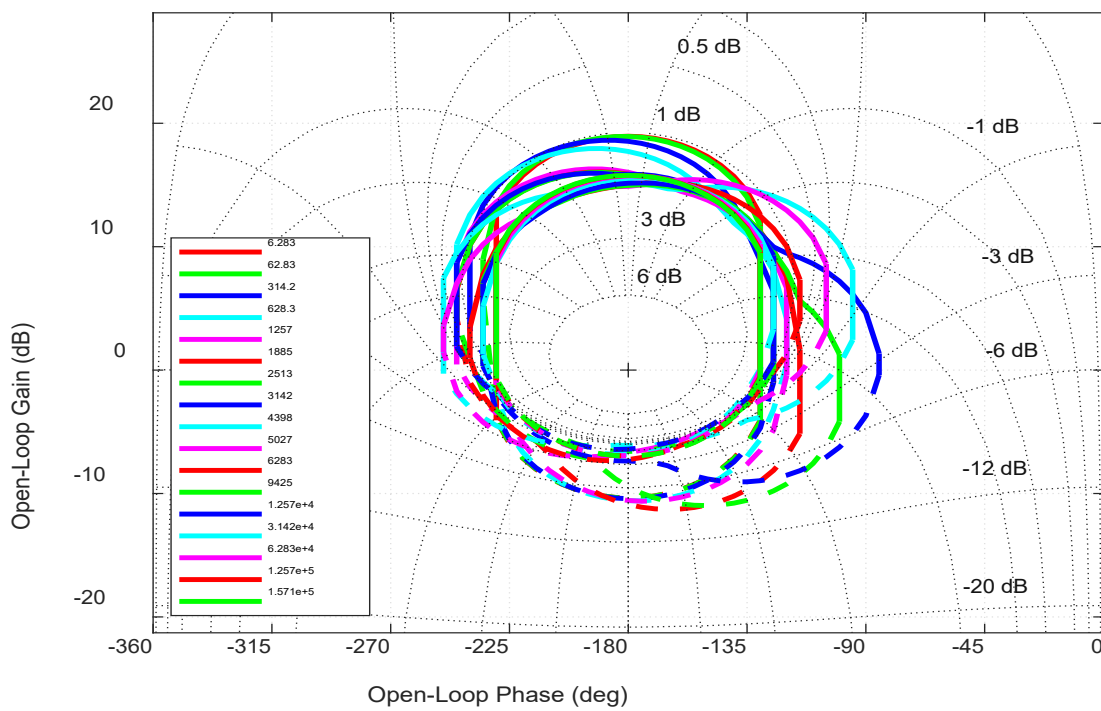


Fig. 4. 45 Phase Margin Bound of Current controller of QBSTIC.

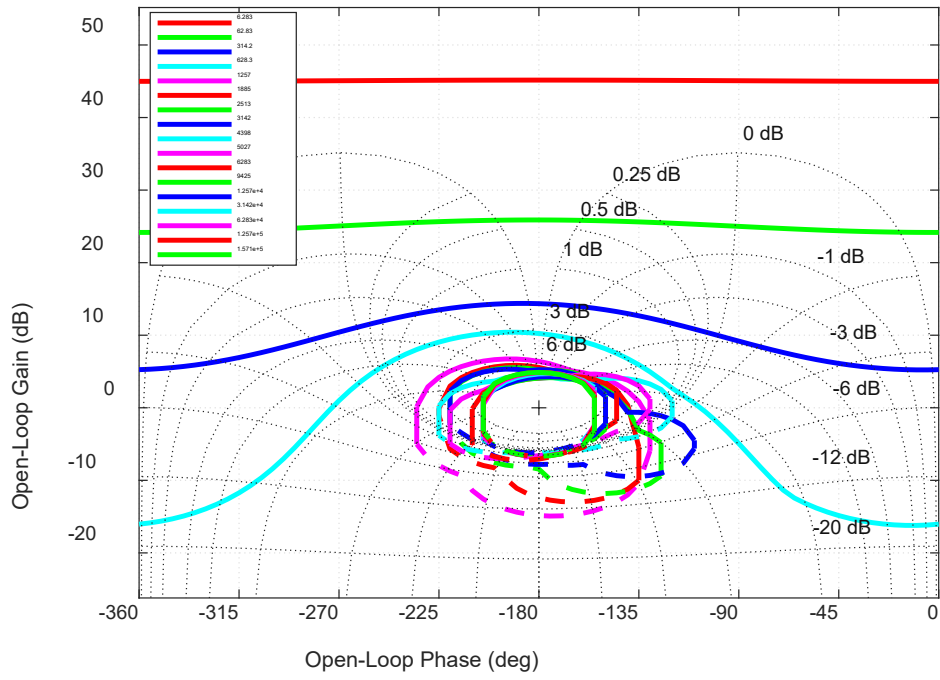


Fig. 4. 46 Sensitivity Bound

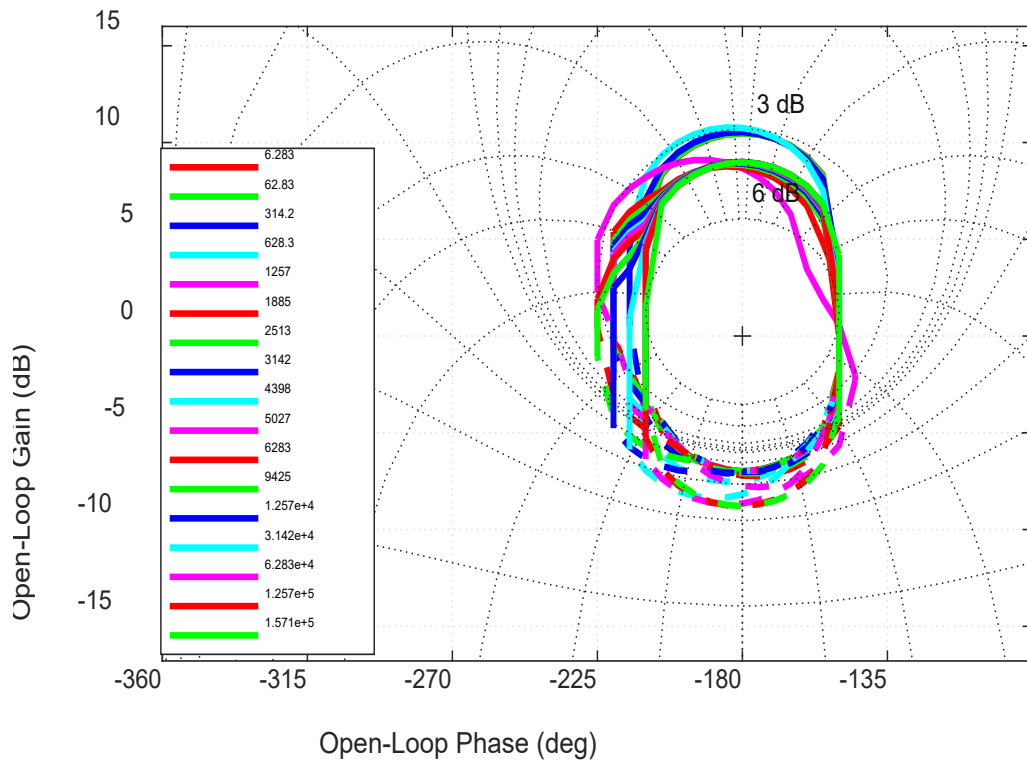
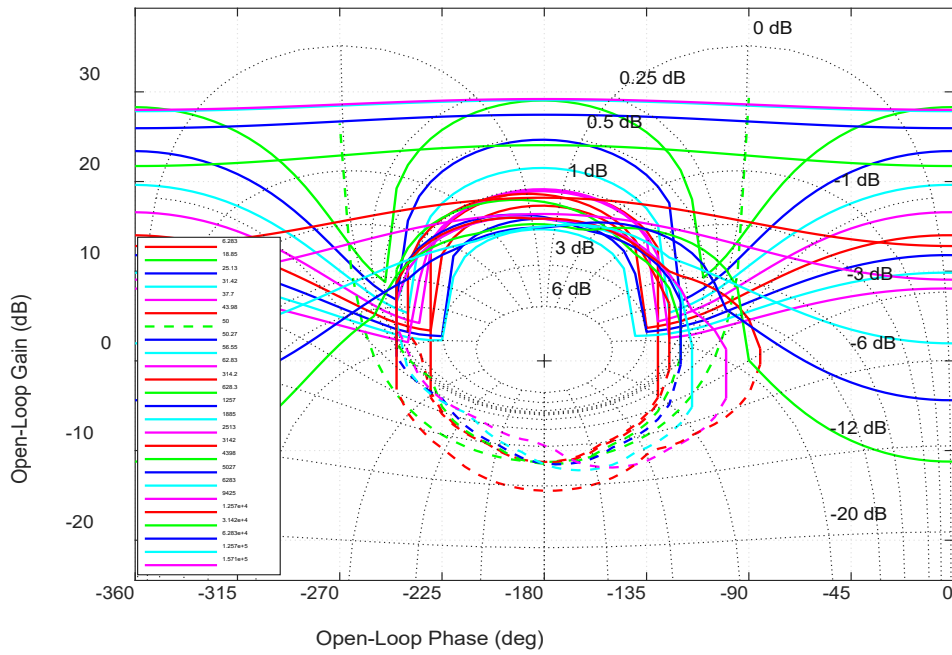


Fig. 4. 47 Modulus Margin Bound



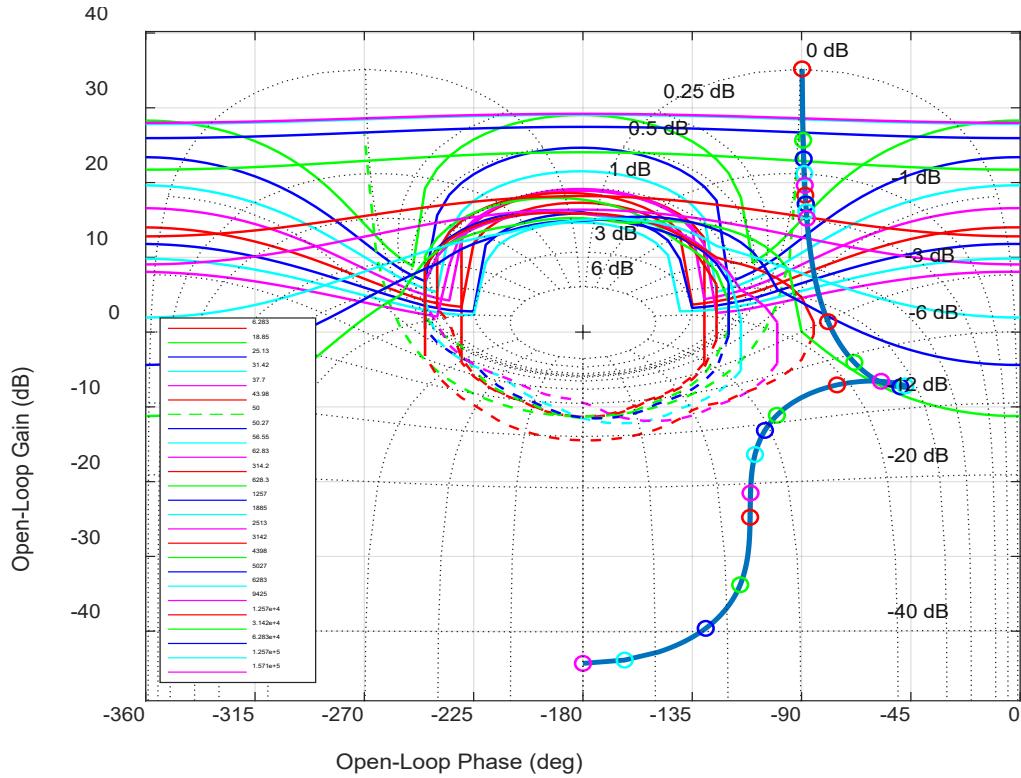


Fig. 4. 50 Loop-shape of controller G_{c22} of Current-loop

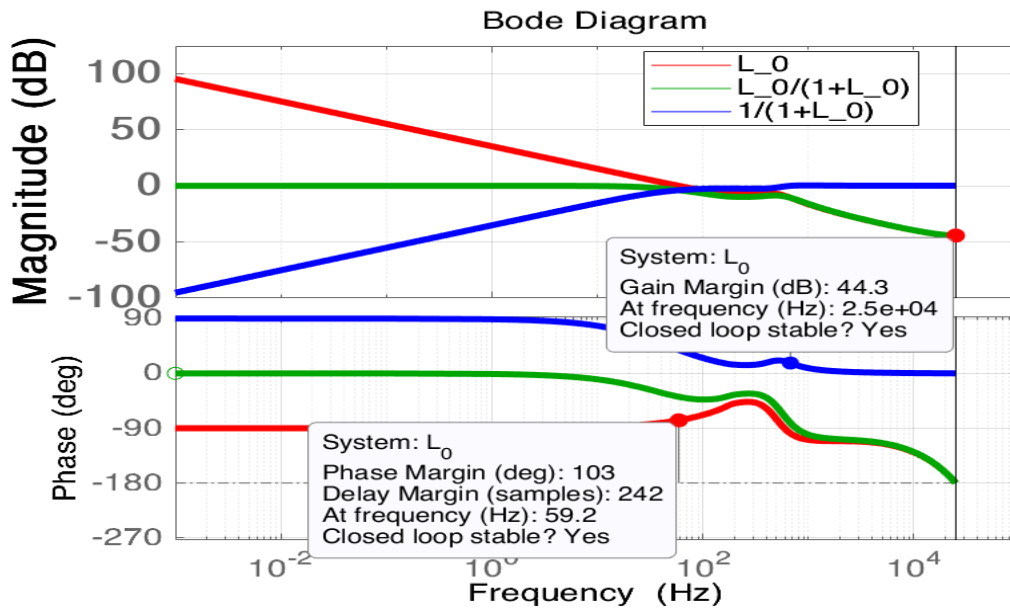


Fig. 4. 51 Bode plot of Loop gain ($G_{c22} * Q_{22}$) (red), complementary sensitivity (T), Sensitivity (S) of voltage control loop.

The current controller for current loop is given by eq. 4.32.

$$G_{c22} = \frac{0.009674 (z-0.9937) (z-0.9777)}{(z-1) (z-0.983)} \tag{4.36}$$

The pre-filter F_{22} is given by 4.32.

$$F_{22} = \frac{0.036779 (z-0.9972)}{(z-0.9964)(z-0.9709)} \tag{4.37}$$

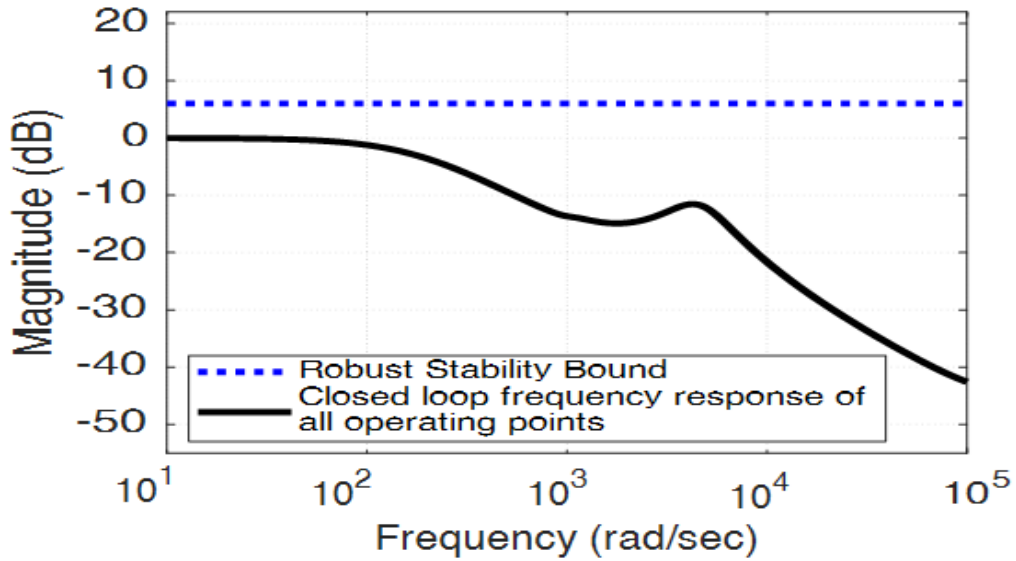


Fig. 4. 52 Robust stability check for Loop-2

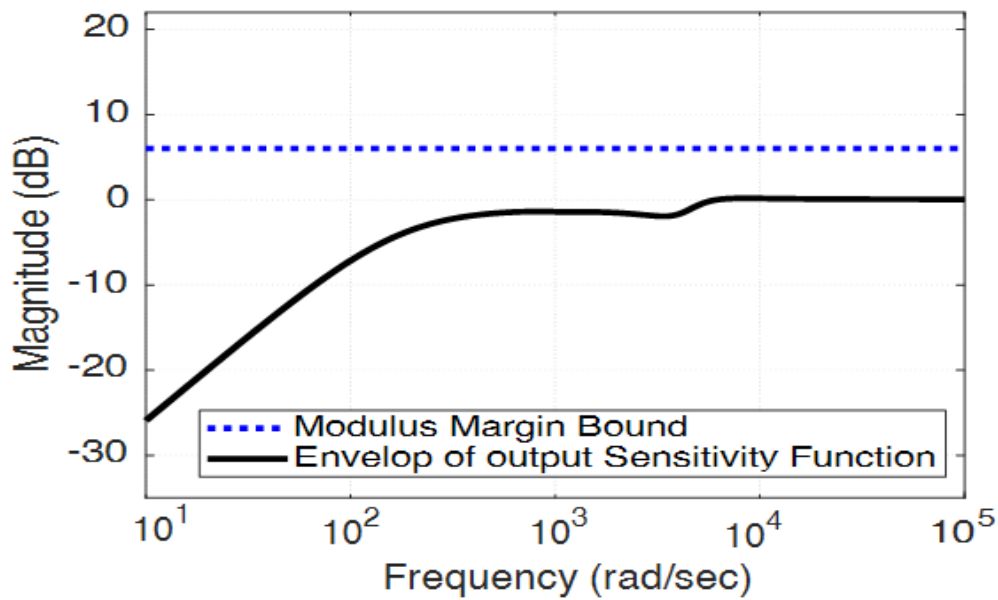


Fig. 4. 53 Closed-loop system stability check of Loop-2

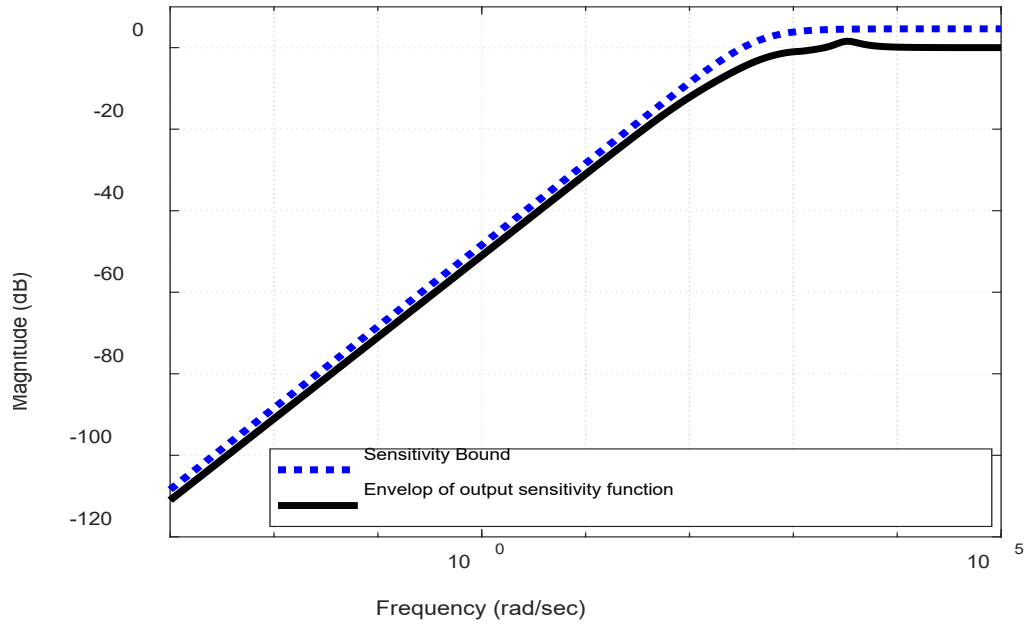


Fig. 4. 54 Closed-loop system stability check of Loop-2

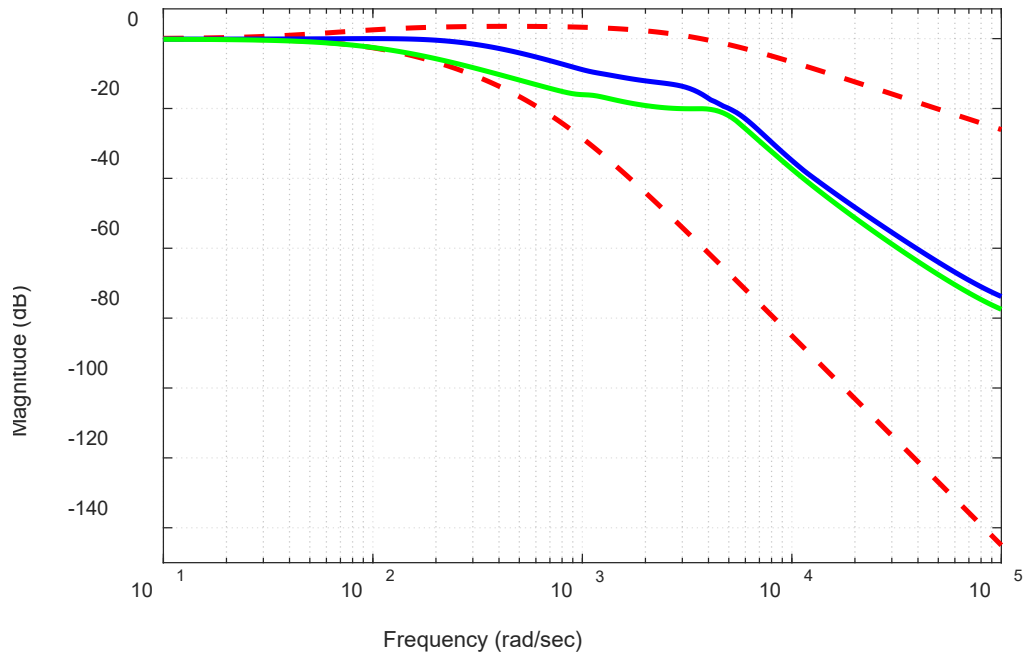


Fig. 4. 55 Tracking verification of (F2) design of Loop-2

The envelopes of the robust stability, output sensitivity functions for all operating points in the uncertainty set are found to be less than the respective bounds, shown in the Figs. 4.52-4.55. Having designed the diagonal controllers ‘ G_{c11} , G_{c22} ’, and their pre-filters ‘ F_{11} , F_{22} ’ the off-diagonal controller design is handled in the subsequent section.

4.4.3.14 Off-diagonal controller design

The main aim of designing the off-diagonal controllers is to reduce the coupling, once the diagonal controllers are designed and they satisfy constraints like disturbance rejection and stability etc., the off-diagonal compensators just become a trade-off. Since the off-diagonal controllers do not belong to either voltage or current loops, the loop-shaping controller design and pre-filter are not required. For off-diagonal controllers instead, they are designed in sequence from already obtained diagonal controllers G_{c11} , G_{c22} to minimize the coupling given by eq.s (4.34,4.36), as per the procedure given in [61], [58]. The off-diagonal controllers are to be designed with the plant which has the magnitude and phase which is in the middle range of uncertainty set.

$$C_{12} = p_{12}^* - \left[\frac{p_{22}^*(p_{12}^* + G_{c12})}{(p_{22}^* + G_{c22})} \right] \quad (4.38)$$

$$C_{21} = p_{21}^* - \left[\frac{p_{11}^*(p_{21}^* + G_{c21})}{(p_{11}^* + G_{c11})} \right] \quad (4.39)$$

The element G_{c12} , G_{c21} are designed over the frequencies of interest so that its magnitude, phase passes through the middle of expression mentioned in eqs. (4.38, 4.39) are selected,

$$G_{c12} = \left[G_{c22} \frac{p_{12}^*}{p_{22}^*} \right] \quad (4.40)$$

$$G_{c21} = \left[G_{c11} \frac{p_{21}^*}{p_{11}^*} \right] \quad (4.41)$$

From the above two equations, the off-diagonal controllers are obtained as:

$$G_{C12} = \frac{0.00013 z (z - 0.9998)}{(z - 1) (z - 0.8644)} ; \quad (4.42)$$

$$G_{C21} = \frac{0.000017z}{(z - 1)} \quad (4.43)$$

The full controller matrix is given by eq. 4.44.

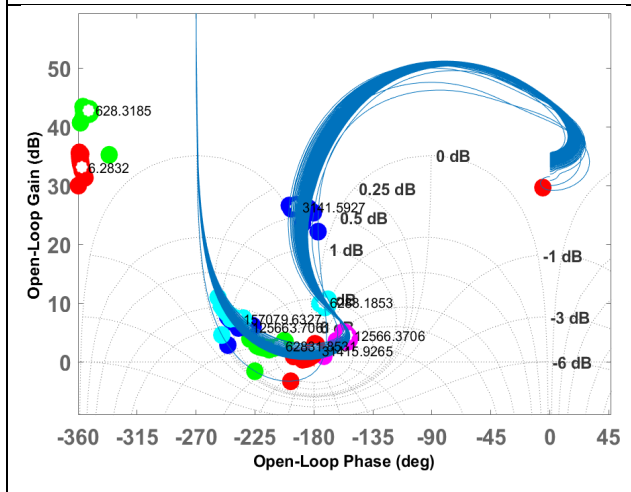
$$[G_C] = \begin{bmatrix} \frac{0.003787 (z-0.9937)(z-0.9814)}{(z-1) (z-0.997)} & \frac{0.0013 z (z - 0.9998)}{(z - 1) (z - 0.8644)} \\ \frac{0.00017z}{(z - 1)} & \frac{0.009674 (z-0.9937) (z-0.9777)}{(z-1) (z-0.983)} \end{bmatrix} \quad (4.44)$$

The loop-gain matrix (L_P) is obtained by eq. 4.45:

$$[L_P] = \begin{bmatrix} L_{P11} & L_{P12} \\ L_{P21} & L_{P22} \end{bmatrix} = \begin{bmatrix} G_{C11}Q_{11} & G_{C12}Q_{12} \\ G_{C21}Q_{21} & G_{C22}Q_{22} \end{bmatrix} \quad (4.45)$$

The Figures 4.56, 4.57, 4.58, 4.59, and 4.59, which show the uncertainty template plots for the frequencies of interest of frequency array discussed in subsection 4.4.3.1, each of these figures have two plots: the ones on the left are the uncertainty template variation for transfer functions Q_{11} , Q_{12} , Q_{21} , Q_{22} , while the ones on the right are the plots of loop gains $G_{c11}Q_{11}$, $G_{c12}Q_{12}$, $G_{c21}Q_{21}$, $G_{c22}Q_{22}$. The uncertainty templates of effective transfer functions of matrix $[Q]$ were found varied unevenly around the critical point (180° , 0 dB) "+" symbol on the Nichols chart, exhibiting improper phase and gain margins. After the controllers are designed the uncertainty plots of loop gains are plotted which showed the proper phase and gain margins for each of the plant's remaining transfer functions.

The Nichols charts of uncertainty template plots without controllers



The Nichols charts of uncertainty template plots along with the controllers incepted

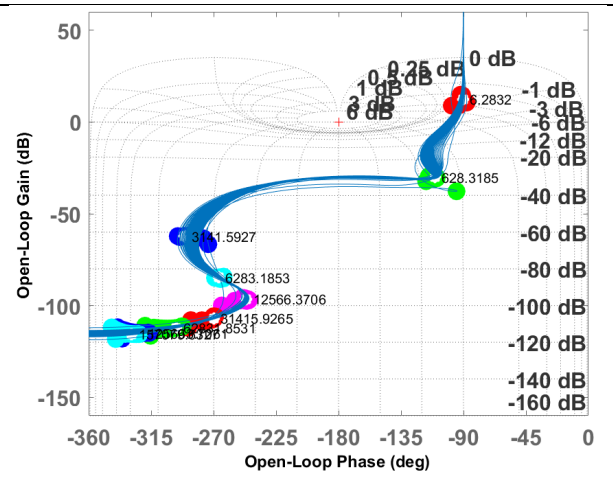


Fig. 4. 56 Nichols charts of uncertainty template plot of Q_{11} and loop gain $Q_{11} G_{c11}$

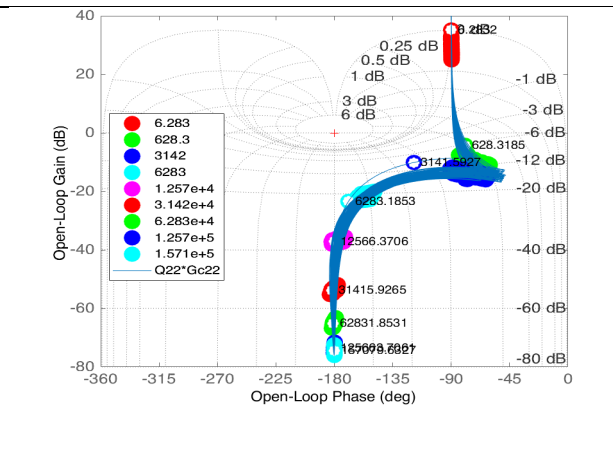
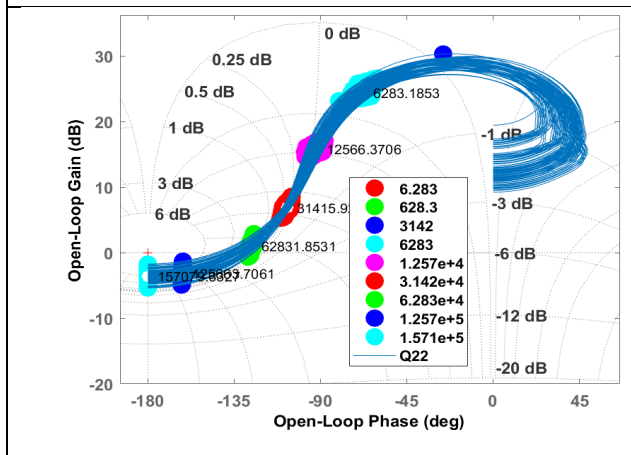


Fig. 4. 57 The uncertainty template plot of Q_{12} and loop gain $G_{c12} Q_{12}$

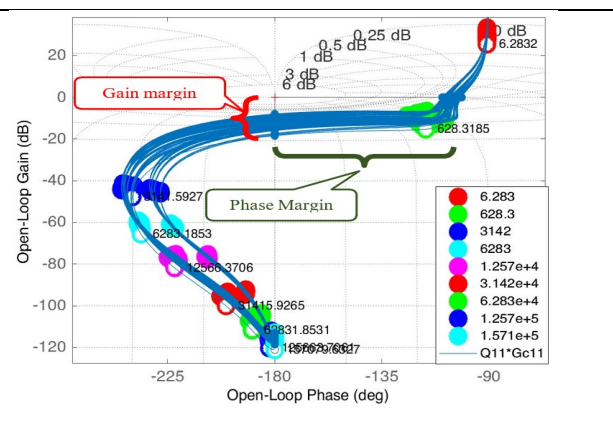
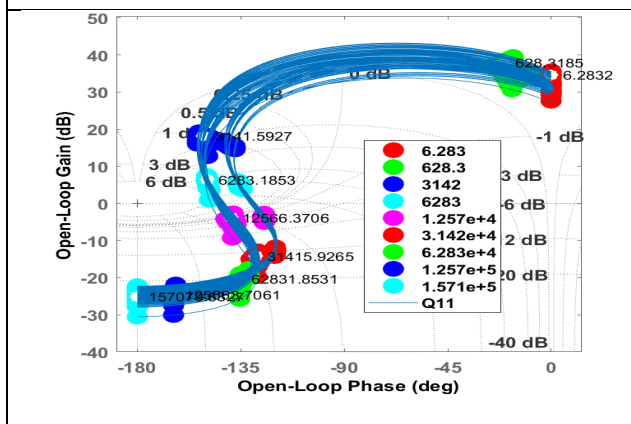
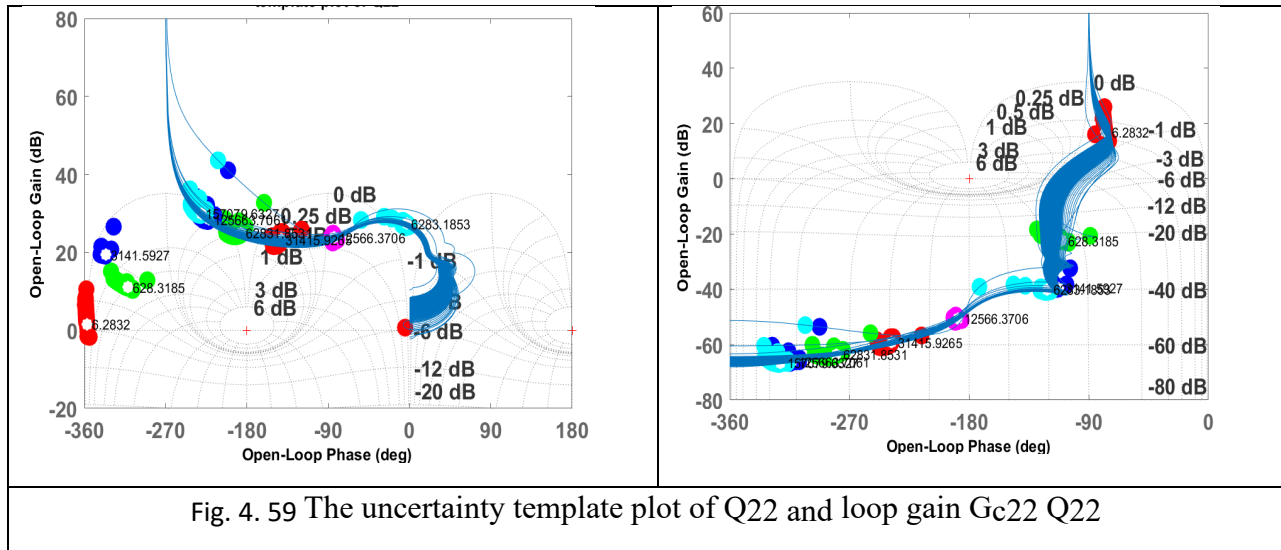


Fig. 4. 58 The uncertainty template plot of Q_{21} and loop gain $G_{c21} Q_{21}$



The Figs. 4.56 to 4.59 are the Nyquist plots of the plant-controller loop gains, after the inception of controller the Nyquist plot is plotted to check the stability of all the four loops, as per the procedure given in the book “Robust control Engineering: Practical QFT Solutions”, by Mario- Garcia-Sanz, explains the procedure to check the stability condition.

4.4.4 Stability check on controllers of QBSTIC

The sequential non-diagonal MIMO QFT controller design when finished, should meet the stability conditions:

- (i) Each loop $Q_{ii}G_{cii}$, $i=1,2$ has to satisfy the Nyquist encirclement condition
- (ii) There should not be any pole-zero cancellations.
- (iii) No Smith McMillan pole-zero cancellation between Q , G_c .

The plots are shown in Fig. 4. 60 (a)-(d) are the Nyquist plots of loop-gains mentioned in eq. 4.43, upon observing the plots all curves are away from the critical point $(-1,j0)$, which ensures the stability of all the loops. It was observed that due to calculation of equivalent plant Q_{ii} needs the inverse of plant matrix usually introduces some exact pole-zero cancellations, which could

erroneously be introduced due to computer rounding errors [58], maybe ignored, such cases are observed for unrealizable combinations of every uncertainty set, and were ignored.

The Nyquist plots are plotted for the nominal plant and the designed controllers to check the closed-loop stability condition which was shown in Fig. 4.60, all the Nyquist plots are away and not encircling the critical point and hence the closed-loop system is stable at the nominal operating point.

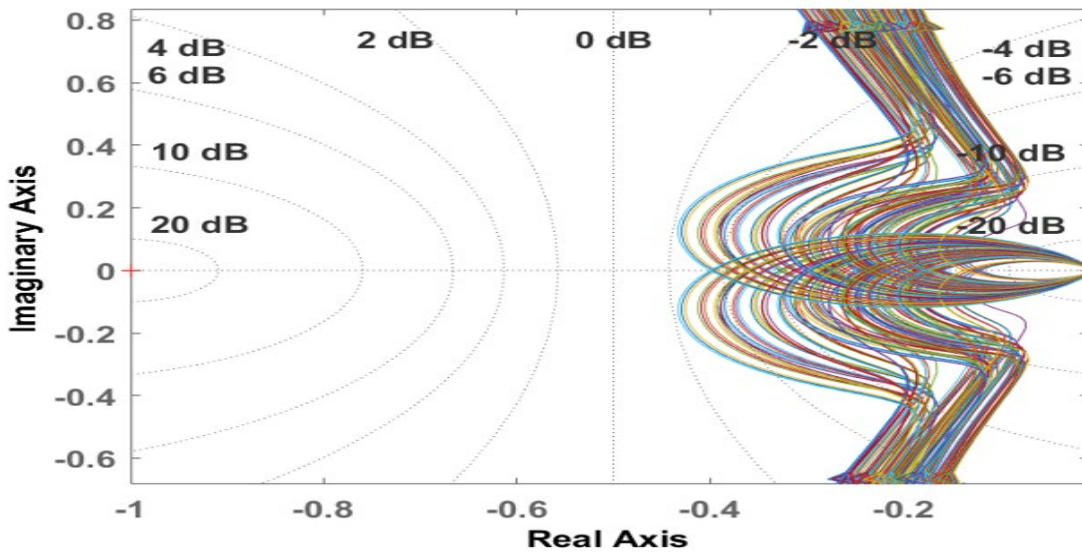


Fig. 4. 60 The loop gain of $(Q_{11} G_{c11})$,

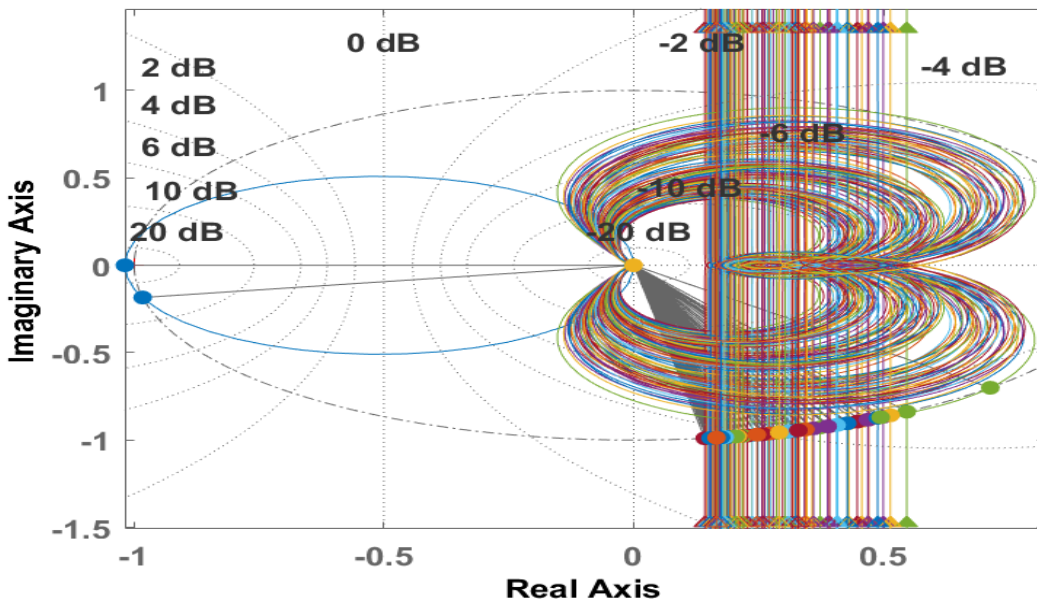


Fig. 4. 61 The loop gain of $(Q_{12} G_{c12})$

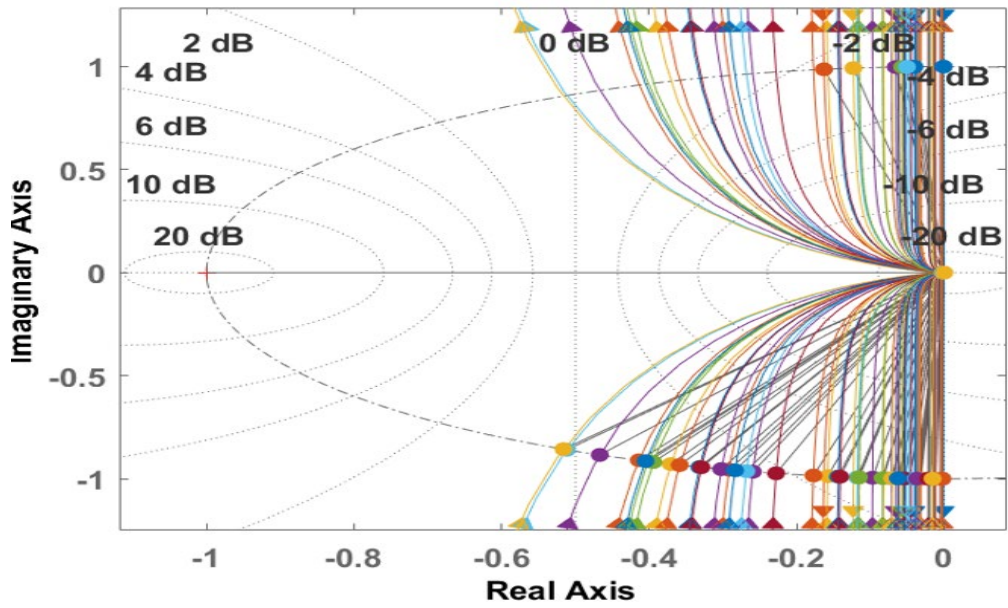


Fig. 4. 62 The loop gain of $(Q_{21} G_{c21})$,

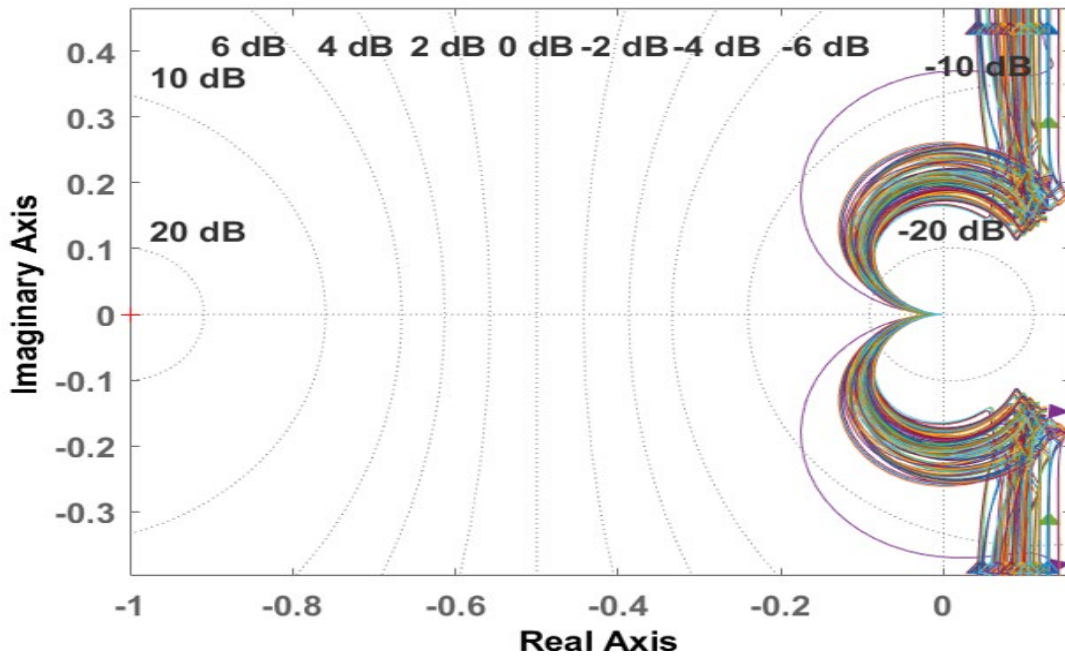


Fig. 4. 63 The loop gain of $(Q_{22} G_{c22})$

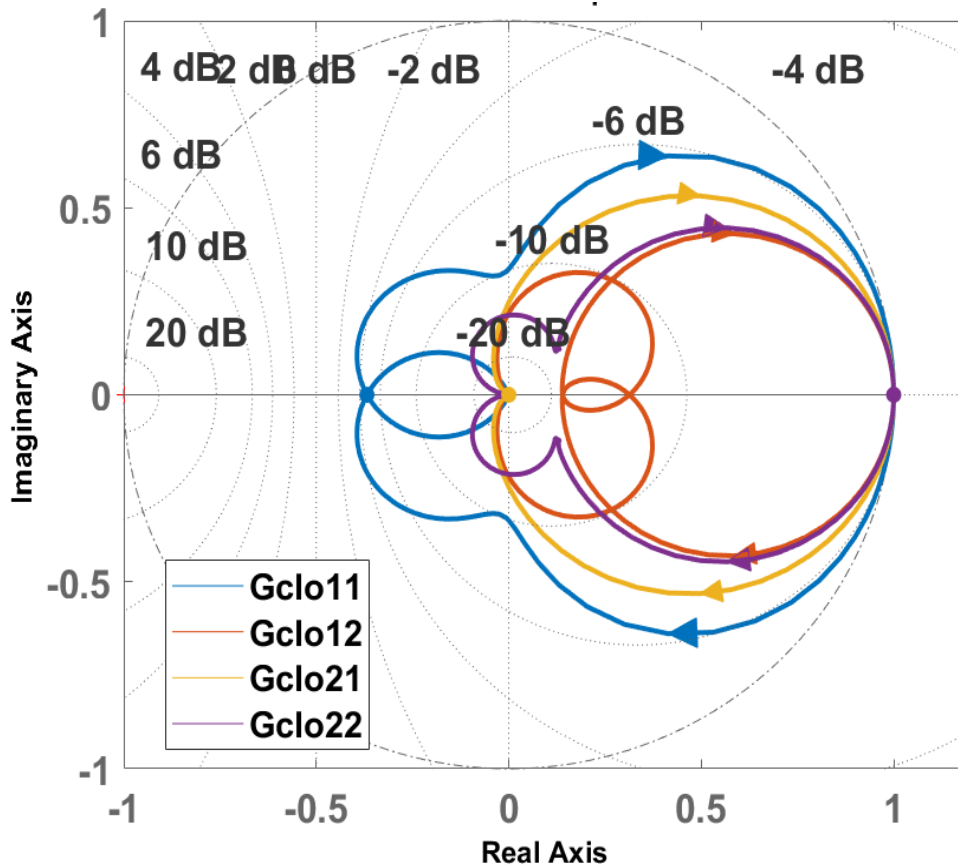


Fig. 4. 64 Nyquist plot of the nominal plant loop

4.4.5 Performance Validation and simulation

In order to verify the design of QFT controllers of eq. 4.36, the open-loop frequency response of all the disturbances at the output of the voltage and current loops due to parametric variation of Table 4.2 [52], and their worst-case bounds are shown in Fig. 4.61, and the frequency response plots of the open-loop and the closed-loop responses of the nominal plant are shown in Fig. 4.54. The worst-case bound for both the voltage and current loops were obtained and are given by expressions $Aud_{v_{gd}}$ for voltage loop and $Aud_{i_{gd}}$ for the current loop, shown in eq. 4.46,47:

$$Aud_{V_{gd}} = \frac{0.1067z^2 - 0.1394z + 0.03326}{z^3 - 2.004z^2 + 1.012z - 0.006957} \quad (4.46)$$

$$Aud_{I_{gd}} = \frac{0.4773z^2 - 0.2143z - 0.2451}{z^2 - 1.843z + 0.8491} \quad (4.47)$$

These are the two bounds which are placed as a constraint for the disturbances at the output of both the loops and envelop of all of the disturbances at the output voltage and current loop should lie below these two bounds shown in eq. 4.39, to ensure the robust performance of the controller, which is plotted below in Figs. 4.65, 4.66.

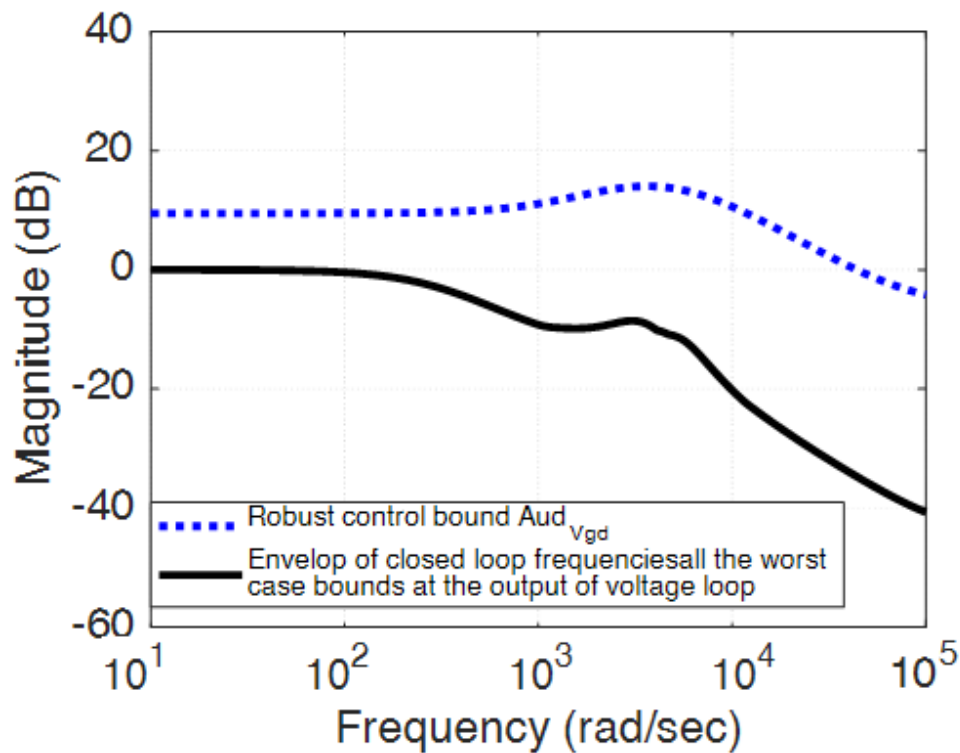


Fig. 4. 65 Robust stability bound check for disturbance attenuation at Voltage-loop

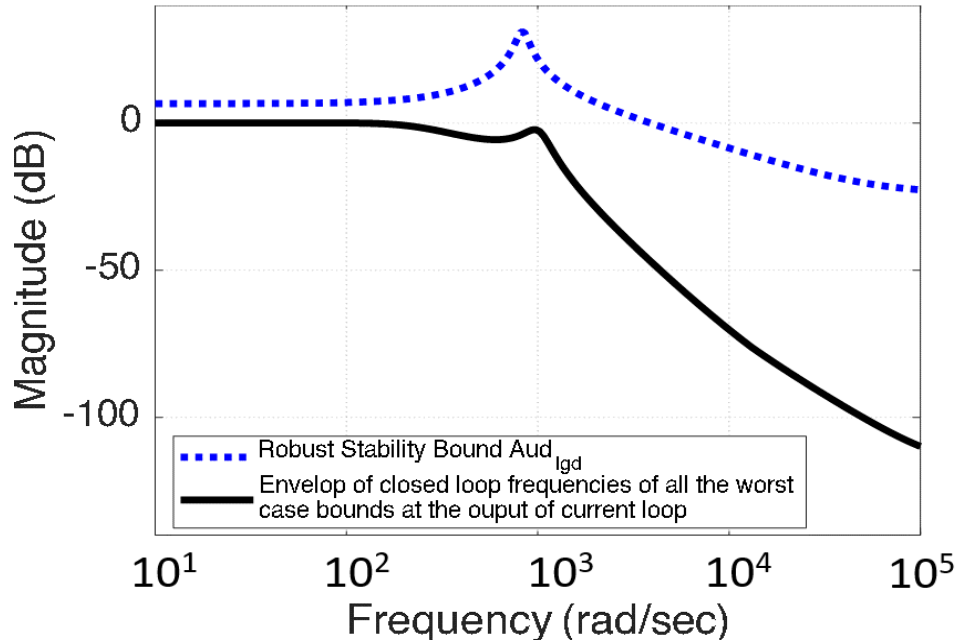


Fig. 4. 66 Robust stability bound check for disturbance attenuation at Current-loop

The above validations confirm the effectiveness of the controllers in minimizing the disturbances and ensuring the stable operation, in the next section the controllers obtained are used to carry the time-domain simulations.

4.4.6 Performance Validation and simulation :

Time-domain simulation:

The effectiveness of the SMQFT controller is demonstrated for a 36/12V, 96W prototype QBSTIC for testing the voltage, current regulation and checking the robustness against the source/load variations. After designing the SMQFT controllers for QBSTIC, a series of simulations are carried out to validate the effectiveness of the controller in attaining the output voltage regulation and source current regulation. For the uncertainty set mentioned in Table 4.19, of section 4.4.3 and the following results are obtained. The steady-state waveforms of load voltage and source current and load current are shown in Fig. 4.67.

When the load Resistance is fixed, and the source voltages are varied from 36V to 40V, 36V to 32V, at 0.3 secs, and source voltage V_{g2} varied from 12-14V and 12 to 10V at 0.5 secs, shown in the Figs. 4.68 to 4.71, in all the cases, appropriate duty ratios are generated to maintain the load voltage regulation and source current regulation.

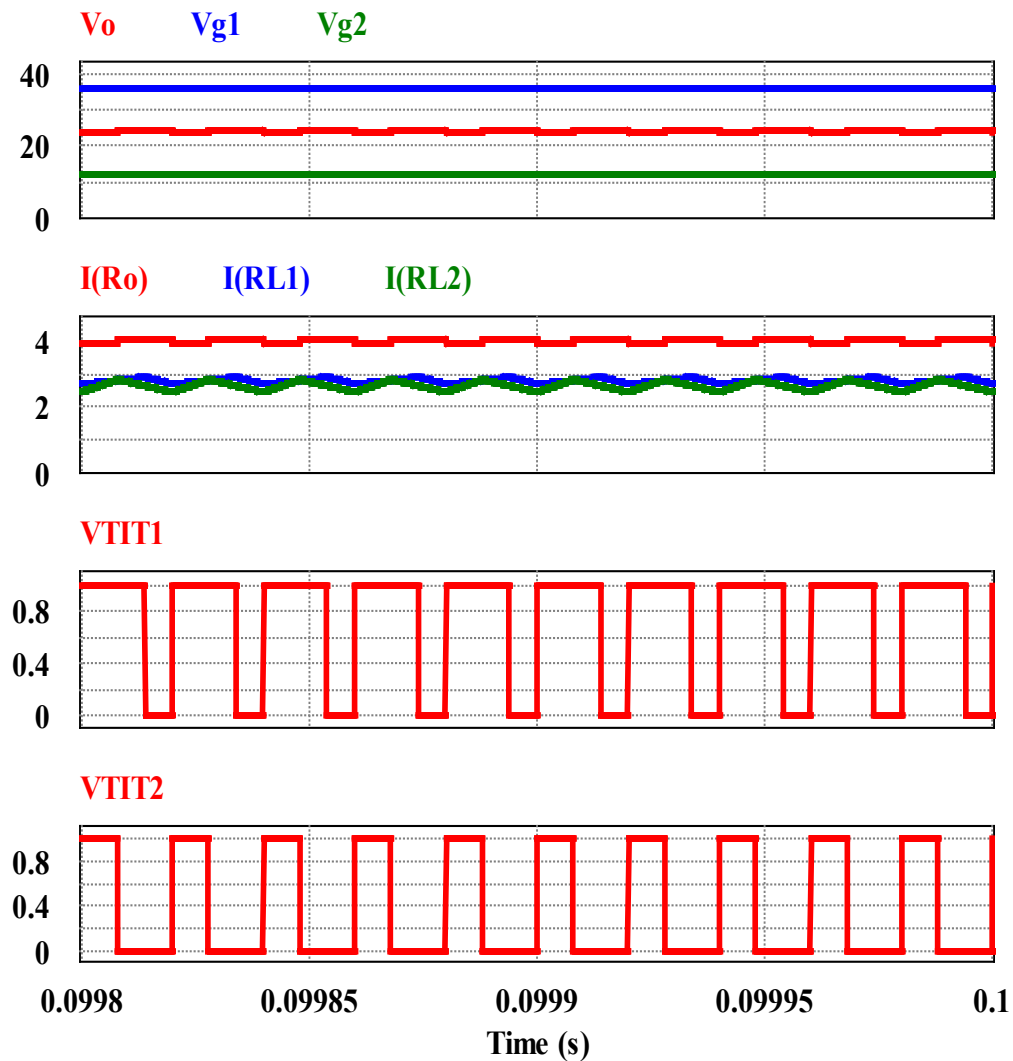


Fig. 4. 67 Steady-state waveforms for QBSTIC.

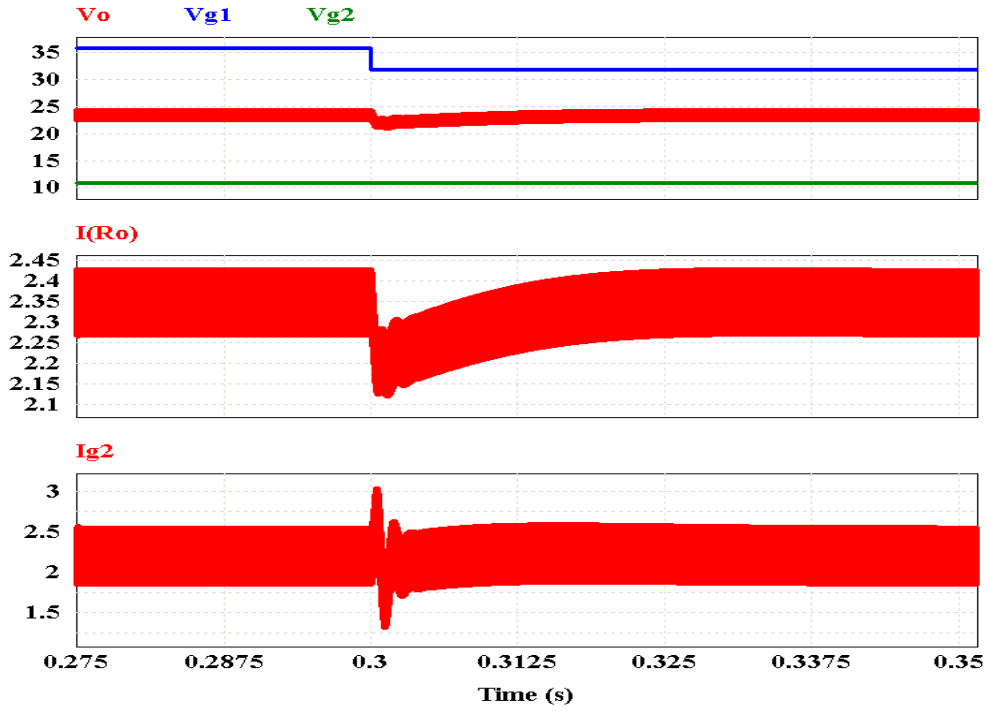


Fig. 4. 68 The variation of V_o , I_o , I_{g2} currents due to variation of V_{g2} : 36V to 32V

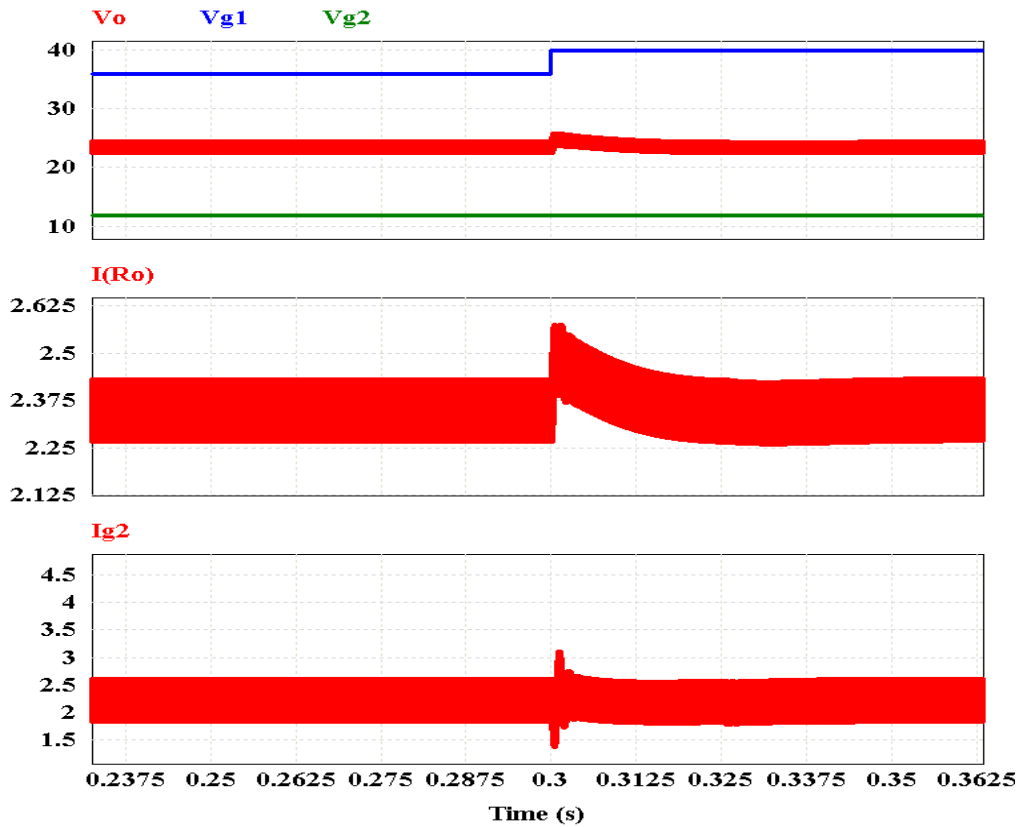


Fig. 4. 69 The variation of V_o , I_o , I_{g2} currents due to variation of V_{g1} : 36V to 40V

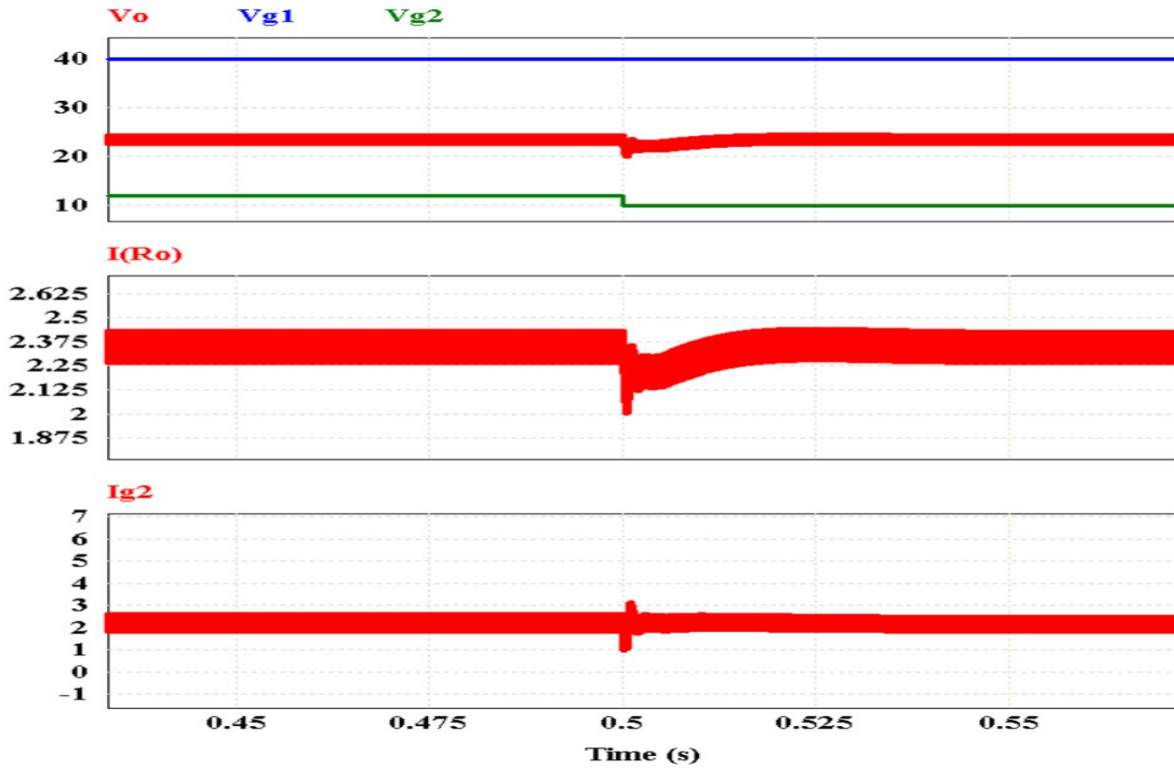


Fig. 4. 70 The variation of V_o , I_o , I_{g2} currents due to variation of V_{g2} : 12V to 10V

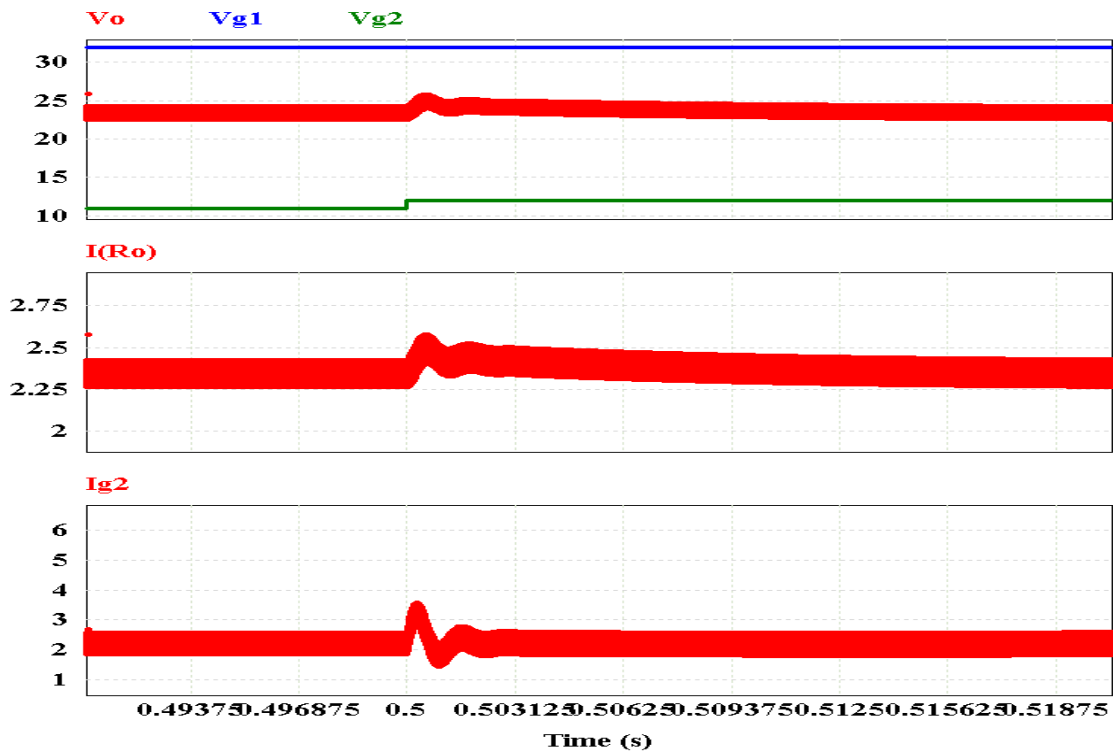


Fig. 4. 71 The variation of V_o , I_o , I_{g2} currents due to variation of V_{g2} : 12V to 14V

The simulation result is shown in Fig. 4.72 is plotted by fixing the source voltages at their rated value and the load resistance is varied from $10\ \Omega$ - $4\ \Omega$ at 0.8 secs, it was observed that the output voltage started to fall from 24V to 18V, and source-2 current varied from 2Amps to approximately 5A, shown in the figure below, meanwhile the duty ratios D_V and D_I are being altered so that the output voltage is driven to 24V in about 10mSec and similarly the current is regulated to the rated 2A, which proves the effectiveness of the designed SMQFT controllers

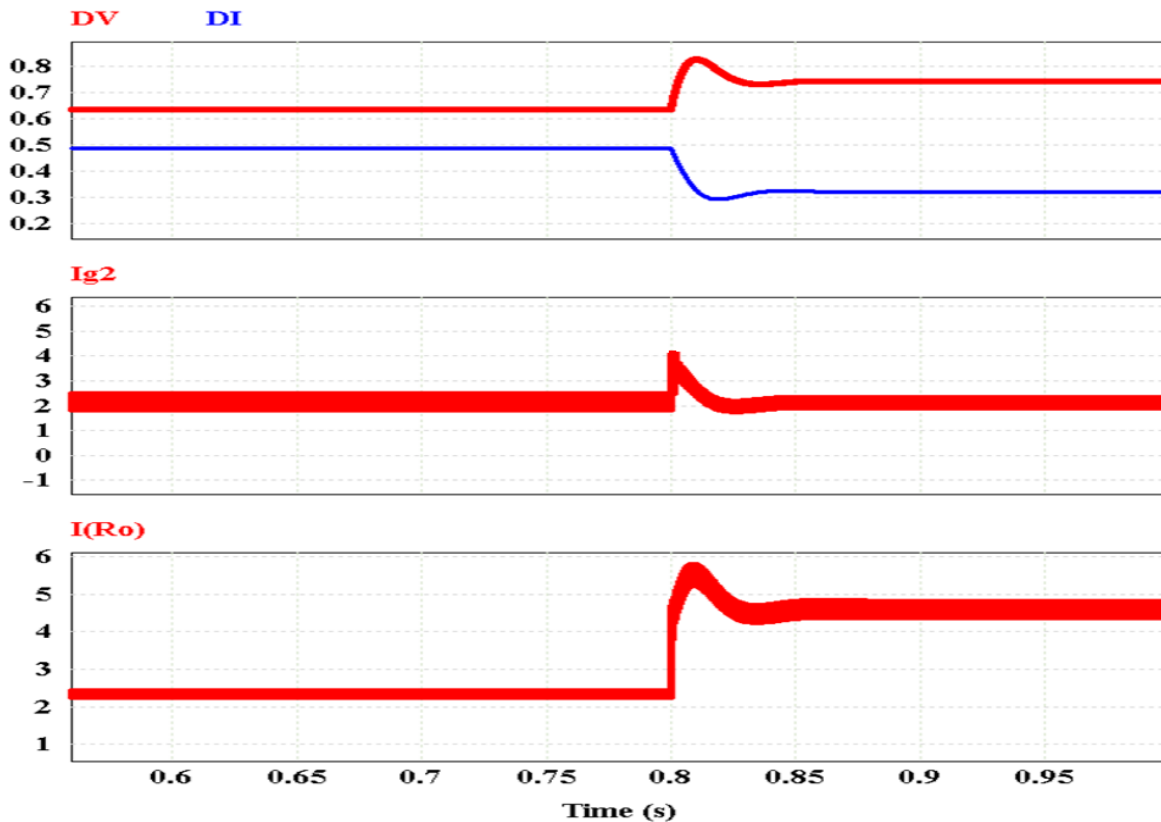


Fig. 4. 72 The variation of V_o , I_o , I_{g2} for variation in load R: $10\ \Omega$ - $4\ \Omega$

All the voltage variation combinations of V_{g1} and V_{g2} are tested, and the responses are shown in Figs. 4. 73, it may be observed from all of them that the duty ratio₂ remained same so that a constant current of 2A is drawn continuously from V_{g2} , and duty-ratio 'd₁' varied in all the

cases so that the voltage regulation is maintained constant at 24V, which proves that the output voltage is controlled by y_1 , and source-2 current (i_{g2}) is controlled by y_2 , this also proves the feasible pair identification from RGA matrix.

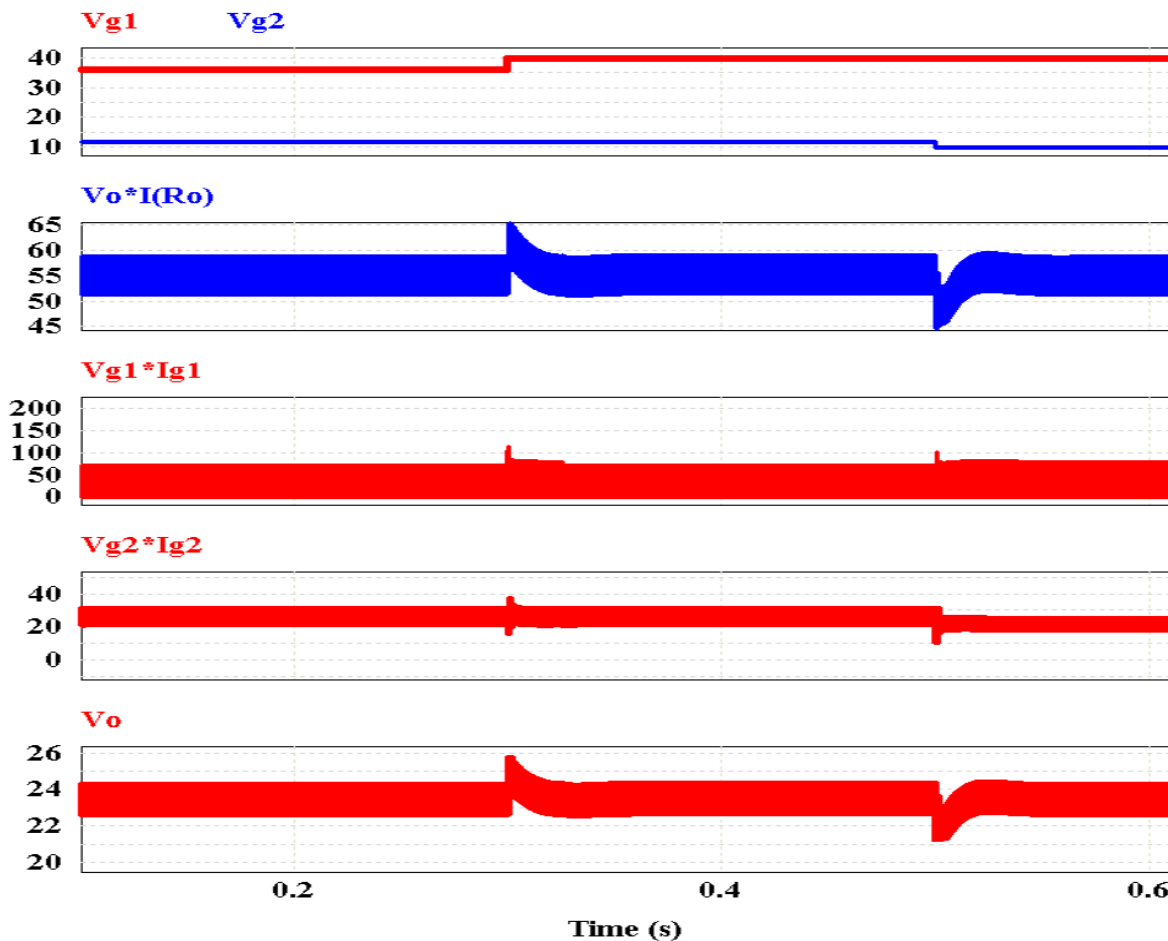


Fig. 4. 73 Power Management among the sources for variation in sources

similarly, during the load variation shown in Fig.4.72, both d_1 and d_2 got varied to maintain the voltage and current regulation during the load disturbance, this proves the efficacy of controller in attenuating the source and load disturbances, Fig. 4.73 shows the power management among the source and load during the source to regulate the voltage and current during the load disturbances.

4.5 Controllers design for SIHBSTIC Topology

Apart from designing ICD controllers for SIHBSTIC topology, an attempt is made to design another type controllers for SIHBSTIC topology. The values of RGA matrix of SIHBSTIC shown in Table 4.1, it is observed that the interactions are considerable, for designing the controllers two approaches were considered, first is based on the ICD mentioned in section 4.3.1 and another method based on non-inverted plant-based approach reported in [70], [71], [72], [73],[74],[75],[76],[79] were tried. So, a controller design reported in [74],[79] were considered initially for controller design. Designing diagonal controllers may not be a feasible solution due to the presence of the interaction among the loops, so an attempt is made to study the simplified decoupling controller design approaches of [54], and [74] are implement it with the QFT based controller design, because of the existence of the de-couplers between the loops, the voltage and current loops acts like two independent loops, this feature fortified to implement the Decoupled Decentralized MIMO QFT (DDMQFT) controller design technique. The block diagram of the controller is given in Fig. 4.74.

4.5.1 Decoupled Decentralized MIMO QFT control

The process of designing the diagonal controllers is the same as that of the process mentioned in section 4.4; the decouplers are designed in the DDMQFT process. In Two-input-Two-Output (TITO) decoupled-Decentralized QFT control, the relationship of input and output vector is given by:

$$Y(z) = G(z)D(z)U(z) \quad (4.48)$$

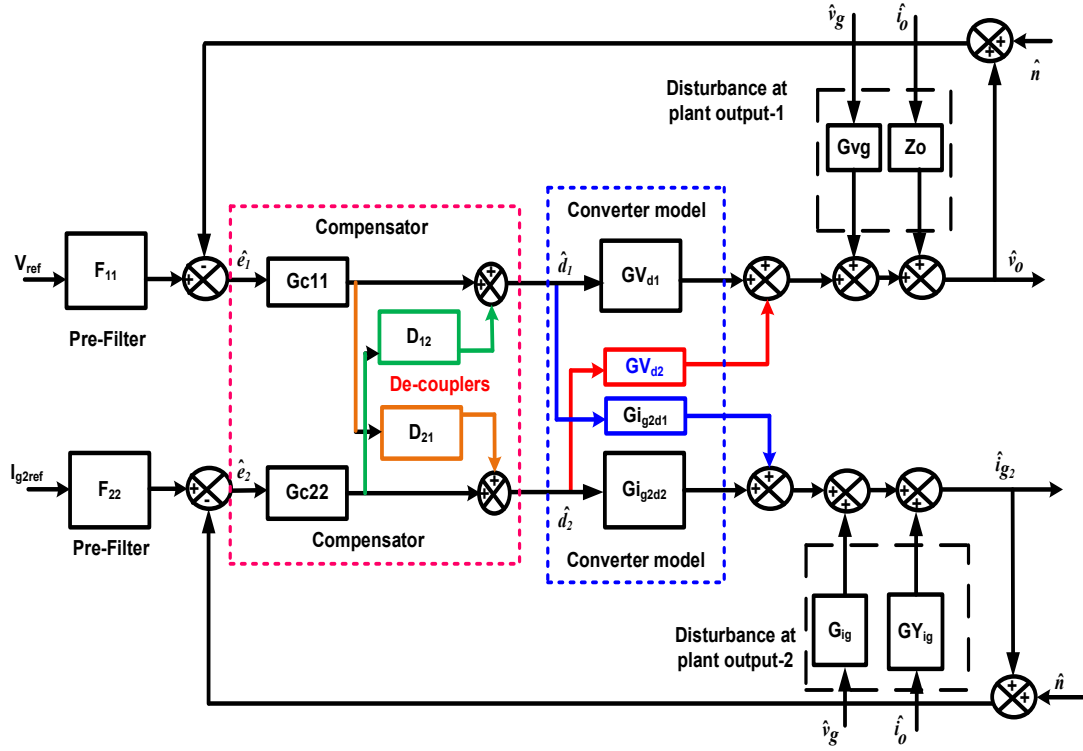


Fig. 4. 74 Small-Signal block diagram of closed-loop control of a 2DOF TITO system.

Where $Y(z)$ is the Output Vector, $G(z)$ is the plant TFM, $D(z)$ is the de-coupler Matrix, $U(z)$ is the control duty ratio matrix.

The TITO SIHBS system with diagonal controllers is represented in the form of eq. 4.49

$$\begin{bmatrix} \hat{v}_0(z) \\ \hat{i}_g(z) \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} 1 & D_{12} \\ D_{21} & 1 \end{bmatrix} \begin{bmatrix} \hat{d}_1(z) \\ \hat{d}_2(z) \end{bmatrix} \quad (4.49)$$

The Controllers are represented as shown below:

$$\begin{bmatrix} G_{C11}^* & 0 \\ 0 & G_{C22}^* \end{bmatrix} = G(z)D(z) \quad (4.50)$$

$$\begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} 1 & D_{12} \\ D_{21} & 1 \end{bmatrix} = \begin{bmatrix} G_{C11}^* & 0 \\ 0 & G_{C22}^* \end{bmatrix} \quad (4.51)$$

The de-couplers represented as are designed using the ratio of off-diagonal transfer functions as per the methodology presented in [75], the equations are shown in eq.s 4.52, 4.53.

$$D_{12}(z) = \frac{-G_{12}(z)}{G_{11}(z)} \quad (4.52)$$

$$D_{21}(z) = \frac{-G_{21}(z)}{G_{22}(z)} \quad (4.53)$$

Because of existence of the de-couplers, the TITO-SIHBSC voltage and current loops acts like two independent loops, similar to the decentralized system, controllers are then designed individualistically, expressed as [74]:

$$G_{C11}^*(z) = \frac{\hat{v}_o(z)}{\hat{d}_1(z)} = G_{11}(z) - \frac{G_{12}(z)G_{21}(z)}{G_{22}(z)} \quad (4.54)$$

$$G_{C22}^*(z) = \frac{\hat{v}_o(z)}{\hat{d}_2(z)} = G_{22}(z) - \frac{G_{12}(z)G_{21}(z)}{G_{C11}(z)} \quad (4.55)$$

The specifications mentioned in Table 4.6, 4.7, 4.8 are considered for synthesizing the decoupled controllers for SIHSBSTIC.

Table 4. 6 SIHBSTIC Bound Specifications

Specifications	Voltage Loop	Current Loop
Gain Margin	8dB	10dB
Phase Margin	50 degrees	45 degrees
Overshoot	20%	20%
Gain Margin bound	1.25	1.13

Table 4. 7 SIHBSTIC Source and load variations

Parameter	Variation
Source-1 Vg1	36V \pm 10%
Source-2 Vg2	12V \pm 20%
Load Resistance R	10 Ω \pm 50%

Table 4. 8 Robust Performance Specifications

Specification	VMC, CMC
Sensitivity (S)	$\frac{1}{1+L(z)} \leq \delta_s$
Tracking	$T_L(z) \leq \frac{L}{1+L} \leq T_U(z)$
Modulus Margin (MM)	$1/MM = 1/ 1+L _{\min} = S _{\max} \leq 2$

The upper and lower tracking bound transfer functions are given in eq's. 4.56, 4.57:

$$T_U = \frac{0.024892 (z-0.9987) (z-0.779)}{(z-0.9982) (z-0.9881) (z-0.6756)} \quad (4.56)$$

$$T_L = \frac{7.4474e-08 (z+3.704) (z+0.2659)}{(z-0.9977) (z-0.9863) (z-0.9859)} \quad (4.57)$$

The procedure of synthesizing controller is the same as that of the previous controller design method, for realizing diagonal controllers, eq. 4.56 to 4.57 were used for generating tracking bounds, and the following specifications are considered for design:

1. The frequency array FA: $w=2*pi*[1 \ 100 \ 500 \ 1e3 \ 2e3 \ 5e3 \ 10e3 \ 20e3 \ 25e3]$;
2. The nominal plant is selected as the 10th Plant.
3. Uncertainty Template Plot of the equivalent diagonal plants

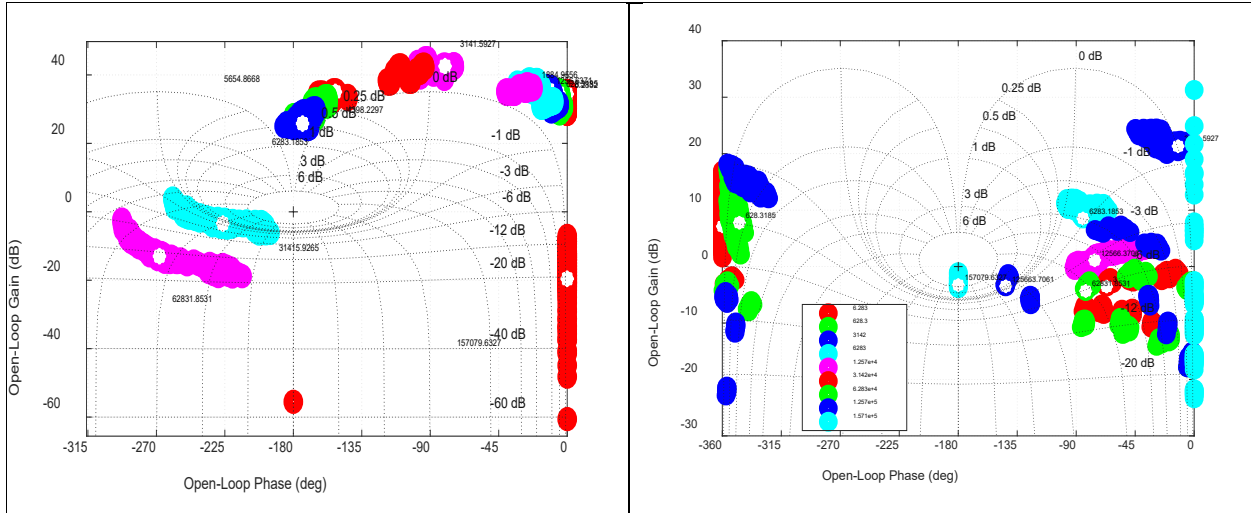


Fig. 4.75 Template plots of G_{11eq} , G_{22eq}

Gain and Phase margin Bound.

GM of 10dB and PM of 45° . $\sigma_{GM}=0.65$ which corresponds 8dB GM, and $\sigma_{PM} = 1.25$ for 45° PM

$$GM=20 \log_{10} \left\{ \frac{\sigma+1}{\sigma} \right\} \text{ dB} \tag{4.58}$$

$$PM=2 \sin^{-1} \left\{ \frac{1}{2\sigma} \right\} \text{ deg} \tag{4.59}$$

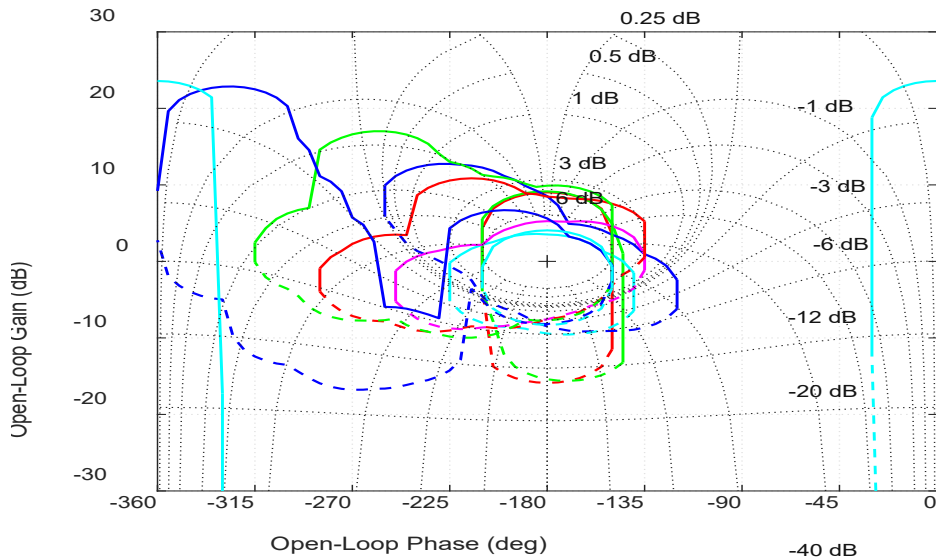


Fig. 4.76 Modulus Margin Bounds voltage-loop

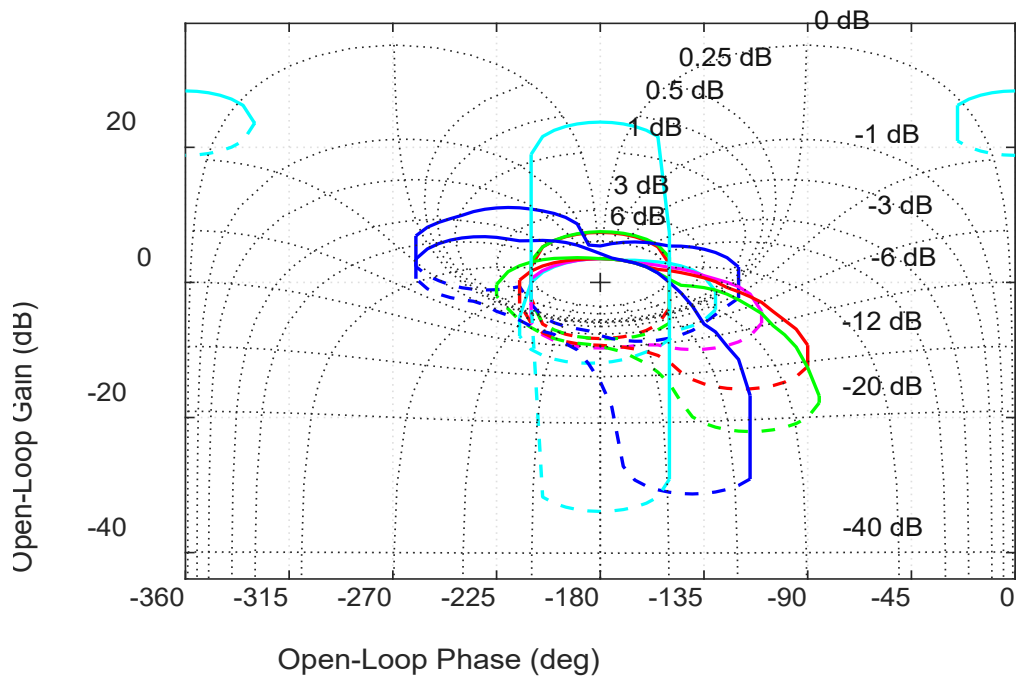


Fig. 4.77 Modulus Margin Bounds current-loop

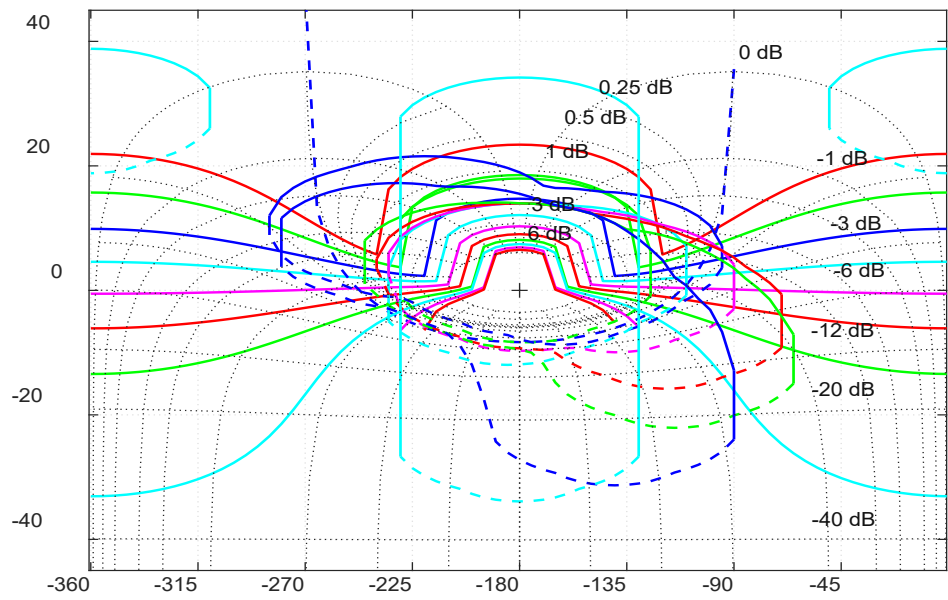


Fig. 4.78 Composite bounds of loop-1

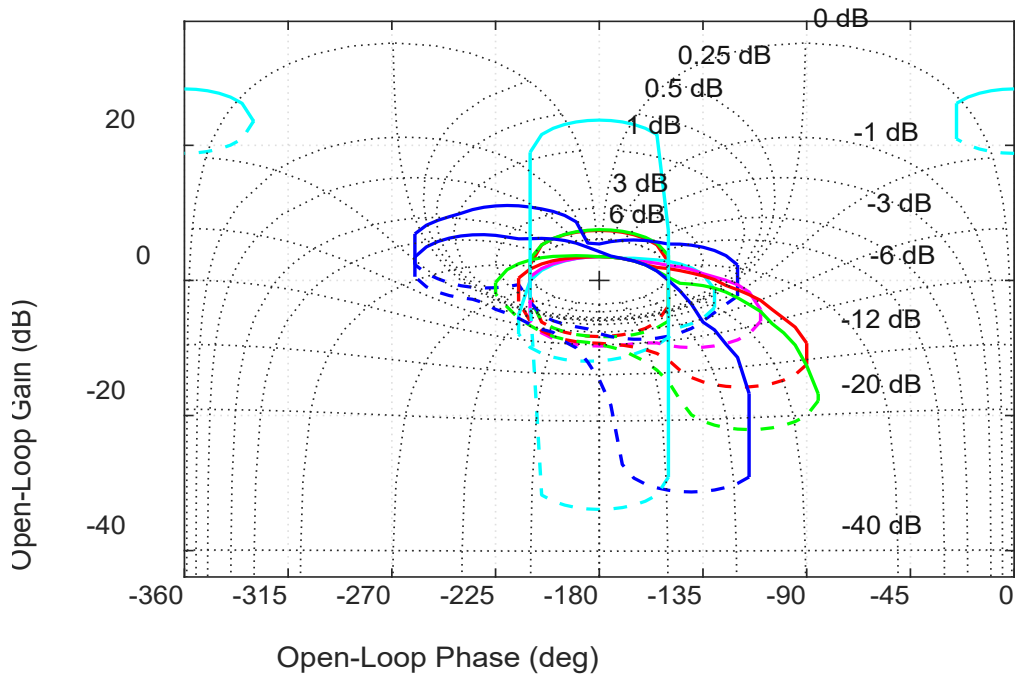


Fig. 4.79 Composite bounds of loop 2

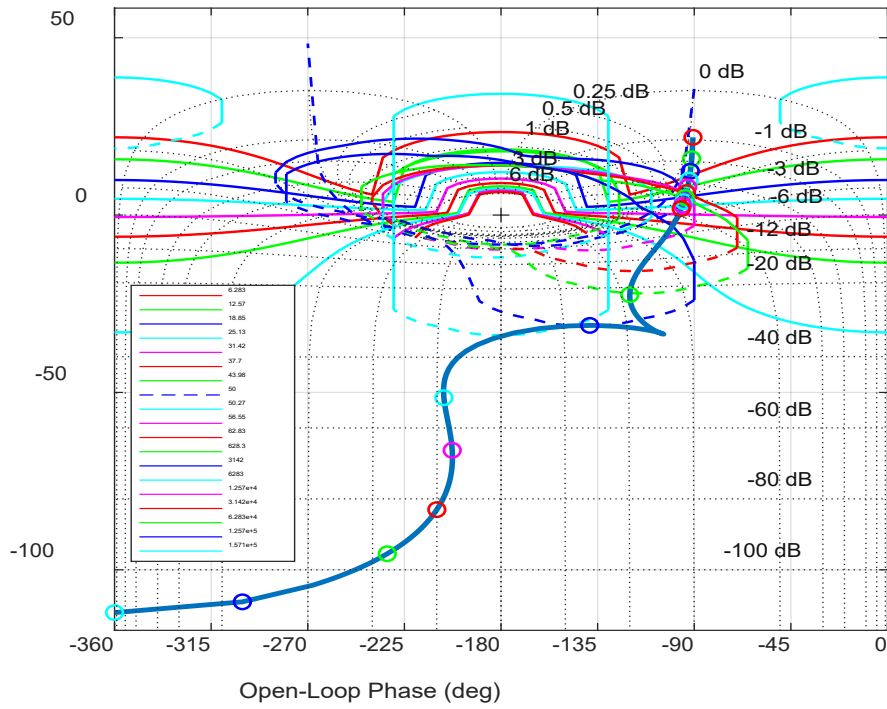
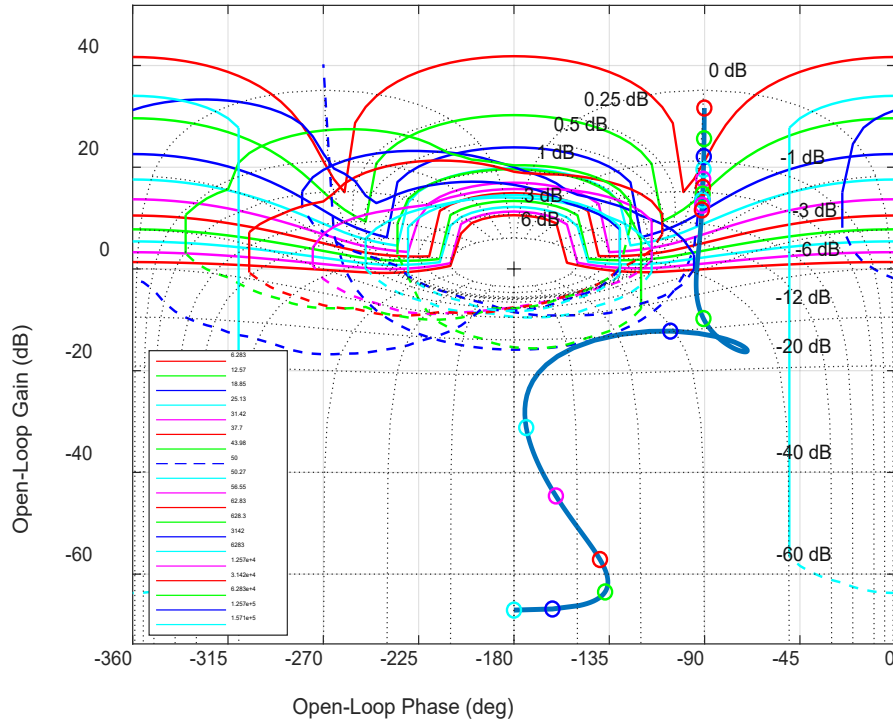


Fig. 4.80 Loop-shaping controller design plot of the Voltage control loop, current control loop



Furthermore, the respective pre-filters are designed and given in eqs. 4.62, 4.63

$$F_1 = \frac{0.6714 (z-0.9829)}{(z-0.9885)} \quad (4.62)$$

$$F_2 = \frac{1.4363 (z-0.998)}{(z-0.9972)} \quad (4.63)$$

From the off-diagonal elements of TFM G_{12} and G_{21} , the de-couplers d_{12} and d_{21} are designed in eq.s 4.64 and 4.65 below:

$$d_{12} = \frac{0.80412 (z-0.9624)}{(z-0.9642)} \quad (4.64)$$

$$d_{21} = \frac{0.3397 (z-1.394)}{(z-0.8388)} \quad (4.65)$$

On obtaining required controllers, pre-filters and decouplers, from eq.s (4.62) to (4.65), the time-domain simulations are done. The figures given in Figs. 4.82 to 4.89 are the frequency response verification bounds to verify the robust stability, sensitivity, and uncertainty set variation. All the uncertainty variations are within the respective bounds, which prove the effectiveness of the controller design.

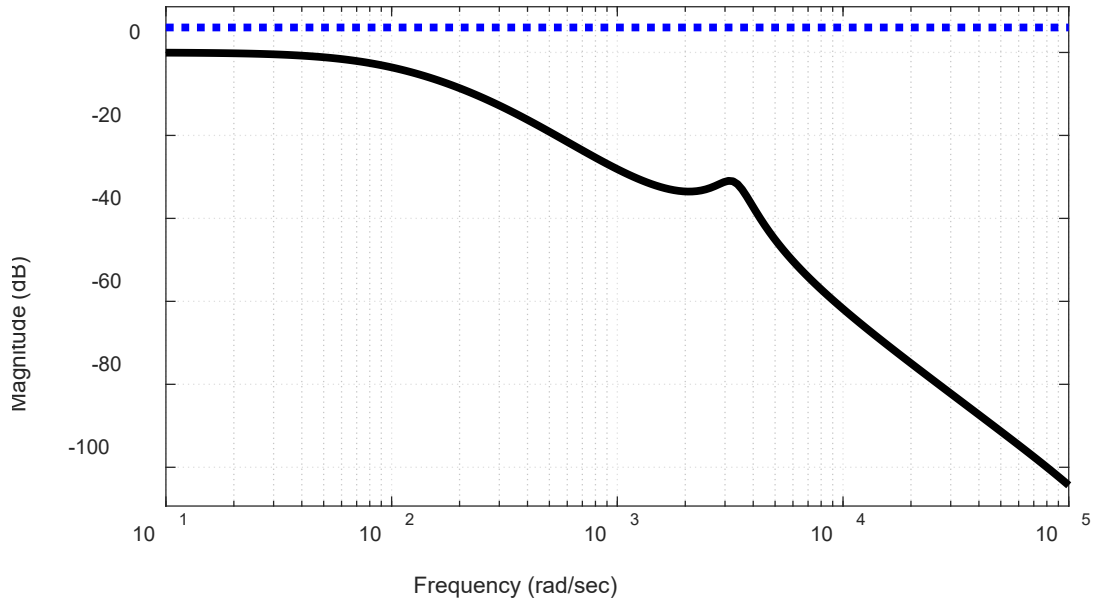


Fig. 4. 82 Robust Stability verification of Voltage control loop

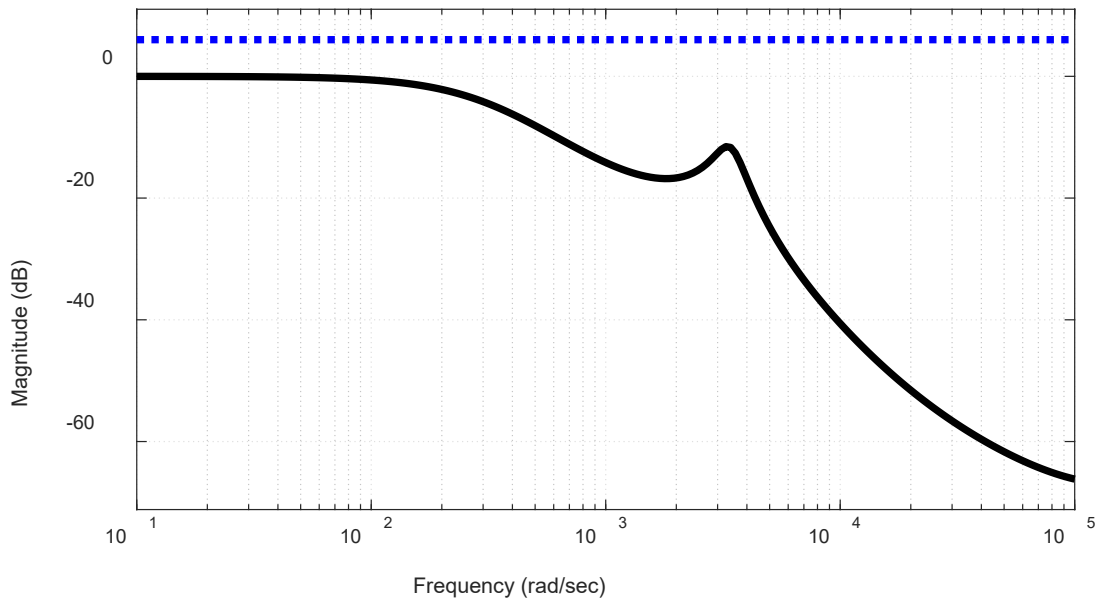


Fig. 4. 83 Robust Stability verification of current control loop

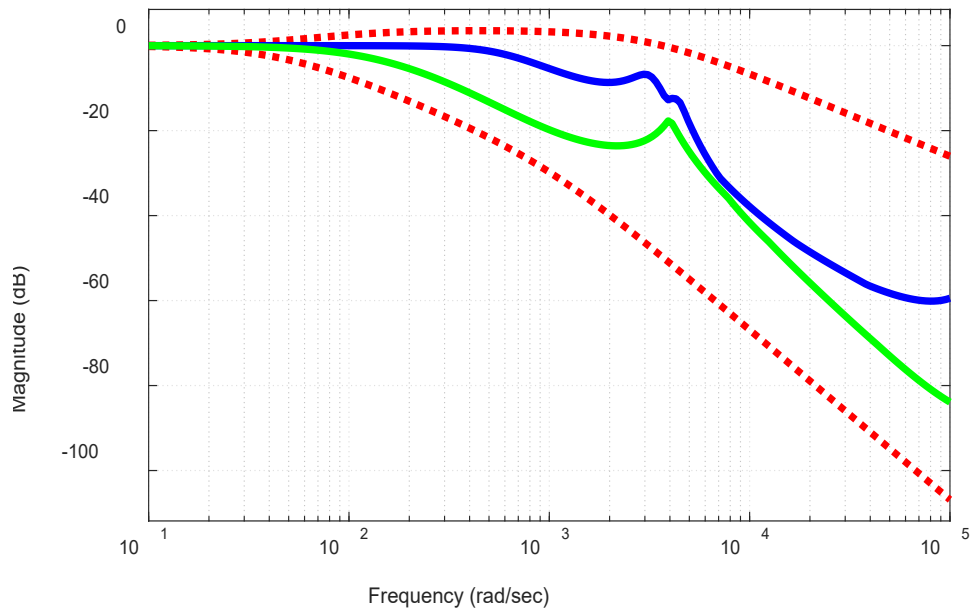


Fig. 4. 84 Closed-loop frequency response verification of uncertainty set Voltage control loop

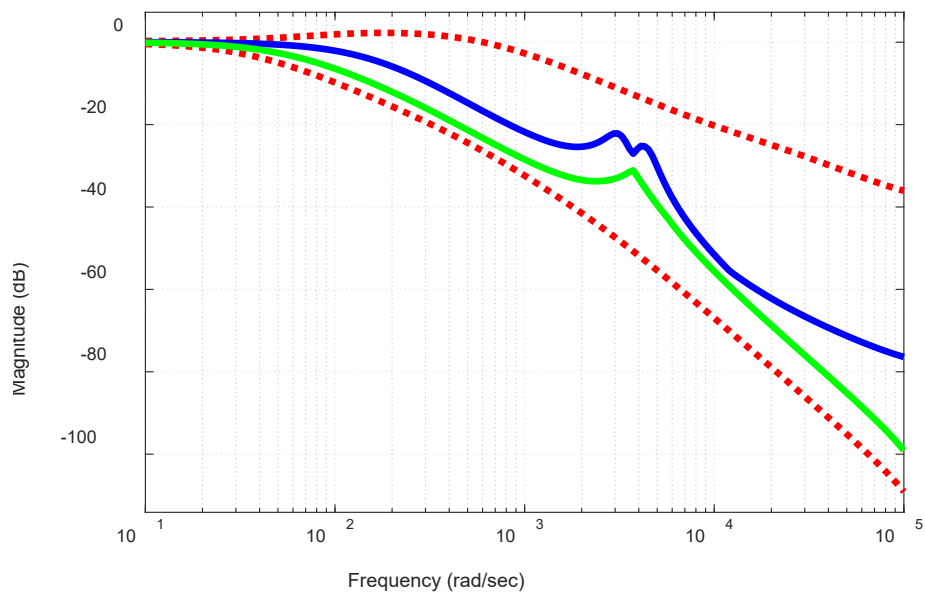


Fig. 4. 85 Closed-loop frequency response verification of uncertainty set current control loop

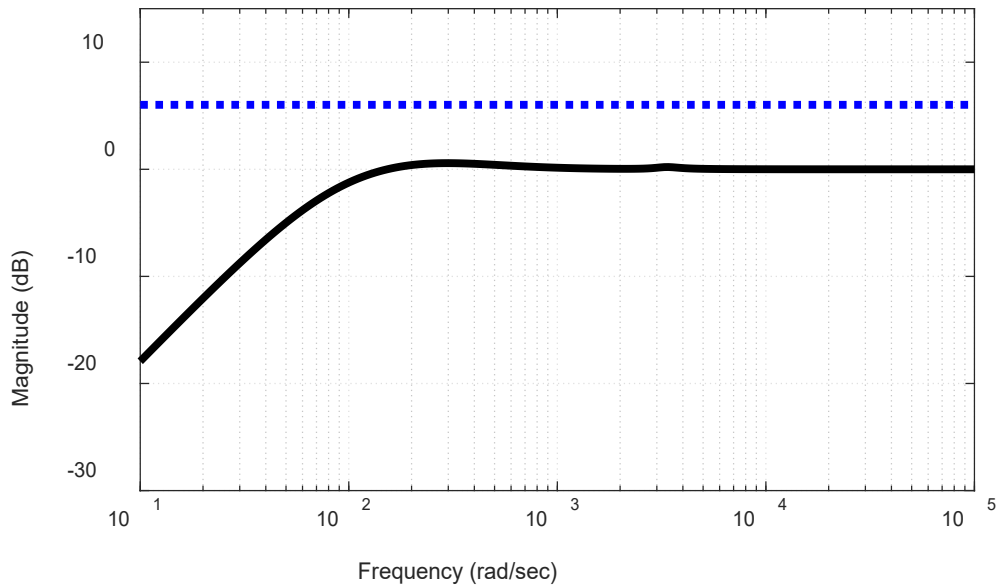


Fig. 4. 86 Closed-loop frequency response verification of voltage control loop

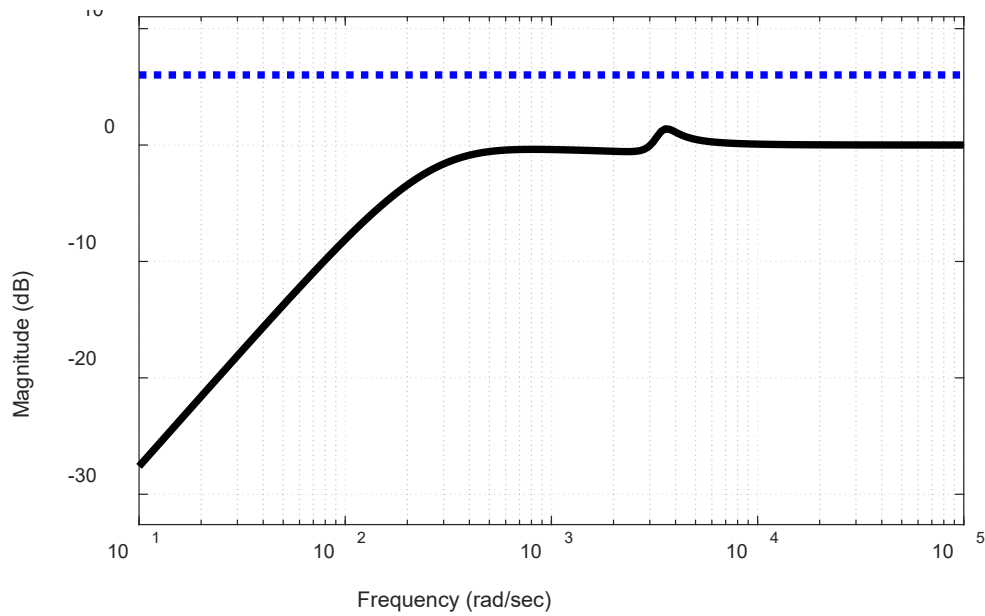


Fig. 4. 87 Closed-loop frequency response with pre-filter of the current control loop

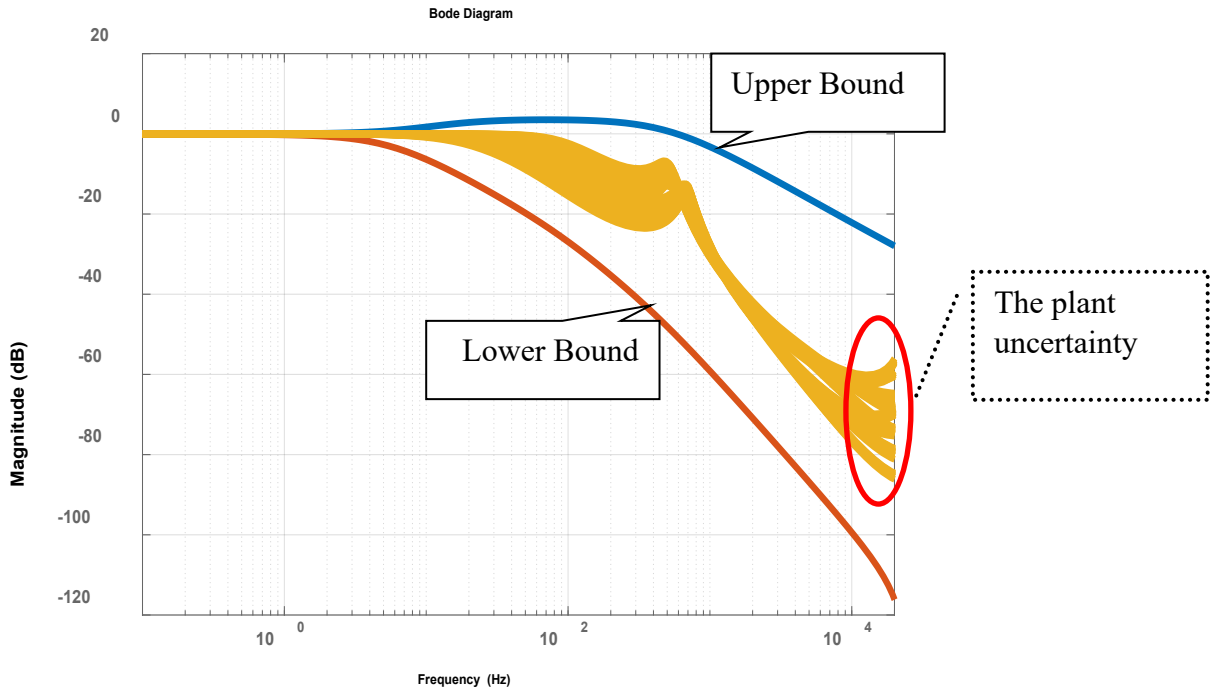


Fig. 4. 88 Closed-loop frequency response of Voltage control loop for uncertainty set

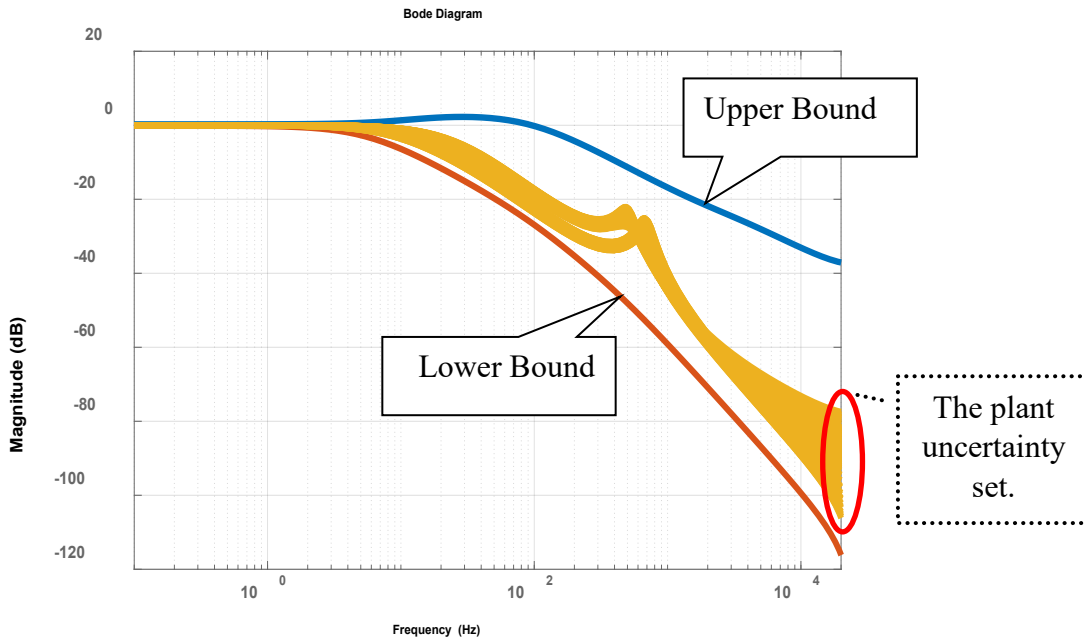


Fig. 4. 89 Closed-loop frequency response current control loop for uncertainty set

The effectiveness of the DDMQFT controller is demonstrated for a 36/12V, 96W prototype SIBSTIC for testing the voltage, current regulation and checking the robustness against the source/load variations. After designing the DDMQFT controllers for SIBSTIC, a series of simulations are carried out to validate the effectiveness of the controller in attaining the output voltage regulation and source current regulation. For the uncertainty set mentioned in Tables 4.5 to 4.7, of section 4.6 and the following results are obtained. The simulation result is shown in Fig. 4.79 for the steady-state waveforms, Fig. 4.80 shows the plot of the voltage and load currents, which is plotted by fixing the source voltages at their rated value and the load resistance is varied from 8Ω - 2Ω at 0.8 secs, it was observed that the output voltage started to fall from 24V to 14V, and source-2 current varied from 2Amps to approximately 8A, shown in the figure below, meanwhile the duty ratios D_v and D_i are being altered so that the output voltage is driven to 24V in about 10mSec and similarly the current is regulated to the rated 2A, which proves the effectiveness of the designed DDMQFT controllers.

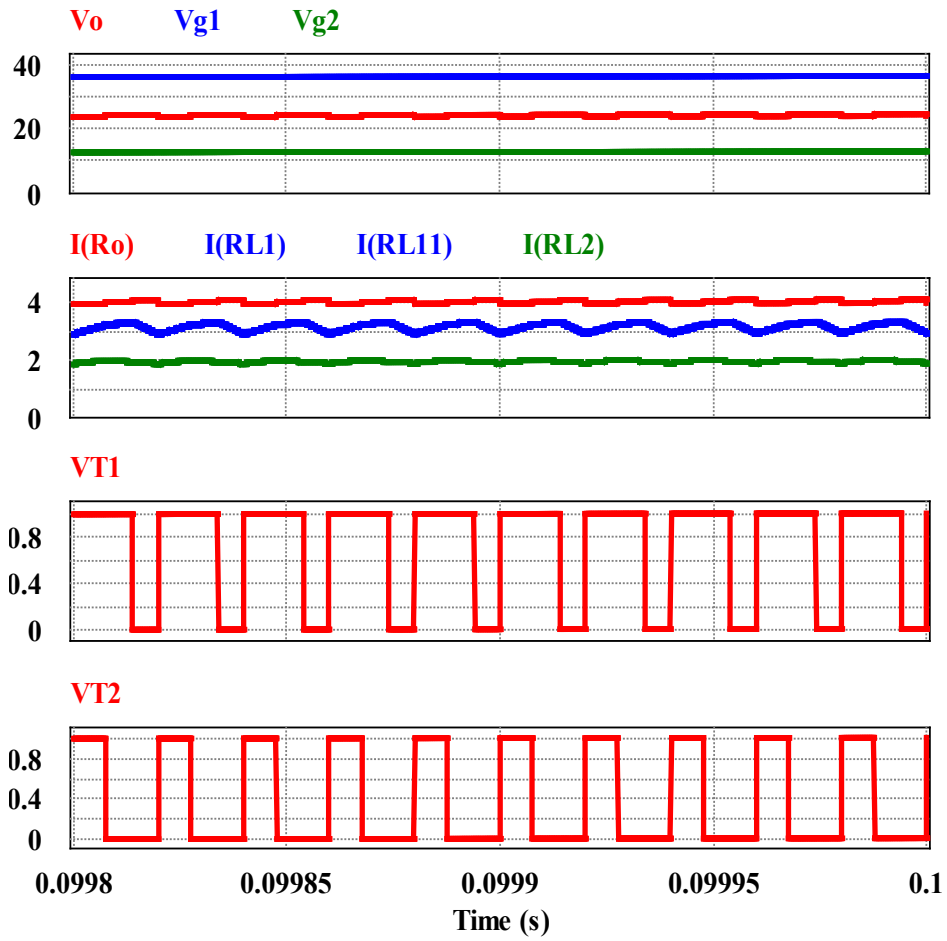


Fig. 4. 90 Steady-state waveforms of SIHBSTIC

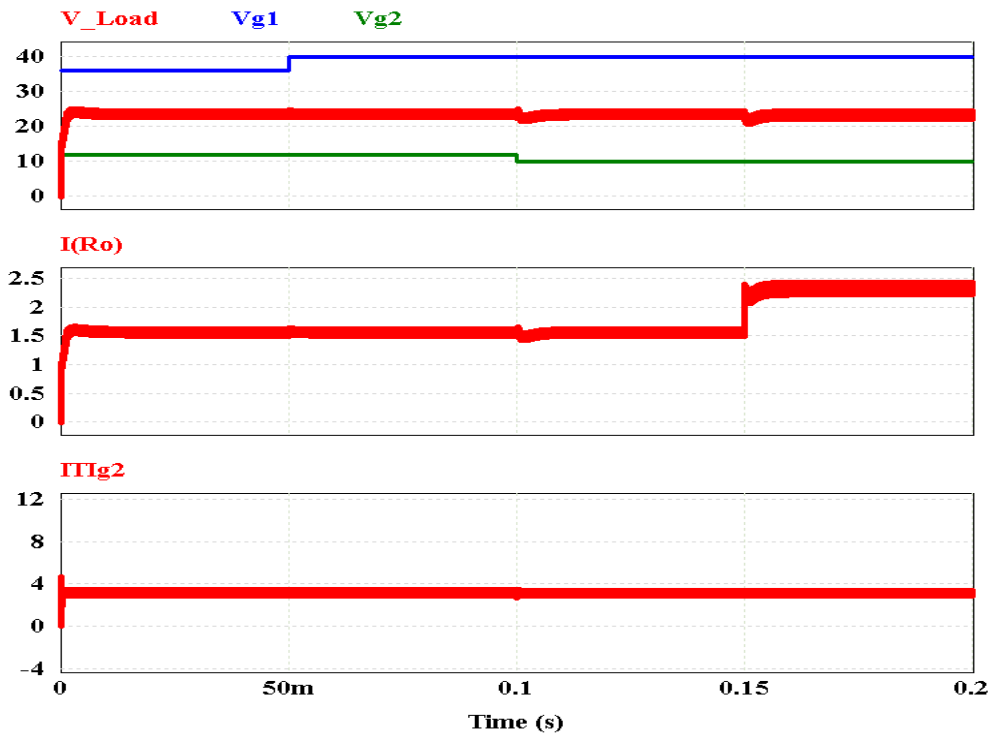


Fig. 4. 91 The variation of V_o , I_o , I_{g2} currents due to variation of V_{g1} : 36 to 40V



Fig. 4. 92 The variation of V_o and I_{g2} currents when V_{g2} : 12V to 10V

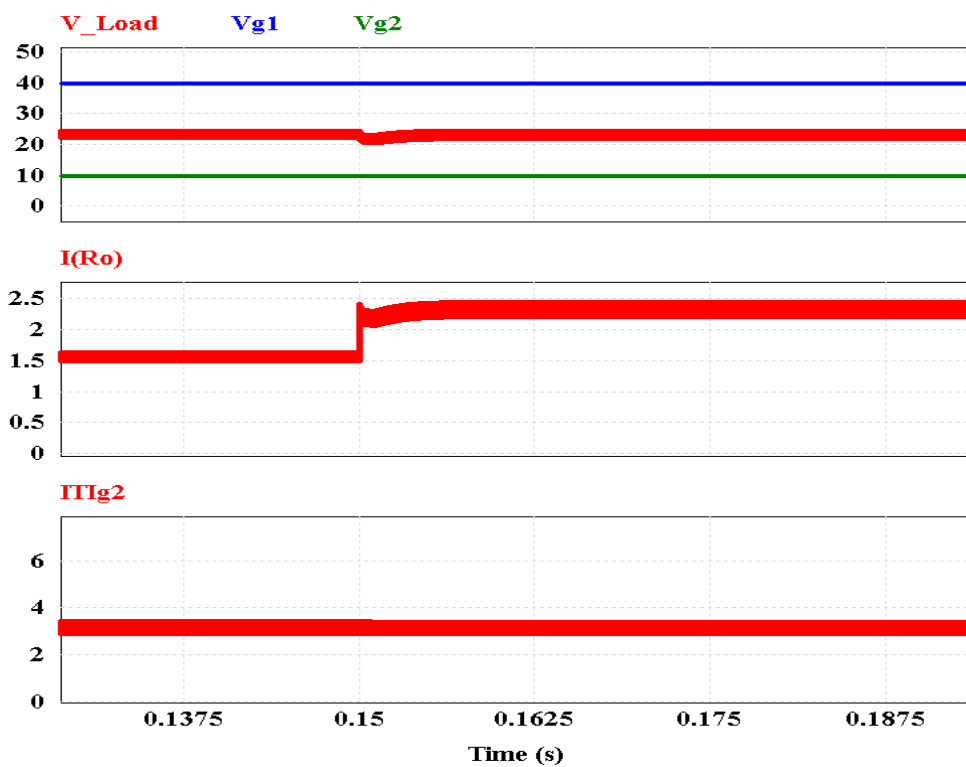


Fig. 4. 93 The variation of V_o , I_o , I_{g2} currents with Load Variation form 10 Ω to 5 Ω
 (I_{g2} is same as I_{RL2} for all figures)

4.5.2 Results of ICD control based design

Apart from working on DDMQFT controllers, the simulation is also performed for SIHSBSTIC using the controllers obtained from ICD technique mentioned in section 4.3.1, and following waveforms for various perturbations in source-1,2 and load variations were obtained as shown in Figs. 4.94 to 4.96. The controller is found effective in reducing the perturbations in source-1,2 voltages and load resistance variation in about 0.2ms. The ICD technique was found to be effective when compared to DDMQFT approach for this topology.

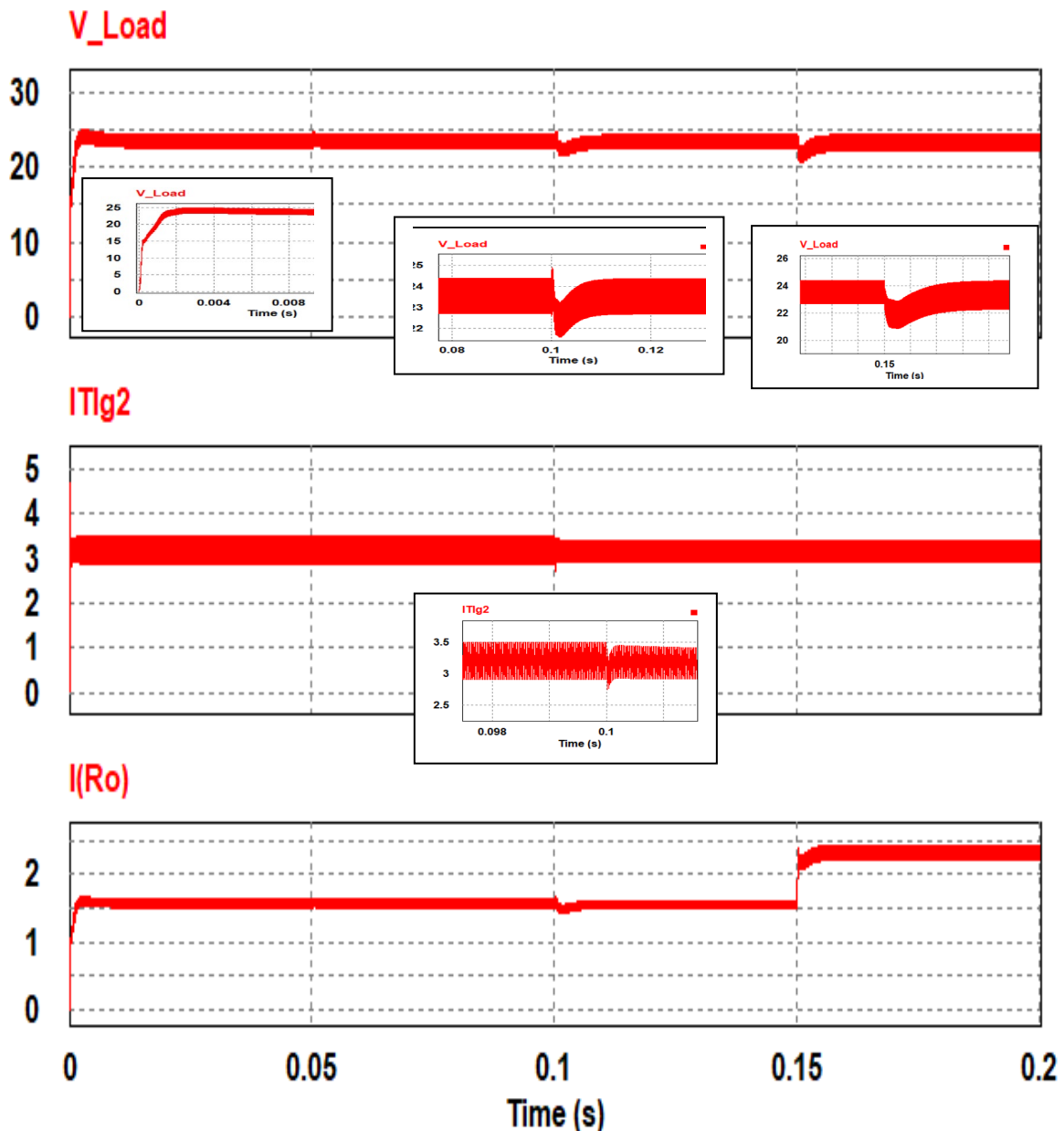


Fig. 4.94 Dynamic response of the SIHSBSTIC, the variation of Output Voltage V_o , Output Current I_o , and source-2 current I_{g2} currents are plotted with variations of Source-1 voltage from 32V to 36V at 50ms, voltage of source-2 from 12V to 10V at 0.1s, and Load from $10\ \Omega$ to $5\ \Omega$ at 0.15s using ICD controller

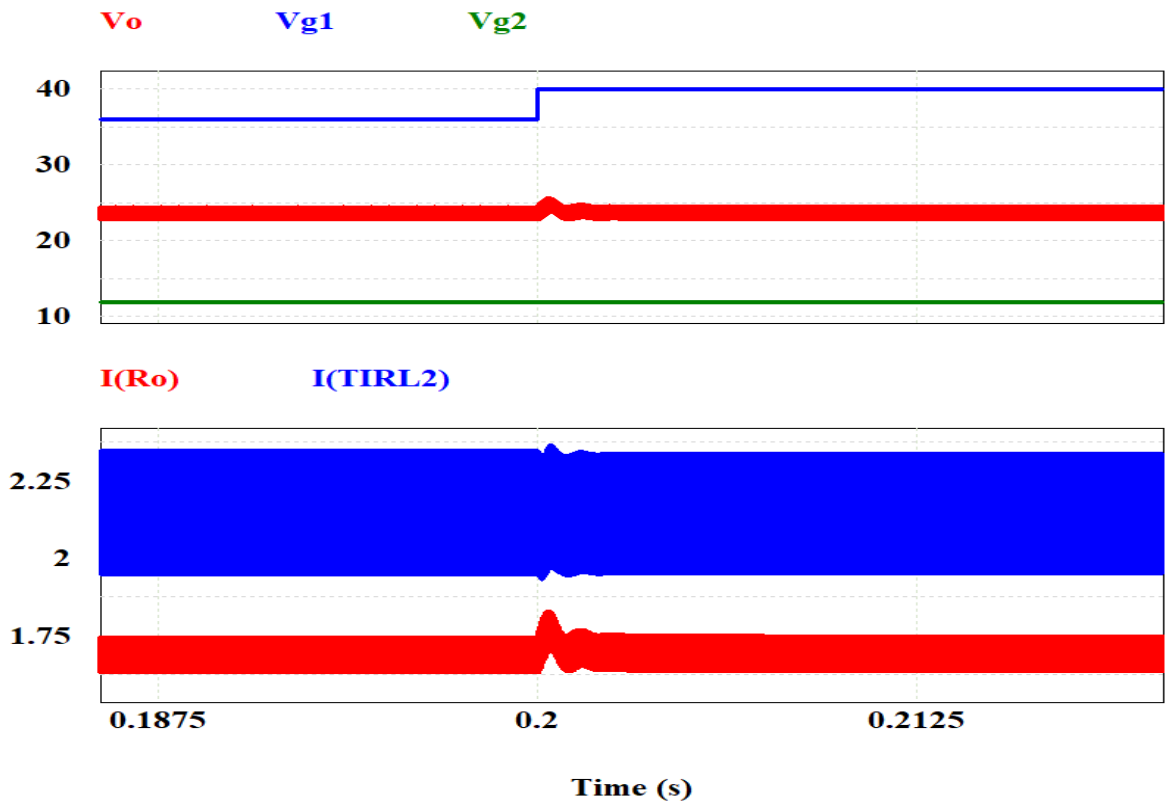


Fig. 4. 95 Dynamic response of the SIHBSTIC, the variaton of V_o , I_o , I_{g2} currents due to varaiton of V_{g1} : 36 to 40V using ICD controller

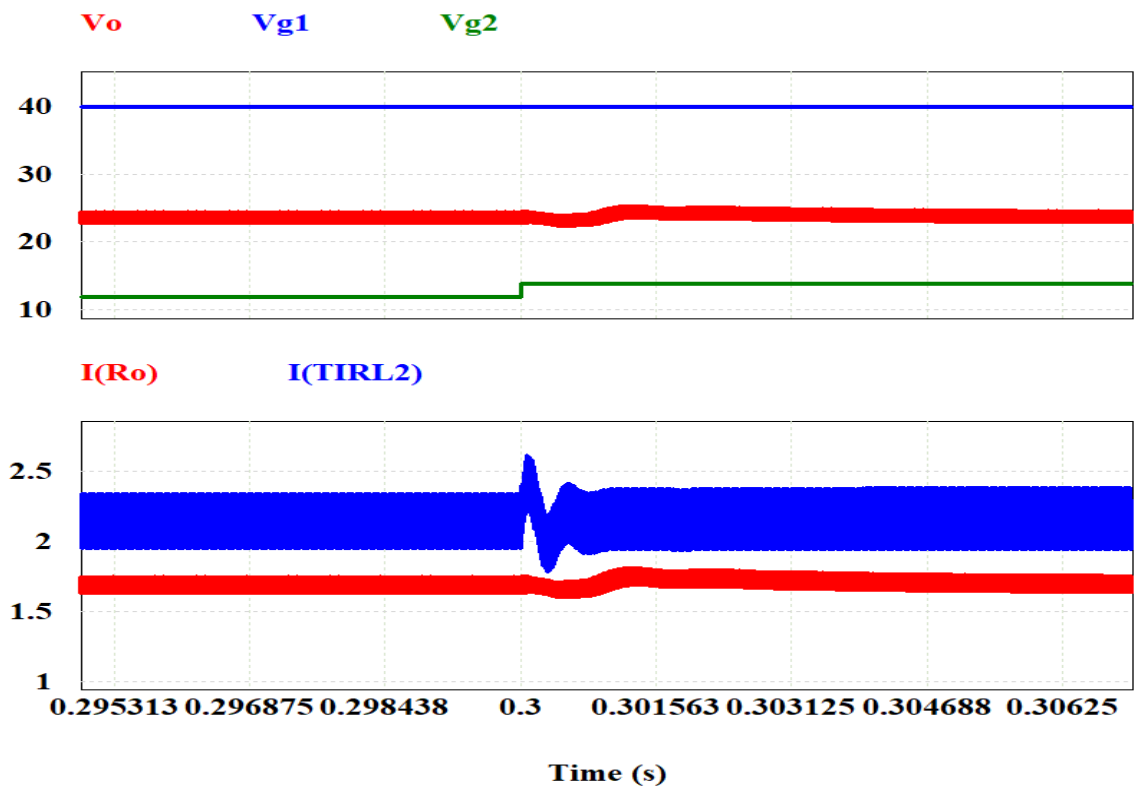


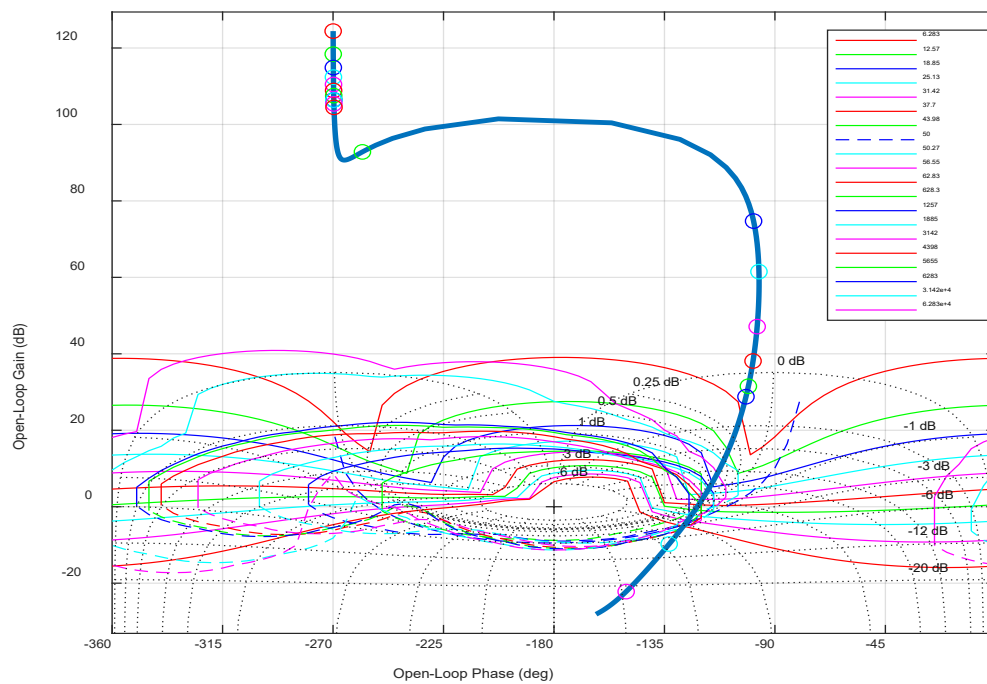
Fig. 4. 96 Dynamic response of the SIHBSTIC, the variation of V_o and I_o , I_{g2} currents when V_{g2} is varied from 12V to 14V at time 0.3s using ICD controller

4.6 Controller Design of SCHBSTIC1

In the similar lines, the Decoupled-Decentralized MIMO QFT controller design discussed in section 4.6.1 is applied to SCHBSTIC1 to obtain the controllers shown below in table 4.9, and the controller loop shaping graphs are shown in Figs. 4.97 and 4.98, followed by the verification plots shown in Figs. 4.99 to 4.104.

Table 4. 9 Controllers and decouplers of SCHBSTIC-1

Voltage Loop Controller	Current Loop Controller
$G_{c11} = \frac{0.47415 (z-0.4326)}{(z-1)}$	$G_{c22} = \frac{0.1997 (z-0.8355)}{(z-1)}$
$d_{12} = \frac{0.2394 (z-0.9578)}{(z-1)}$	$d_{21} = \frac{0.467 (z-0.9858)}{(z-1)}$



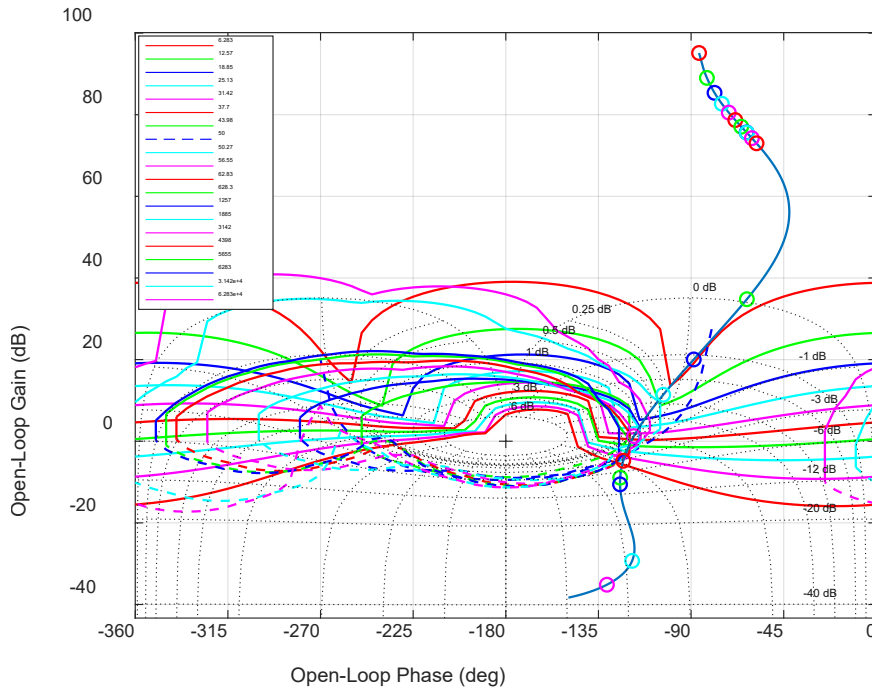


Fig. 4. 98 Loop-shaping controller design plot of the current control loop

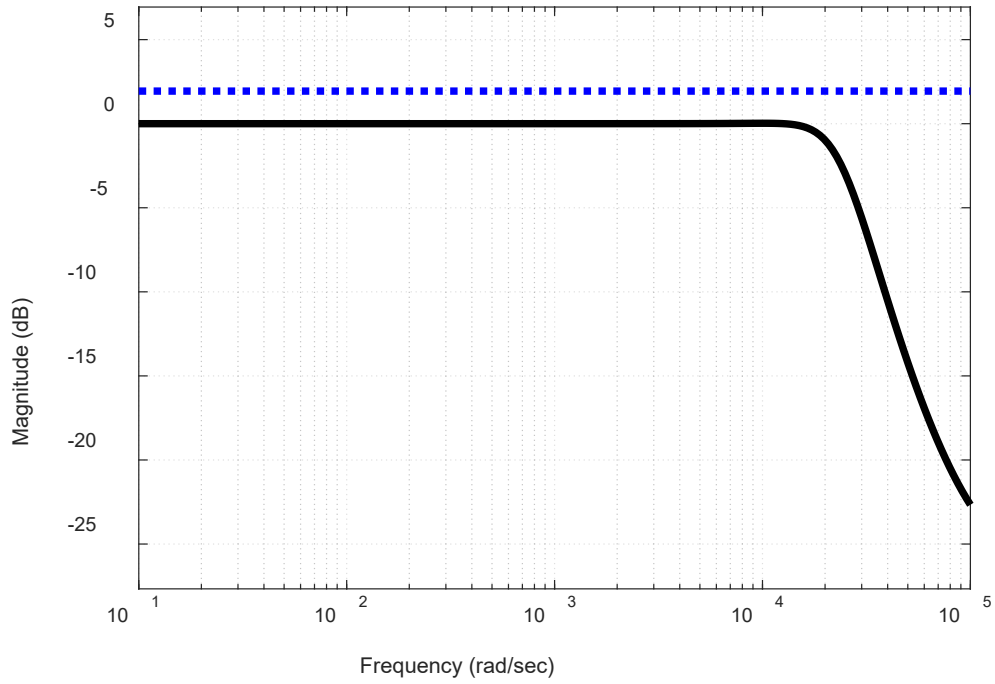


Fig. 4. 99 Frequency response of the Robust control verification bounds of the Voltage loop

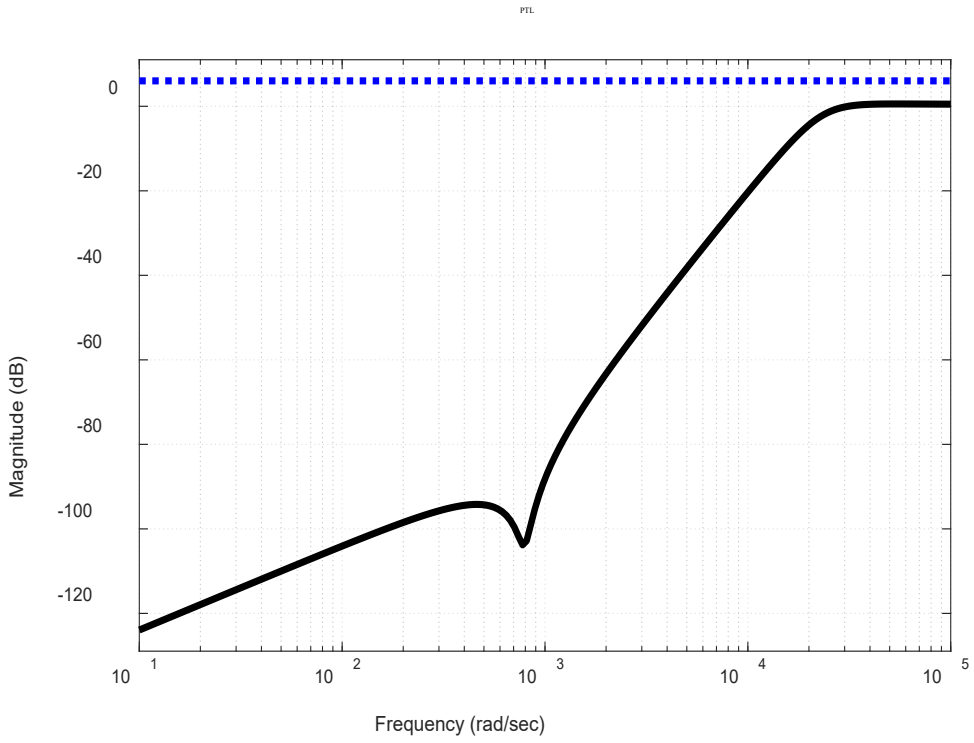


Fig. 4. 100 Frequency response of the sensitivity verification bounds of the Voltage loop

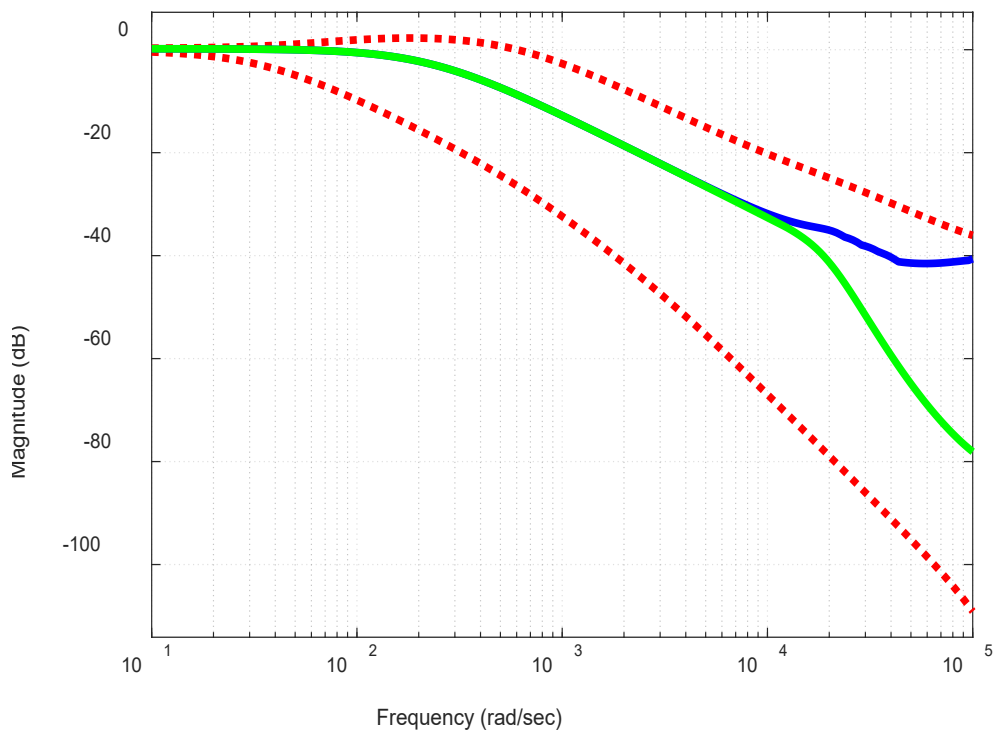


Fig. 4. 101 Closed-loop frequency response verification of uncertainty set of the voltage control loop

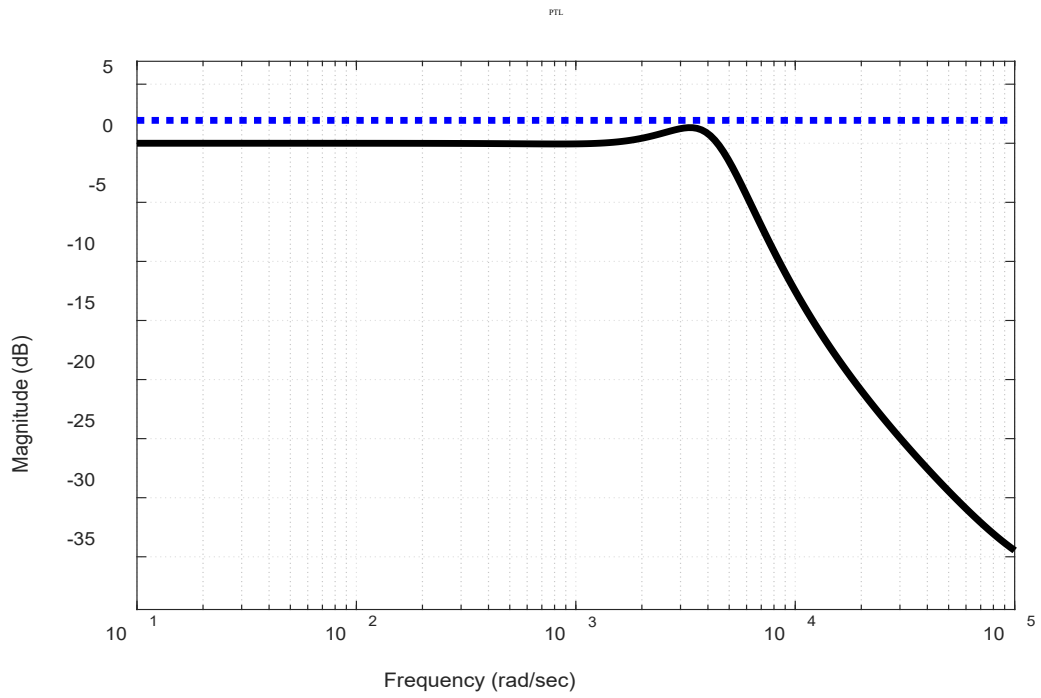


Fig. 4. 102 Frequency response of the Robust control verification bounds of Current loop

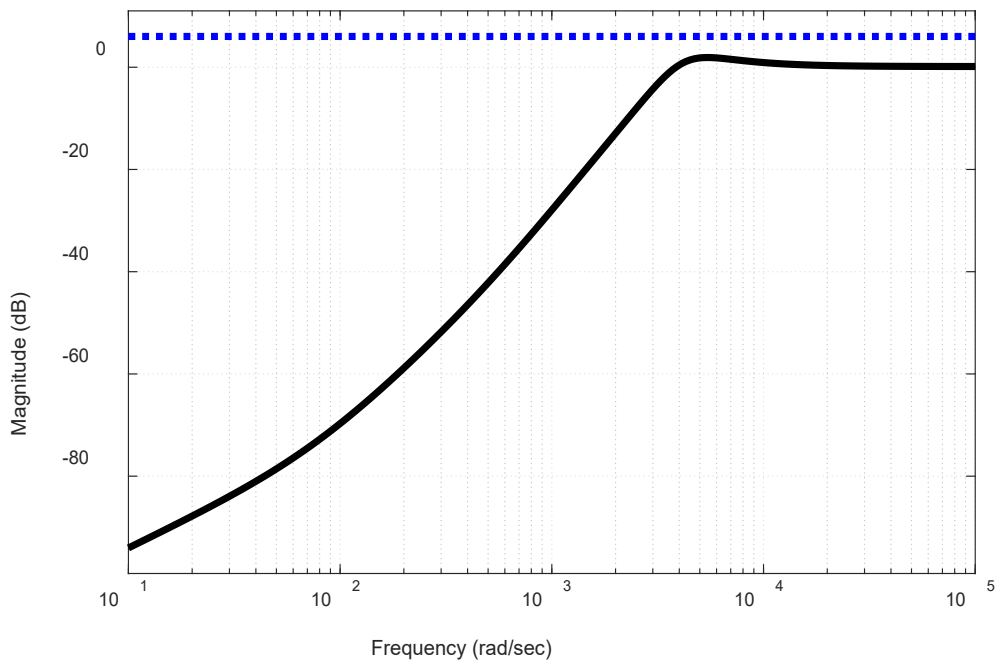


Fig. 4. 103 Frequency response of the sensitivity verification bounds of the Voltage loop

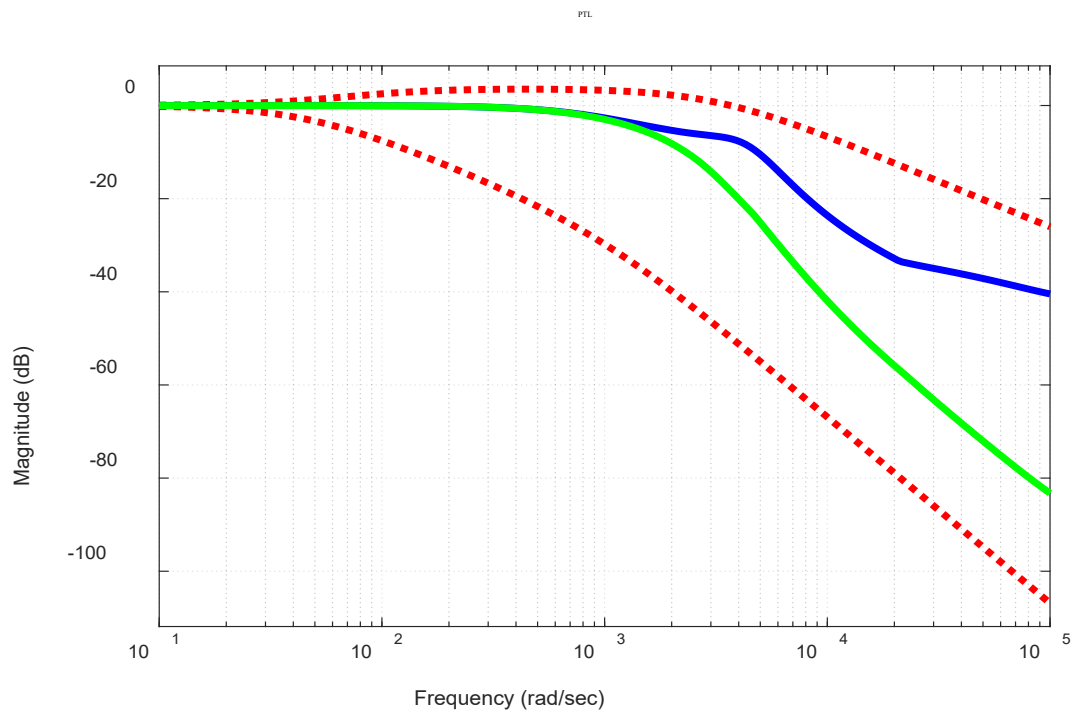


Fig. 4. 104 Closed-loop frequency response verification of uncertainty set current control loop

The effectiveness of the DDMQFT controller is demonstrated for a 36/12V, 96W prototype SCBSTIC1 for testing the voltage, current regulation and checking the robustness against the source/load variations. After designing the DDMQFT controllers for SCBSTIC1, a series of simulations are carried out to validate the effectiveness of the controller in attaining the output voltage regulation and source current regulation. For the uncertainty set mentioned in Tables 4.6 to 4.8, of section 4.6 and the following results are obtained. The simulation result is shown in Fig. 4.105 is plotted for the steady-state waveforms, dynamic response of the SCHBSTIC-1 is shown in Fig, 106, for the variation of source-1 voltage V_{g1} : 32V to 36V, source-2 voltage V_{g2} : 12V to 10V, and load resistance 10Ω to 5Ω , the Output Voltage (V_o), Source Current (I_{g2}), Output current I_o are plotted. It is observed that the output voltage is driven to 24V in about 10mSec and similarly the current is regulated to the rated 2A, shown in Fig. 107, proves the efficacy of the designed DDMQFT controllers.

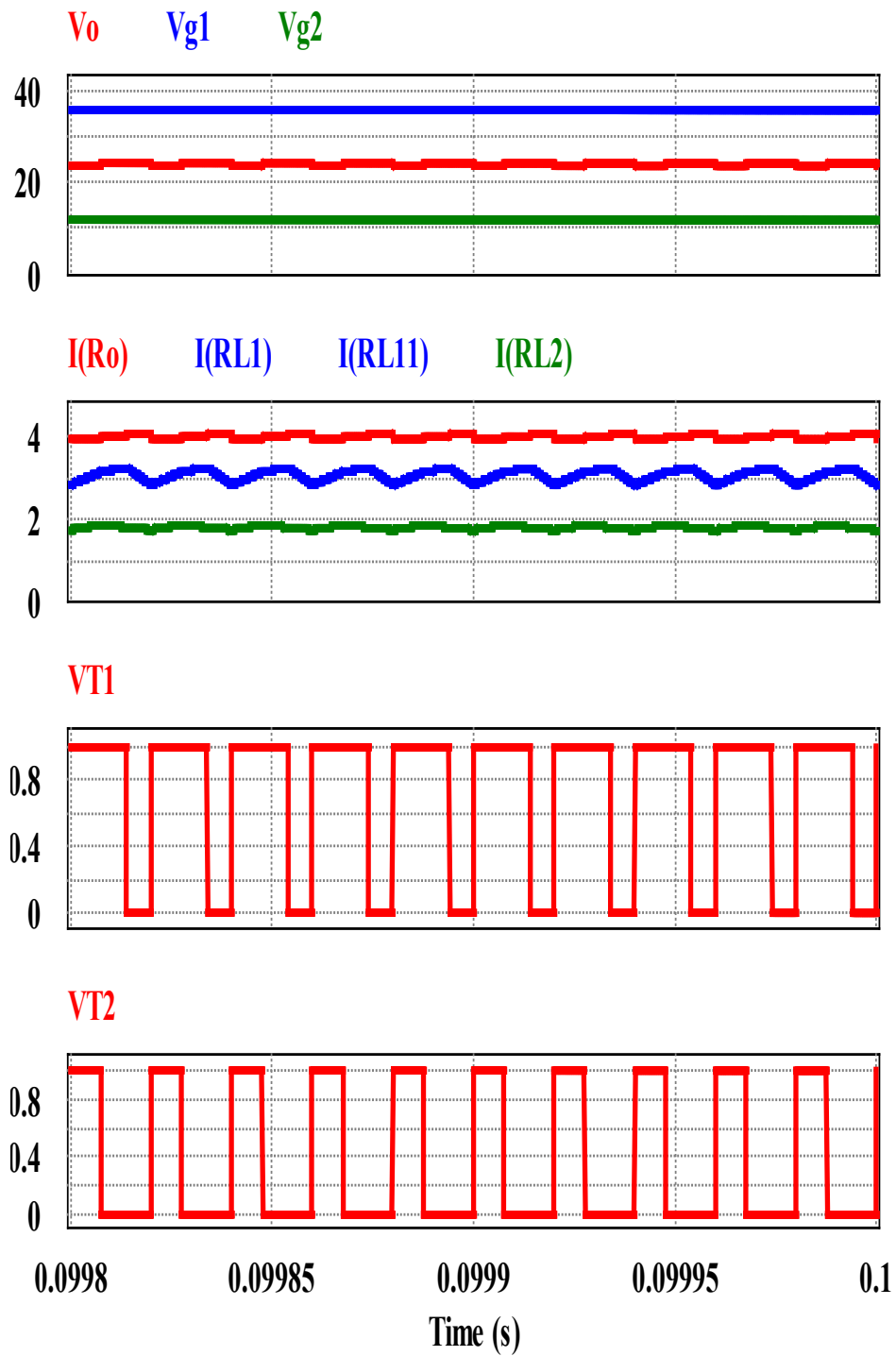
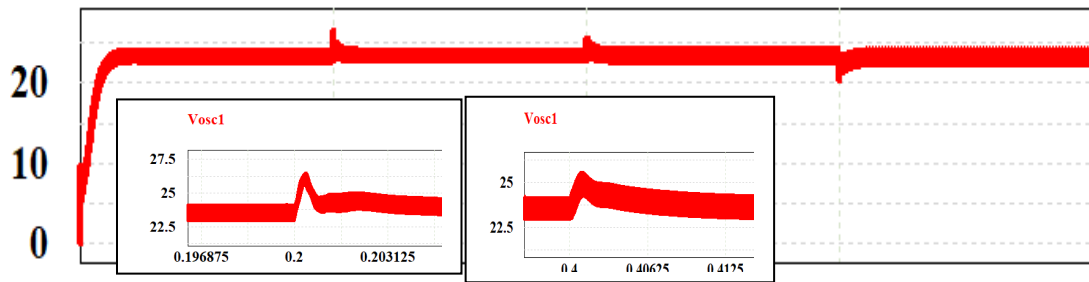
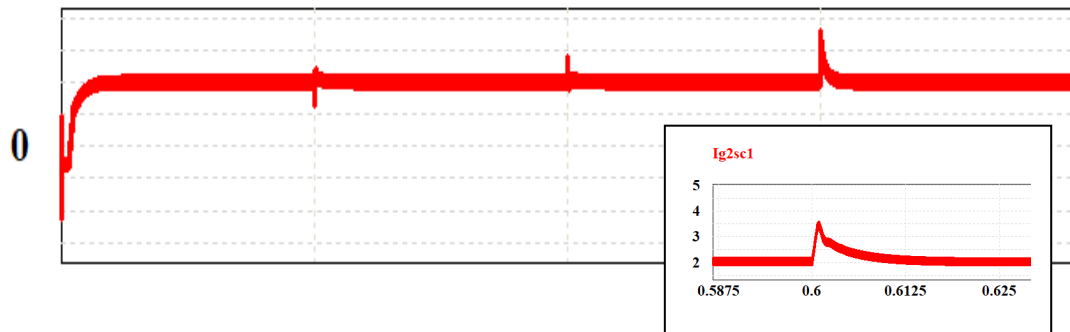


Fig. 4. 105 Steady-state waveforms of SCHBSTIC1

V_{osc1}



I_{g2sc1}



I(R_{osc1})

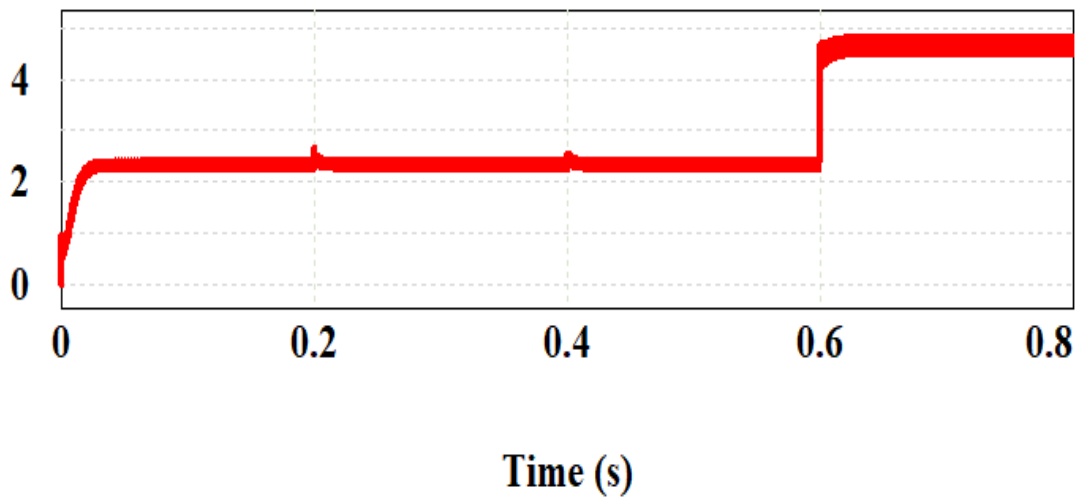


Fig. 4. 106 Dynamic response of the SCHBSTIC-1, for the variation of source-1 voltage V_{g1}: 32V to 36V, source-2 voltage V_{g2}: 12V to 10V, and load resistance 10Ω to 5Ω, the Output Voltage (V_o), Source Current (I_{g2}), Output current I_o are plotted.

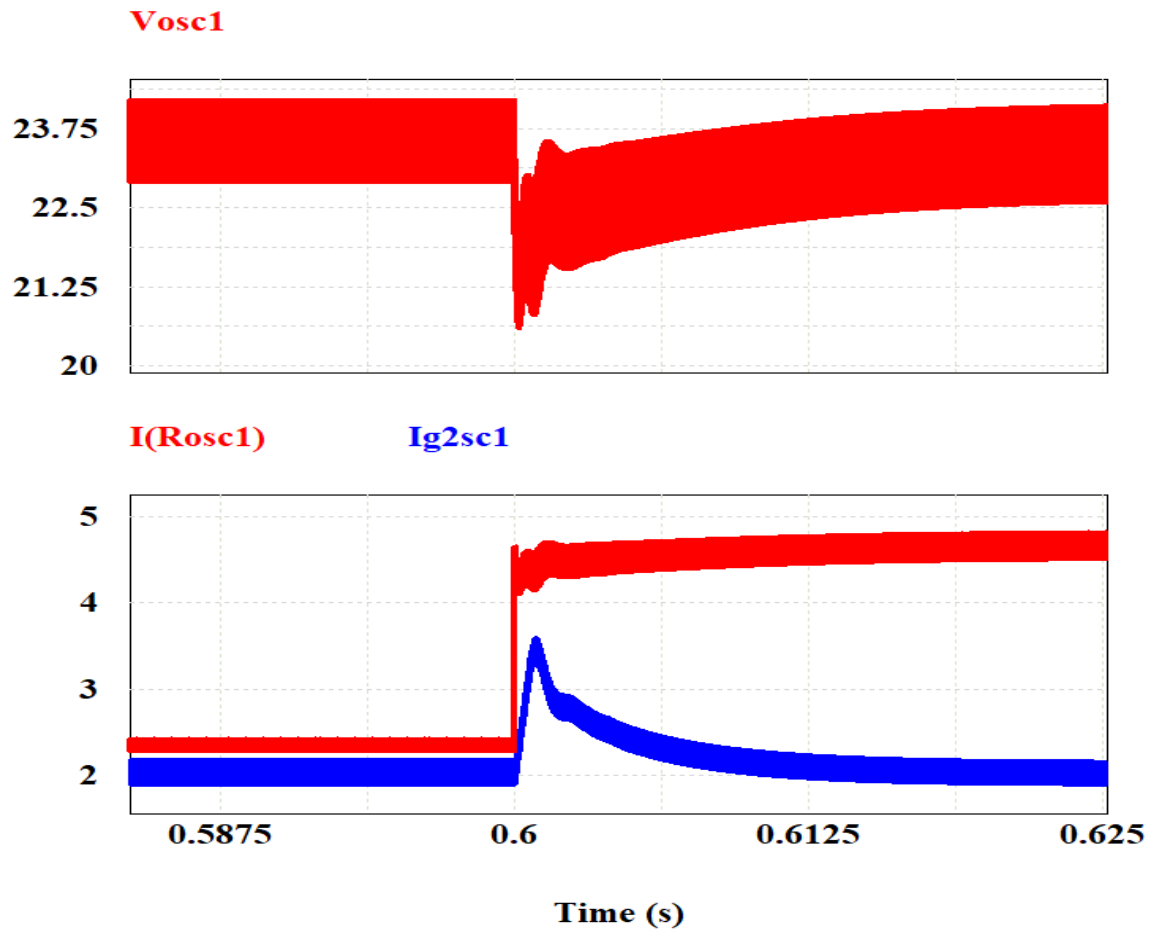


Fig. 4. 107 Dynamic response of the SCHBSTIC2 of the variation of V_o , I_o , I_{g2} currents for Load Variation form 10Ω to 5Ω

4.7 Controller Design of SCCHBSTIC-2

In the similar lines, the Decoupled-Decentralized MIMO QFT controller design discussed in section 4.6.1 is applied to SCHBSTIC1 to obtain the controllers shown below in table 4.10, and the controller loop shaping graphs are shown in Figs. 4.108 and 4.112, followed by the verification plots shown in Figs. 4.109 to 4.111 for voltage control and 4.113 to 4.115. The steady state responses are shown in Fig. 4.116, and the dynamic response of the SCHBSTIC2 topology for the variation in sources and load are shown in Fig. 4.117, the controllers were able to regulate the output voltage and source-2 currents at the required limits.

Table 4. 10 Controllers and decouplers of SCHBSTIC-2

Voltage Loop Controller	Current Loop Controller
$G_{c11} = \frac{0.27 (z-0.89)(z-0.583)}{(z-1) (z-0.72)}$	$G_{c22} = \frac{0.1(z-0.61)(z-0.77)}{(z-1)(z-0.33)}$
$d_{12} = \frac{0.453 (z-0.6578)}{(z-0.1143)}$	$d_{21} = \frac{0.712 (z-0.933)}{(z-825)}$

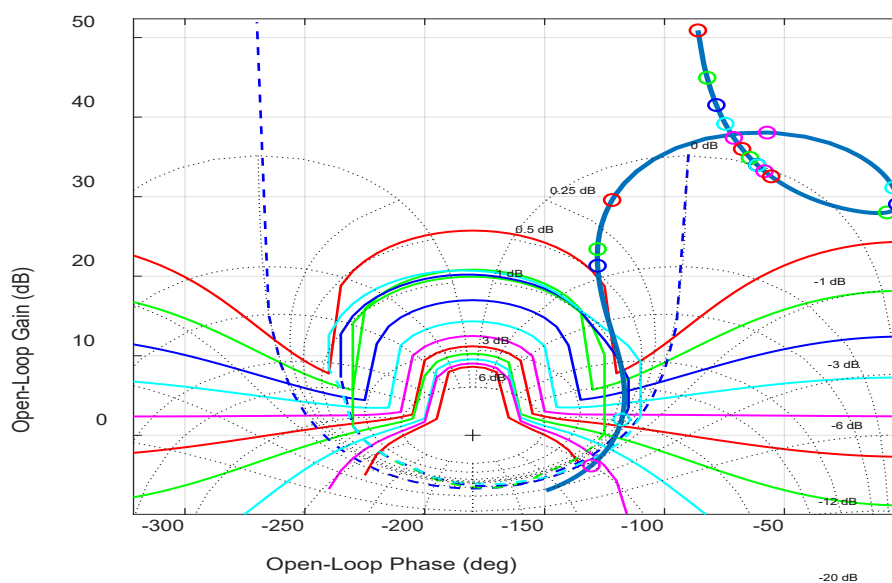


Fig. 4.108 Loop-shaping plot of Current loop

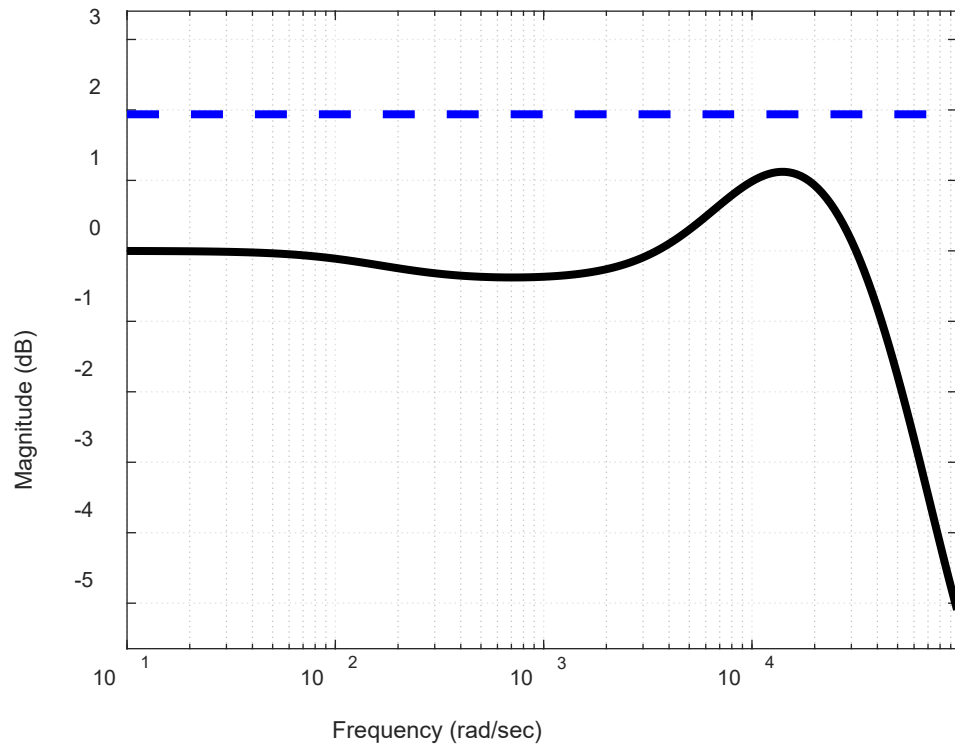


Fig. 4. 109 Frequency response of the Robust control verification bounds of the Voltage loop

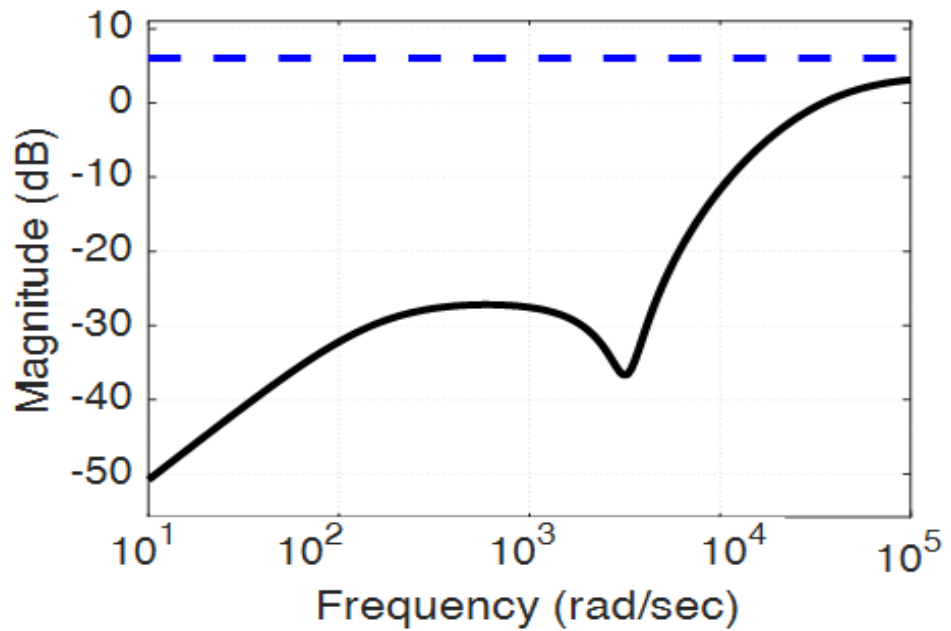


Fig. 4. 110 Frequency response of the sensitivity verification bounds of the Voltage loop

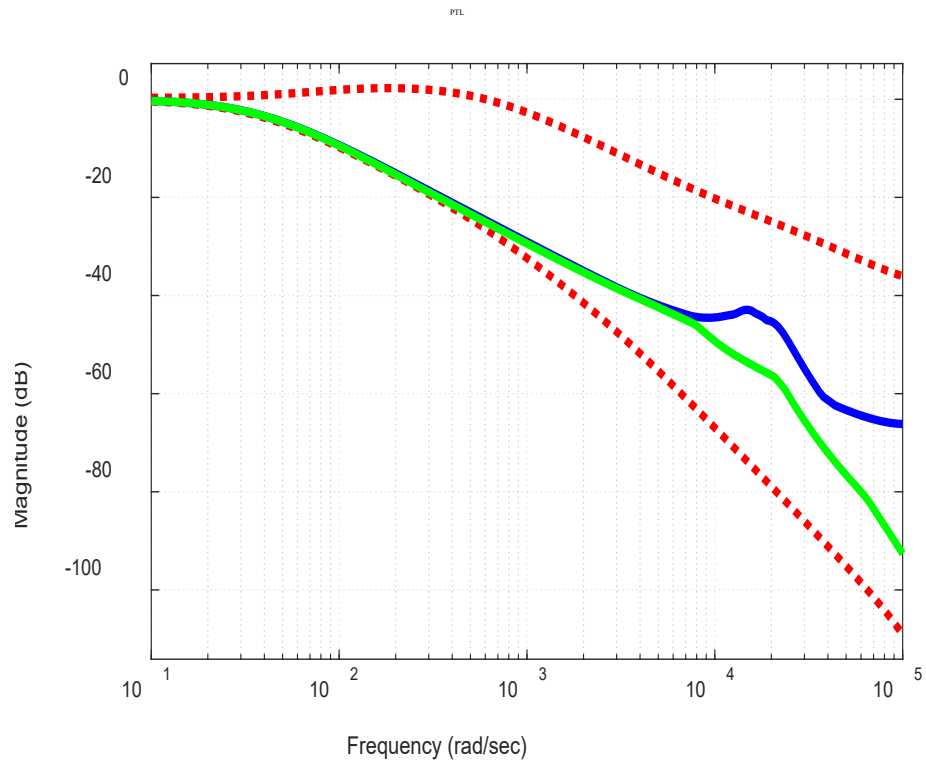


Fig. 4. 111 Closed-loop frequency response verification of uncertainty set voltage control loop

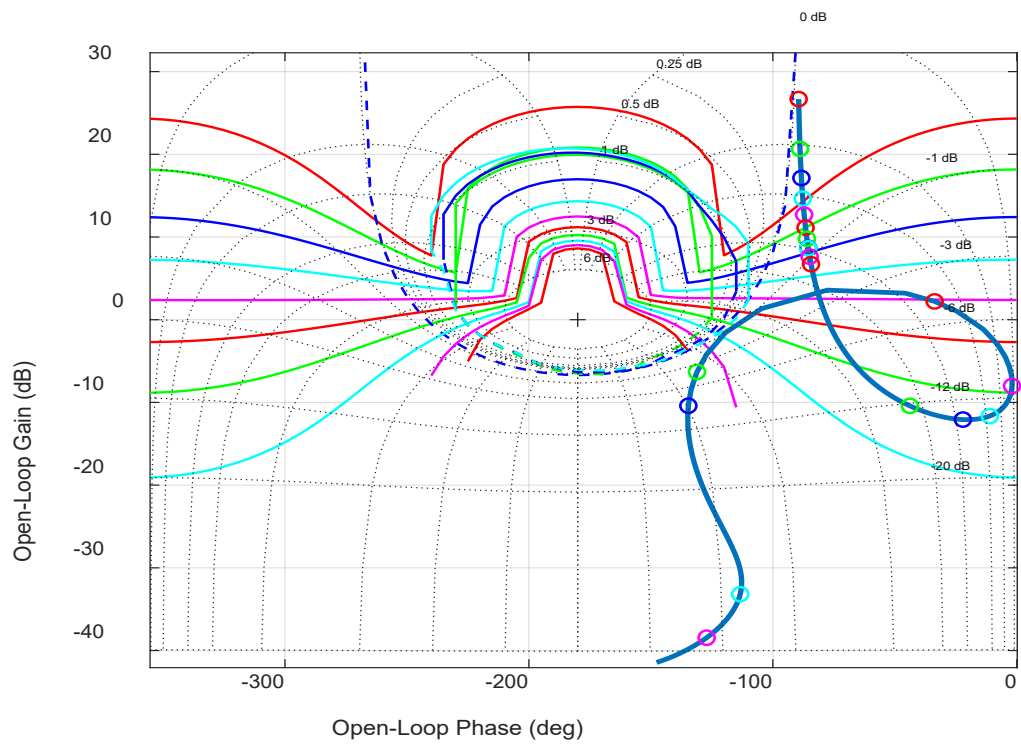


Fig. 4. 112 Loop-shaping plot of Current loop

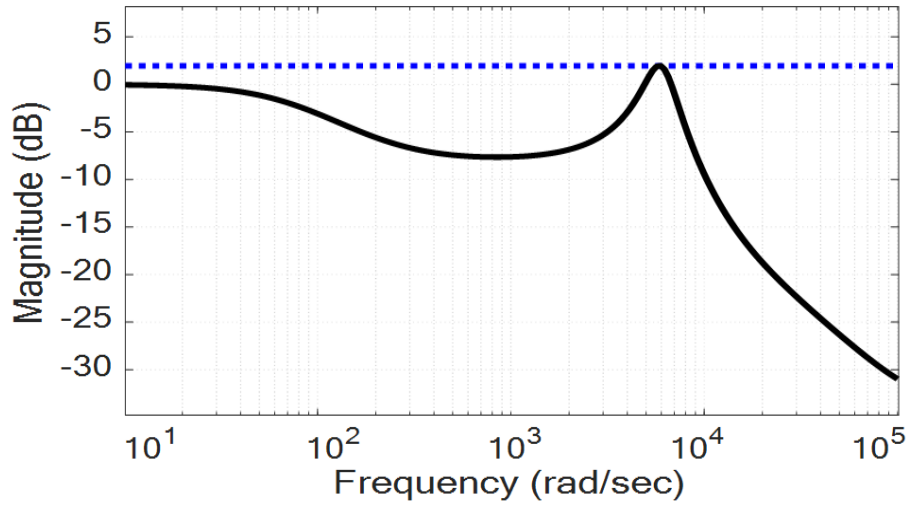


Fig. 4. 113 Frequency response of the Robust control verification bounds of the current loop

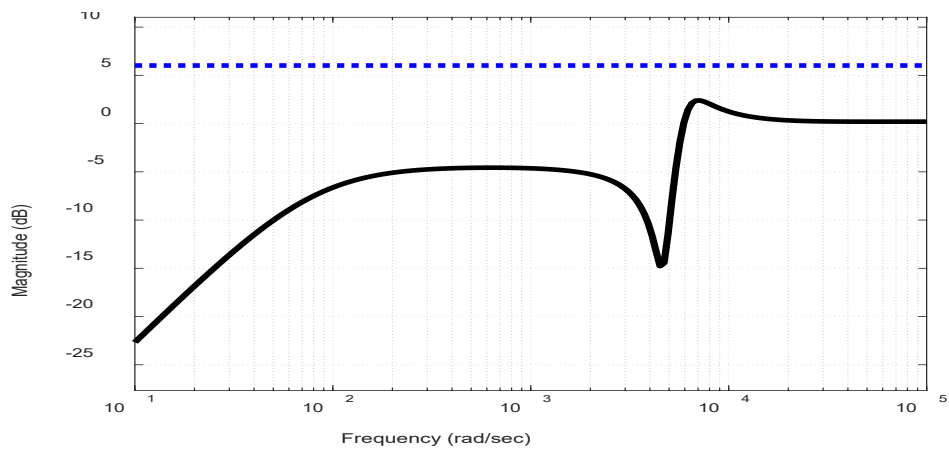


Fig. 4. 114 Frequency response of the sensitivity verification bounds of the current loop.

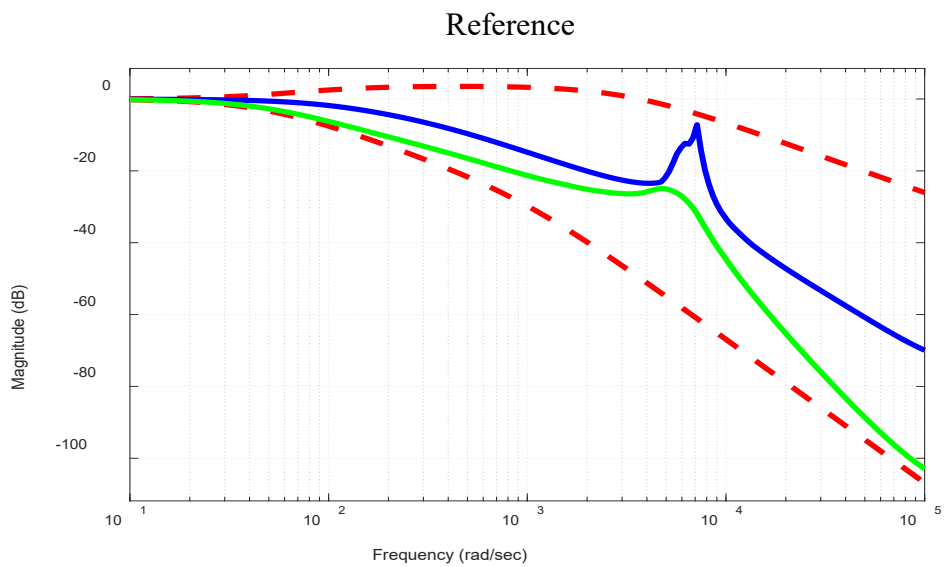


Fig. 4. 115 Closed-loop frequency response verification of uncertainty set current control loop

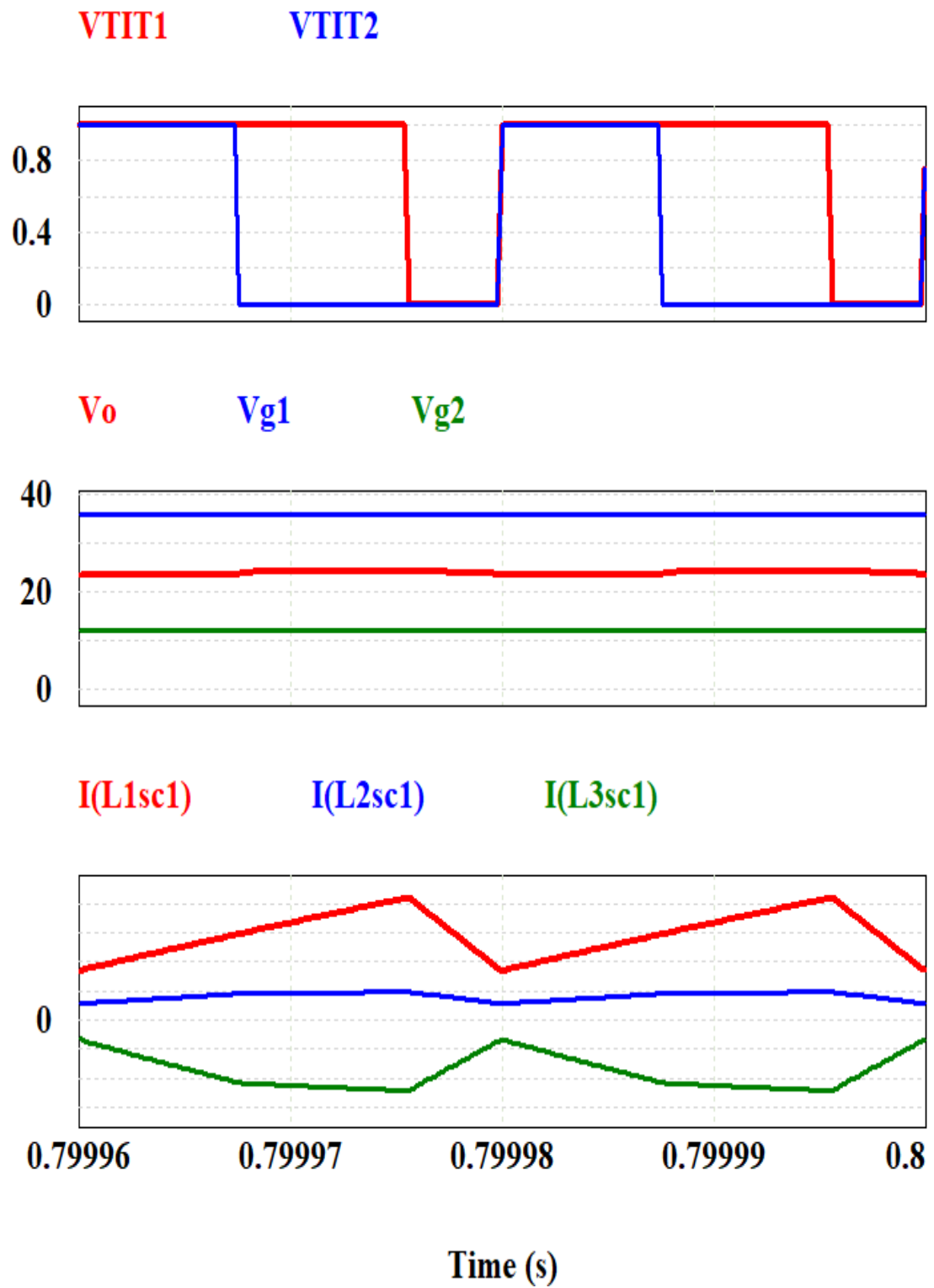


Fig. 4. 116 Steady-state waveforms of SCHBSTIC2

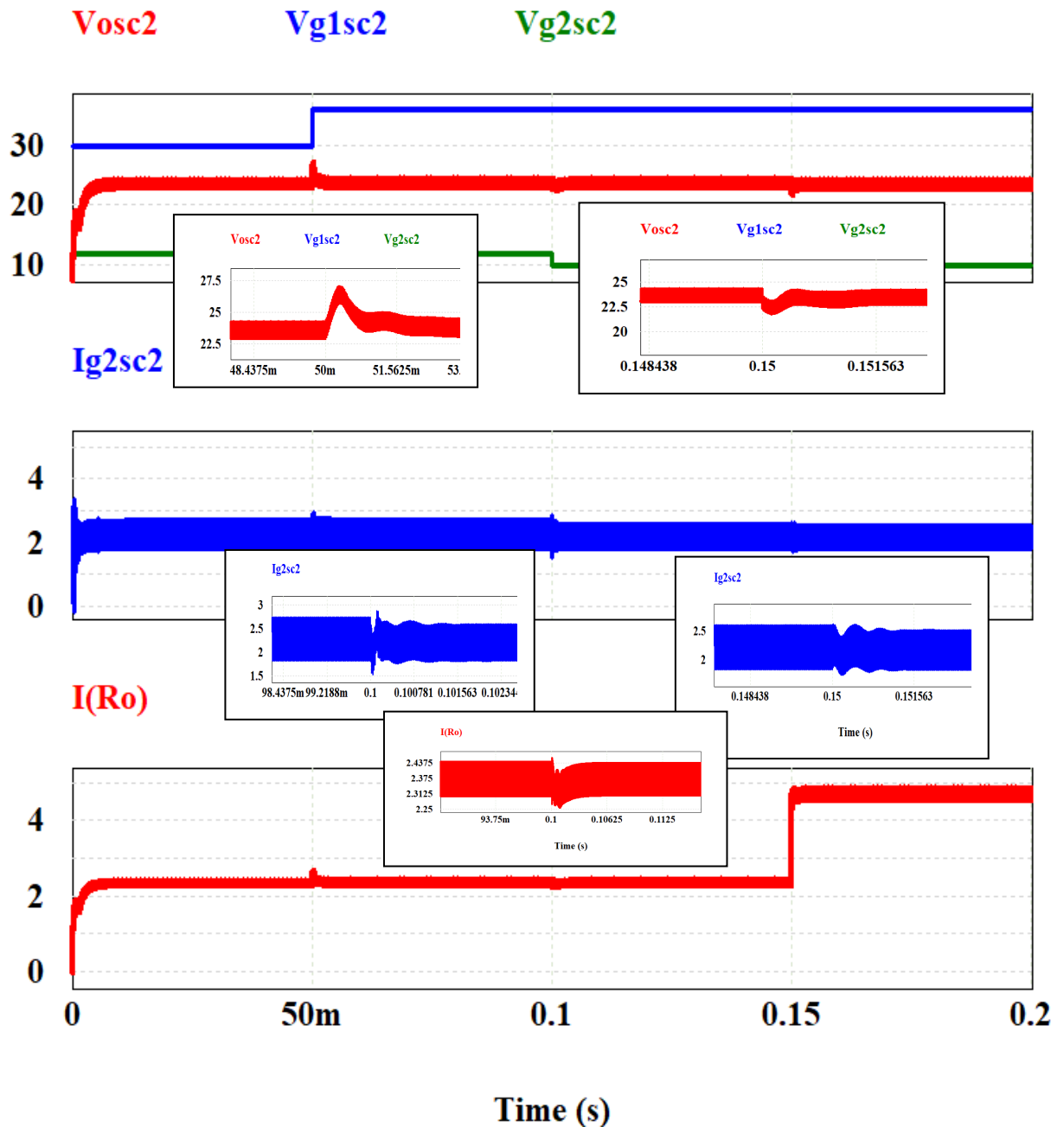


Fig. 4. 117 Dynamic response of the SCHBSTIC2 topology for the variation of source-1 voltage V_{g1} : 30V to 36V, source-2 voltage V_{g2} : 12V to 10V, and load resistance 10Ω to 5Ω , the Output Voltage (V_o), Source Current (I_{g2}), Output current I_o are plotted.

The dynamic response of SCHBSTIC-2 is plotted for variation of source-1 voltage V_{g1} : 30V to 36V, source-2 voltage V_{g2} : 12V to 10V, and load resistance 10Ω to 5Ω , the Output Voltage (V_o), Source Current (I_{g2}), Output current I_o are plotted. It is observed that the output voltage is driven to 24V in about 6mSec and similarly the current is regulated to the rated 2A, which proves the effectiveness of the designed DDMQFT controllers.

4.8 Hardware Results and discussion

To validate the performance of the proposed topologies with the controllers, the experimental set up in the laboratory was carried out on 100 W 50 kHz prototype which is shown in Fig. 4.119, to realize the digital controllers dsPIC33FJ16GS504 digital signal controller was used. The opto-isolator 6N137, driver circuit IR2110, diode MUR1520, and switch IRFP250N are the components utilized in the prototype converter circuits. The microcontroller's on-board ADC receives the measured load voltage after it has been reduced to a range of 0 to 5V. The relevant hardware implementation methodology is shown in Fig. 4.118.

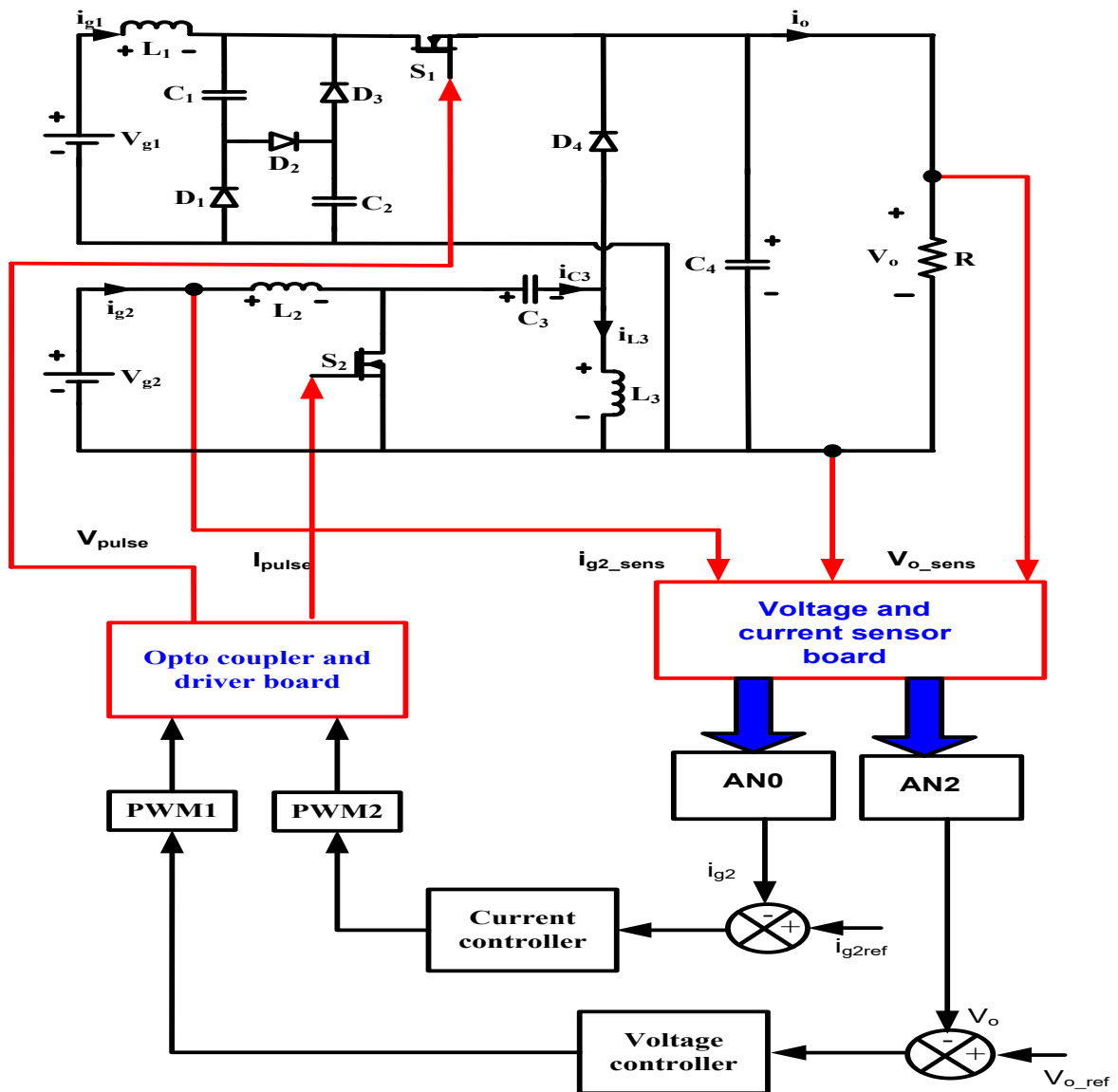


Fig. 4. 118 Block Diagram of Hardware Implementation method of SCHBSTIC-2 topology

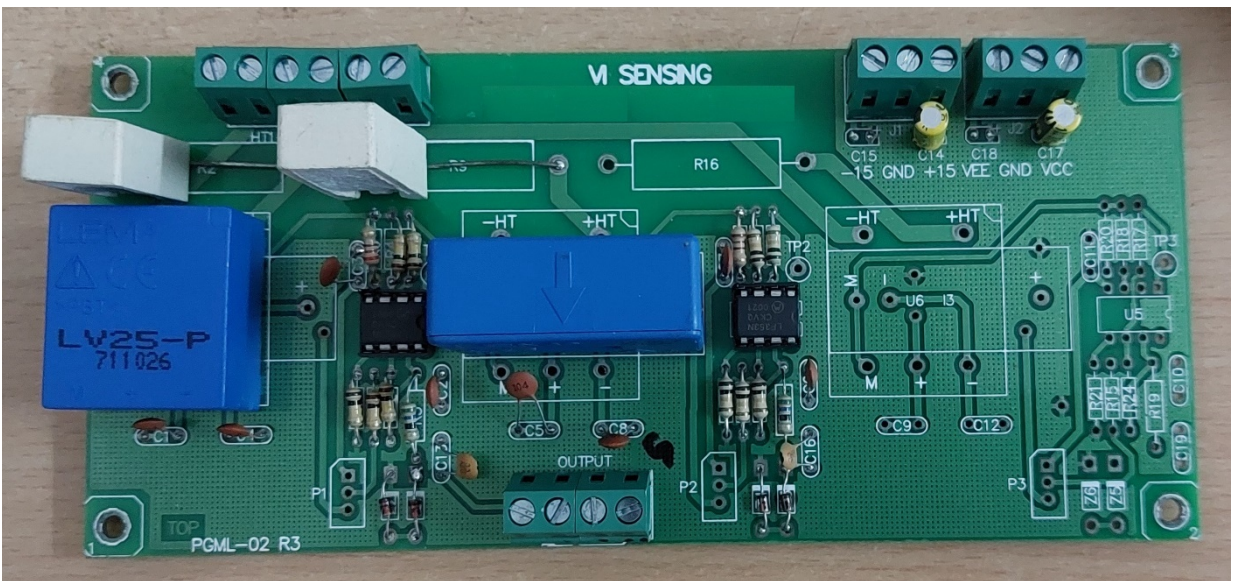
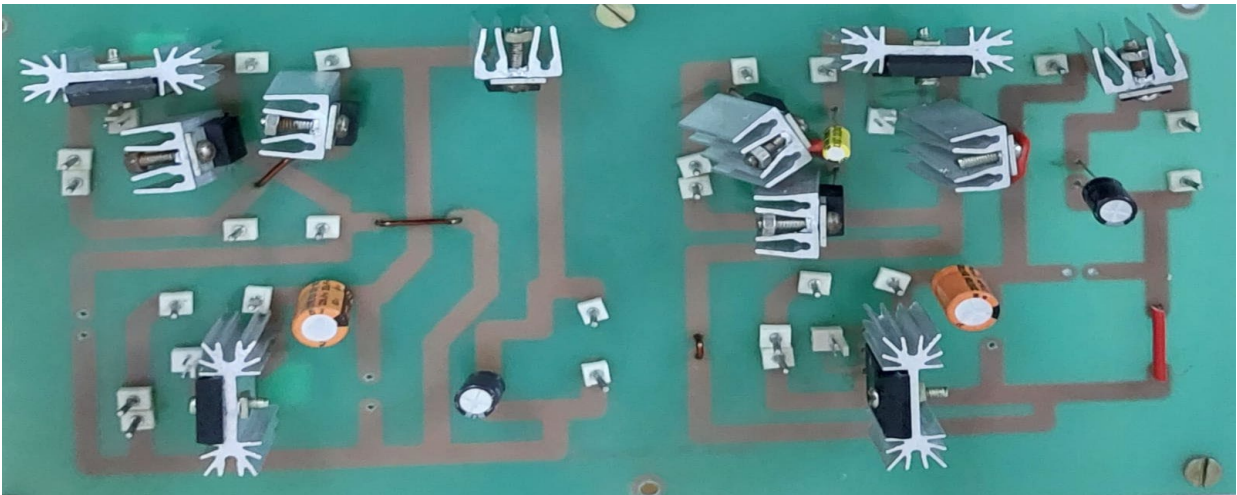
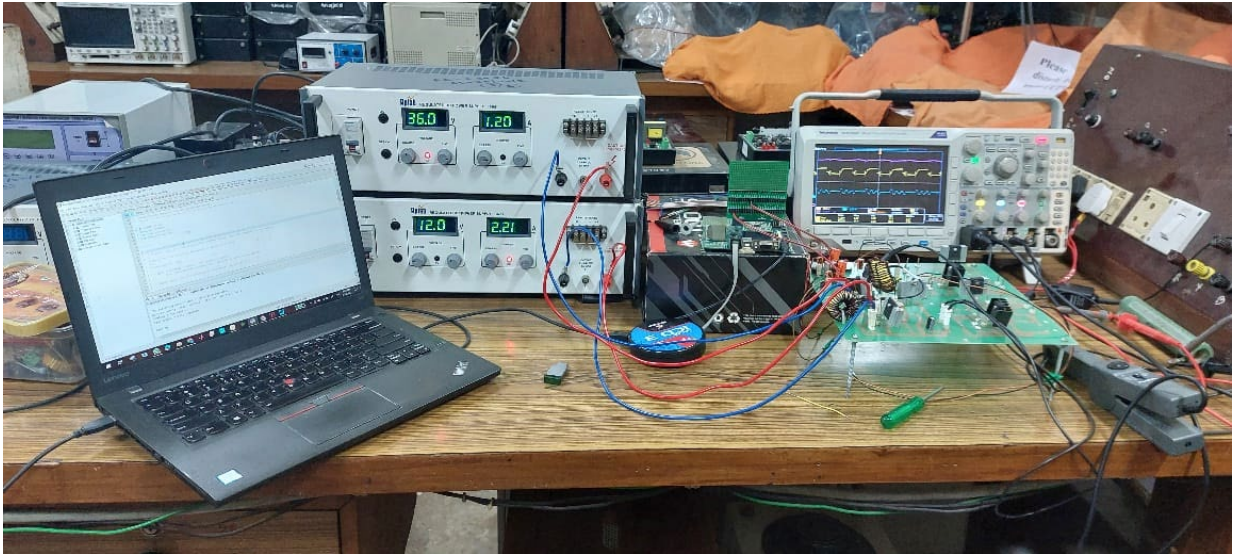


Fig. 4. 119 (a) The Hardware setup for experimentation (b) PCB of TIC topologies (c) Sensing Circuit

The steady-state waveforms for the nominal operating conditions (V_{g1} : 36 V, V_{g2} :12 V, i_{g2} :2.0 A, R : 5 Ω and f_s :50 kHz) are shown in Figs. 4.120, 4.121. Here, the duty-ratio control signals G_{s1} and G_{s2} are shown. As it can be seen, the duty-ratio signal of G_{s1} (d_1) is greater than the duty-ratio signal of G_{s2} (d_2). Here, the load voltage and the source- i_{g2} current are regulated due to closed-loop operation. Another steady-state measurement is captured for $R=10 \Omega$ while keeping the remaining conditions the same as above. Here, the difference in the width of the duty-ratio of the two signals (d_1 and d_2) can be seen. In Fig. 4.120, d_2 has been increased whereas a small decrease in d_1 is visible. This justifies the successful operation of the designed controller which is capable of readjusting the respective duty ratios according to the change in power demand. Furthermore, the regulation of source-2 current and load voltage has been successfully achieved in both conditions. The other quantities such as the load Voltage as well as source-2 current, are also measured and shown in Figs. 4.122 and 4.123 for the cases of load value 5 Ω and 10 Ω , respectively. Similarly the output voltage and source-2 current are obtained for SIHBSTIC and QBSTIC in Figs. 128 and 129.

The measured dynamic response of the SCHBSTIC- topology-2 is also shown in Fig. 4. 124, 4.125 for load change from 10 to 5 Ω for the conditions of V_{g1} :36 V, V_{g2} :12 V, V_0 :24 V. The effectiveness of the designed controller in terms of loads voltage regulation as well as source-2 current regulation is apparent. It takes around 10.0 ms for the converter to achieve its steady-state value. The steady-state of the source-2 current has also been achieved. Dynamic performance in terms of source-2 variation (12 to 16 V) as well as source-1 variation (change from 30 to 36 V) can also be seen in Fig. 4. 125 and 4.126, respectively. In the case of source-1 variation with the conditions of V_{g2} =12 V, V_0 =24 V, R =10 Ω , regulation of load voltage and source-2 current is seen. It takes less than 10.0 ms for the converter to achieve its steady state. The constant flow of load current is also visible. On similar lines, regulation of load voltage, as well as source-2 current, was also seen in case of source-2 voltage change under the condition of

$V_{g1}=36\text{ V}$, $V_0=24\text{ V}$, $R=10\ \Omega$. Regulation is achieved in nearly 50.0 ms. Source-2 current waveform along with the source-2 voltage waveforms are also shown.

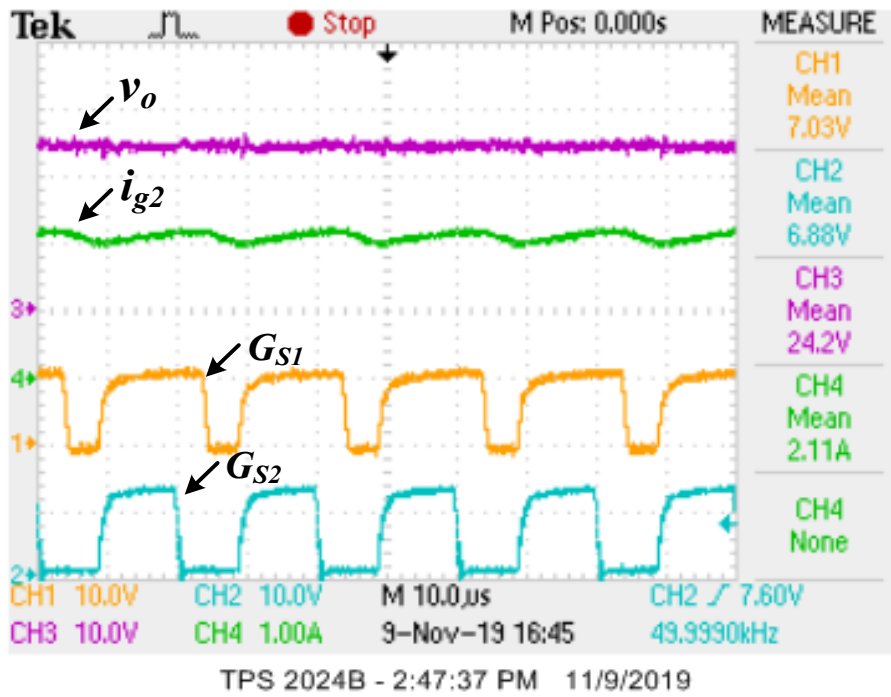


Fig. 4. 120 Steady-state waveforms of SCHBSTIC ($V_{g1}=36\text{ V}$, $V_{g2}=12\text{ V}$, $V_0=24\text{ V}$, $R=5\ \Omega$).

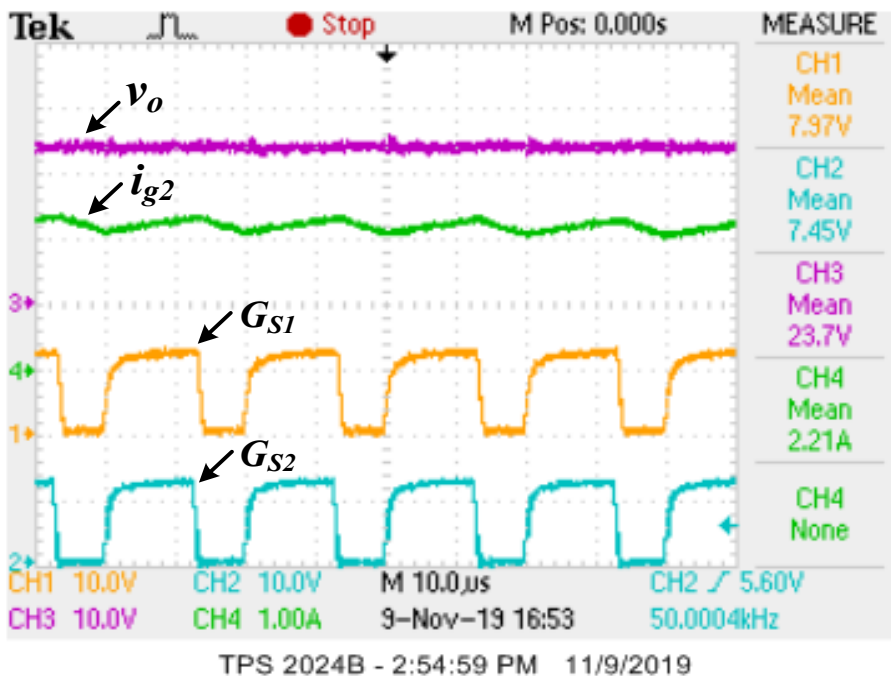


Fig. 4. 121 Steady-state waveforms of SCHBSTIC ($V_{g1}=36\text{ V}$, $V_{g2}=12\text{ V}$, $V_0=24\text{ V}$, $R=10\ \Omega$).

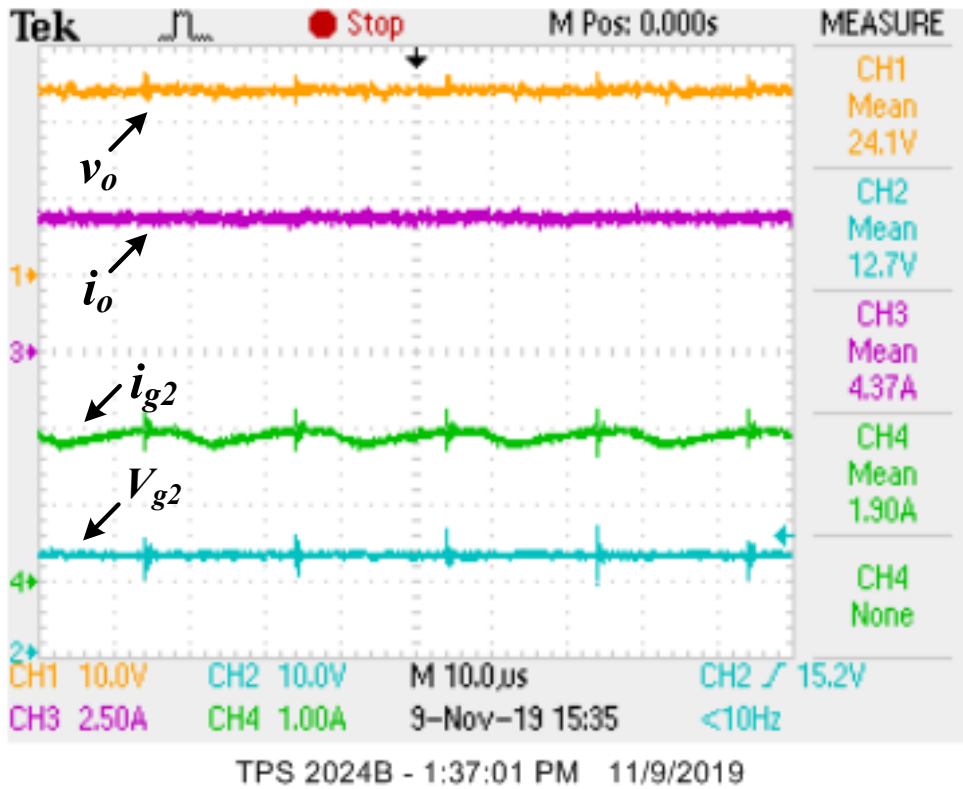


Fig. 4. 122 Steady-state waveforms of SCHBSTIC ($V_{g1}=36$ V, $V_{g2}=12$ V, $V_0=24$ V, $R=5$ Ω).

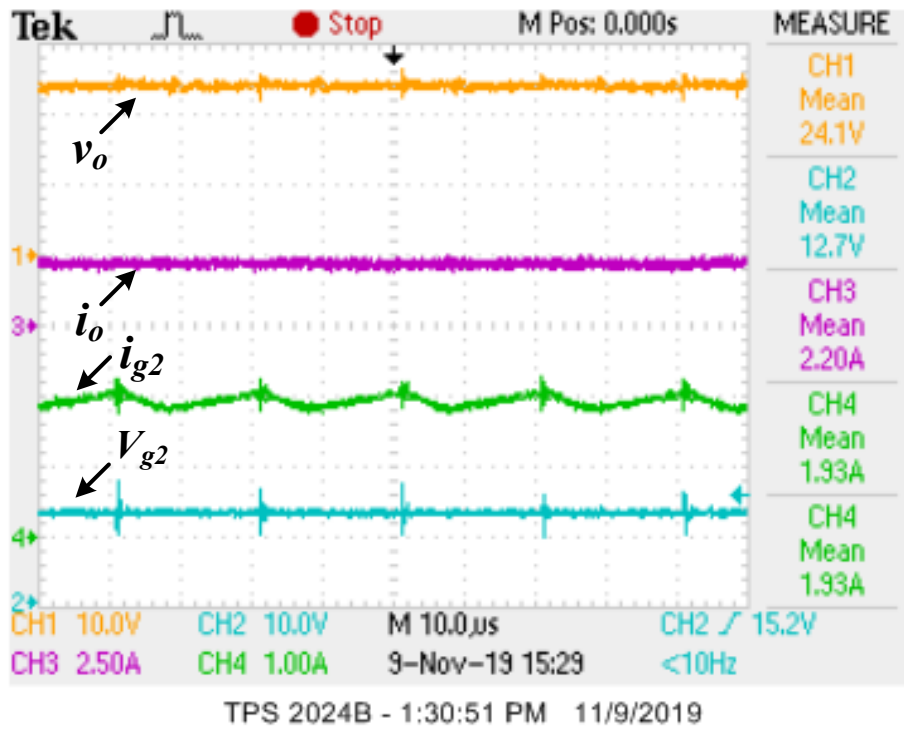


Fig. 4. 123 Steady-state waveforms of SCHBSTIC2 ($V_{g1}=36$ V, $V_{g2}=12$ V, $V_0=24$ V, $R=10$ Ω).

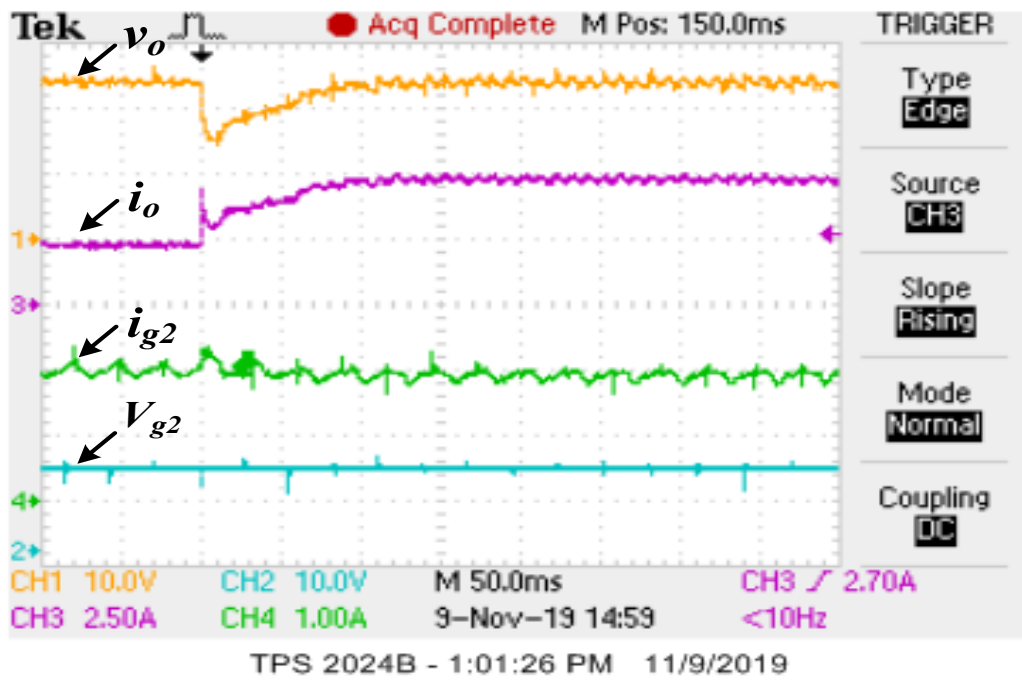


Fig. 4. 124 Dynamic response of the SCHBSTIC2 ($V_{g1}=36$ V, $V_{g2}=12$ V, $V_0=24$ V, $R=10-5$ Ω) using simulation and hardware.

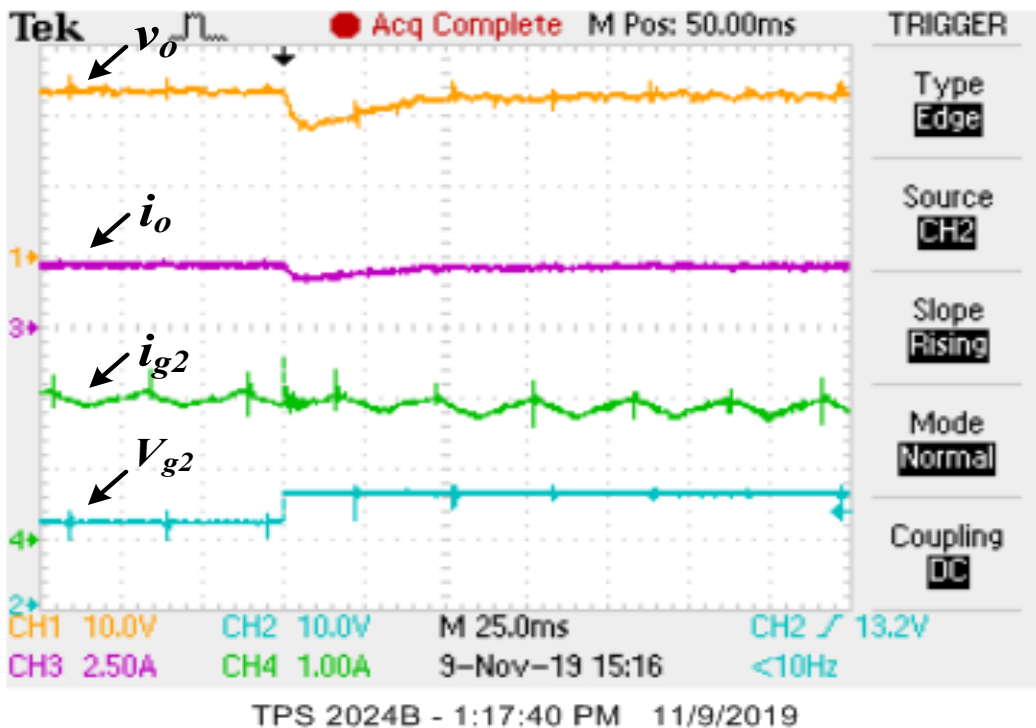


Fig. 4. 125 Dynamic response of the SCHBSTIC2 ($V_{g1}=36$ V, $V_{g2}=12-14$ V, $V_0=24$ V, $R=10$ Ω).

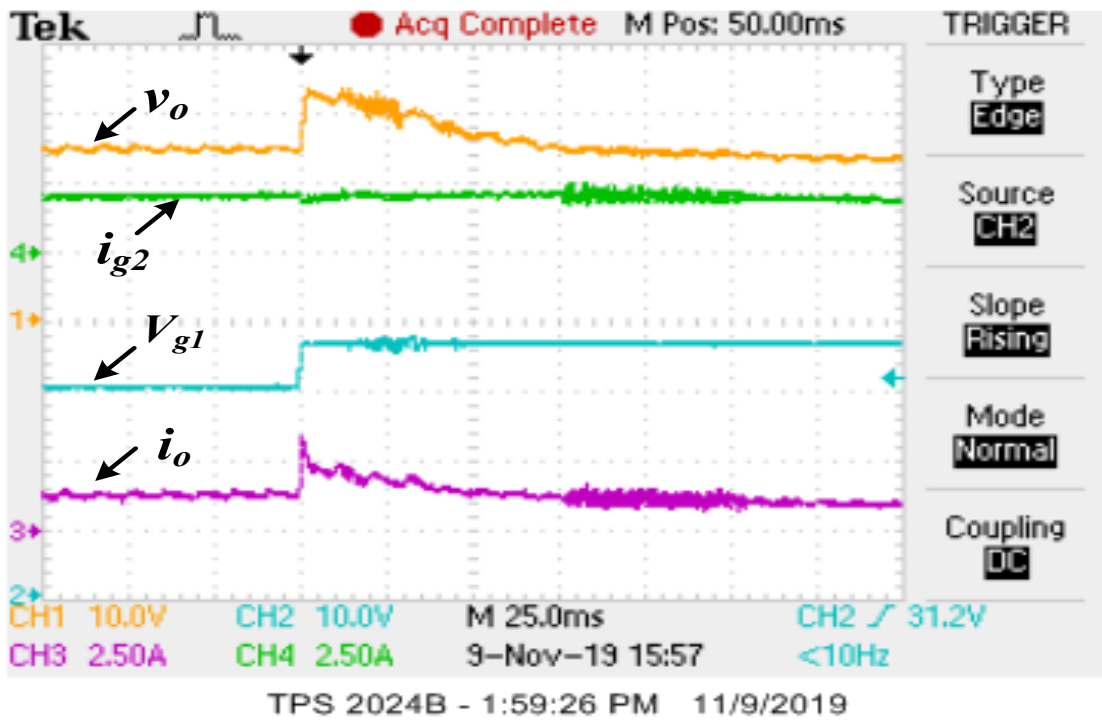


Fig. 4. 126 Results of Dynamic response of the SCHBSTIC2 obtained from simulation and hardware for specifications : $V_{g1}=30-36$ V, $V_{g2}=12$ V, $V_0=24$ V, $R=10$ Ω .

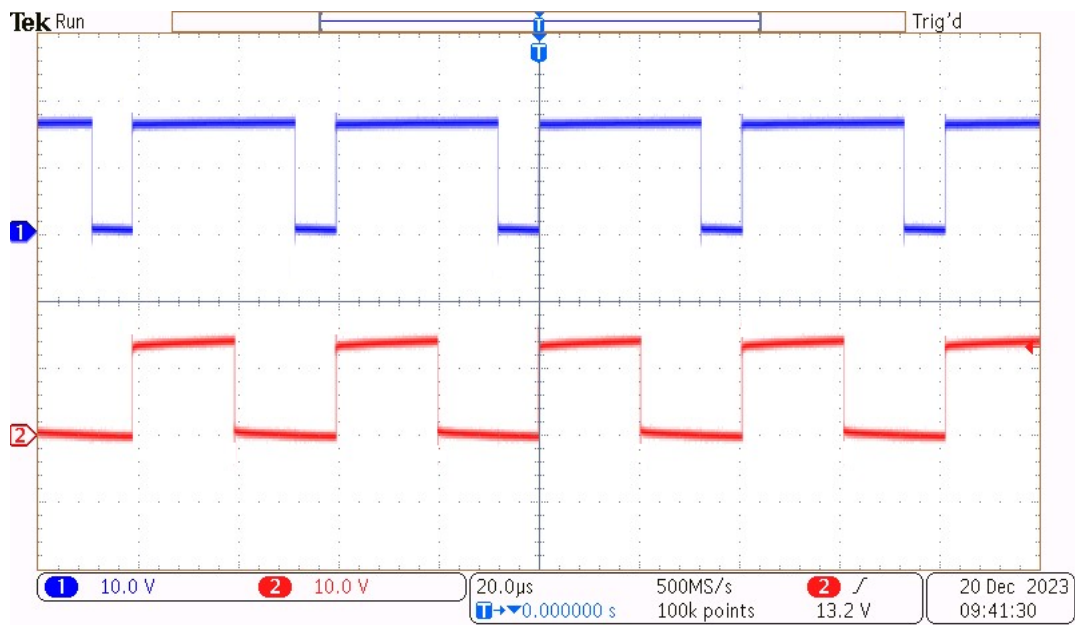


Fig. 4. 127 Gating signals to switches 1 and 2.

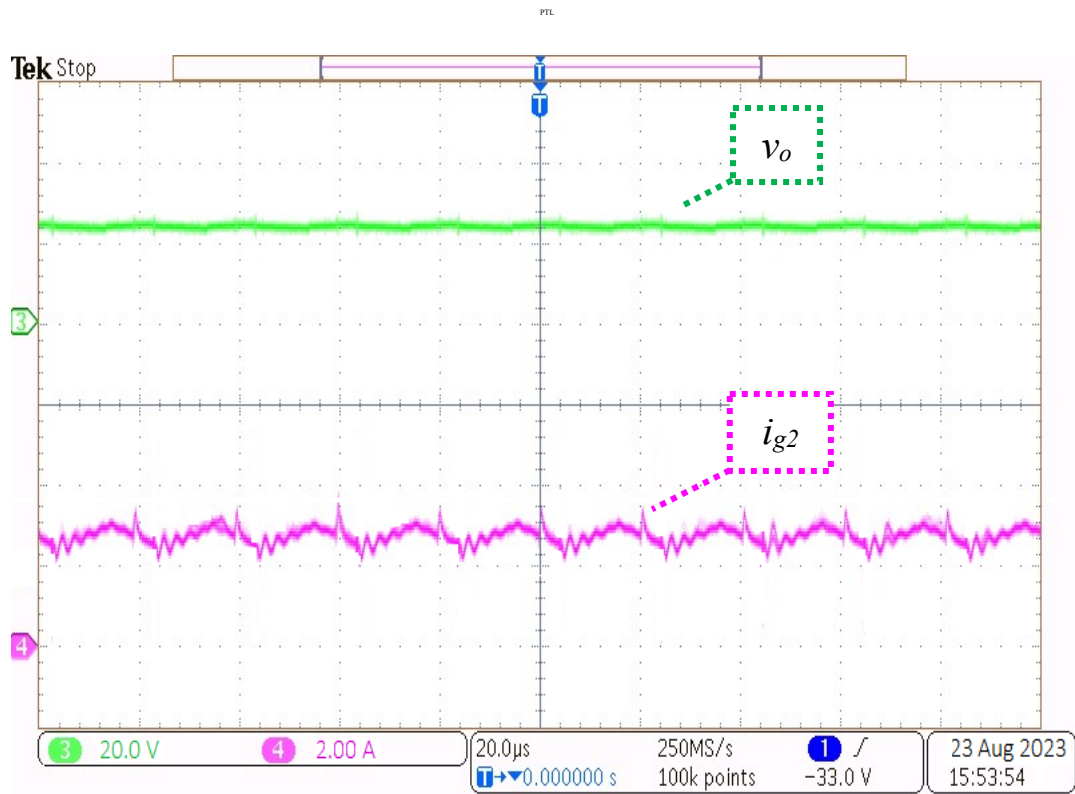


Fig. 4. 128 Steady-state waveforms of SIHBSTIC ($V_{g1}=36$ V, $V_{g2}=12$ V, $V_0=24$ V, $R=10$ Ω)

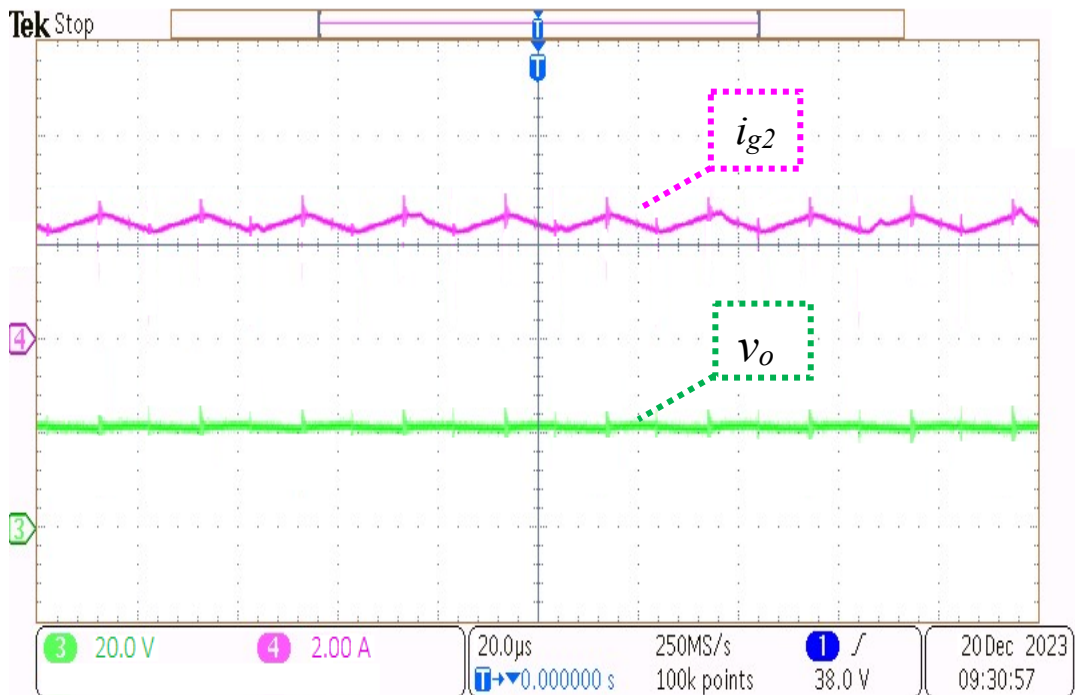


Fig. 4. 129 Steady-state waveforms of QBSTIC ($V_{g1}=36$ V, $V_{g2}=12$ V, $V_0=24$ V, $R=10$ Ω).

4.9 Summary

Chapter 4 discusses controller design techniques for TIC topologies, including ICD, SMQFT, and DDMQFT, to regulate output voltage and source-2 current in case of disturbances. The ICD technique effectively achieves desired results, while decentralized controllers mitigate interactions among loops. The SMQFT technique, applied to QBSTIC, provides feasible voltage and current regulation, but suffers from low gain and high dynamic response ringing. The hardware prototype was set up for SIHBSTIC, QBSTIC, and SCHBSTIC-2 topologies. The steady-state responses were obtained for all three topologies. Dynamic responses were obtained for SCHBSTIC-2 topology. The SCHBSTIC- topology-2 controller is shown in steady-state waveforms for nominal operating conditions, demonstrating its ability to adjust duty ratios based on power demand changes. The controller successfully regulates source-2 current and load voltage in both conditions, with a 10ms time to achieve steady-state values, and also source current regulation. The controller's effectiveness in regulating loads voltage and source-2 current is evident, with the converter achieving steady-state values in less than 10ms for source-1 variation and 50ms for source-2 voltage change.

CHAPTER - 5

CONCLUSIONS AND FUTURE SCOPE OF WORK

5.1. Conclusions

After reviewing the multi-input topologies extensively, it was identified that there is a need to evolve two-input converters capable of exhibiting extreme step-down voltage gains. With this aim, the integration of the buck and SEPIC topologies was done and then amalgamated with the switched-inductor/switched-capacitor cells to yield the two-input hybrid topologies. In these topologies, the switched-inductor/switched-capacitor cells were responsible for ensuring the extreme step-down voltage gain feature. The hybrid converters investigated in this thesis were: (i) Switched Inductor Hybrid Buck SEPIC two-input Converter (SIHBSTIC), (ii) Sixth-order Quadratic Buck-SEPIC two-input DC-DC Converter (QBSTIC), and (iii) Switched Capacitor-cell with Hybrid Buck-SEPIC two-input converter (SCHBSTIC) topology-1 and topology-2. The analysis of these topologies revealed the following: (i) the voltage gain exhibited by all these topologies was a function of both the controlling inputs (duty ratio control signals of the controllable switches d_1 and d_2), (ii) with the aim to realize the desired load voltage by setting the duty ratios d_1 and d_2 , the load shared by the two sources gets hampered. This issue called for the need to bring in the controller on the input source side, (iii) the flexibility of choosing different d_1 and d_2 values offered the benefit of drawing of power of different magnitudes from the input sources. This feature is attractive in the sense that it helped in drawing power from multiple sources according to their power supplying capacities, and (iv) though flexibility is achieved in terms of realizing desired voltage gains, some of these topologies (SIHBSTIC, QBSTIC) exhibited more ripples in their source current. However, the SCHBSTIC topology-1 and topology-2 were successful in minimizing the ripples in the source current.

Dynamic performance features of the proposed topologies were explored after the exhaustive steady-state analysis was done. This was initiated after establishing the transfer functions of all

the topologies. Since the topologies belonged to MIMO systems, multi-variable control theory was applied to understand the interactions (based on RGA theory) existing in the converter systems to obtain the suitable control-loop pairings.

Upon ensuring suitable control-loop pairings that were obtained on a mathematical basis, a non-diagonal control strategy was formulated for all the topologies enlisted above. To design a robust controller, a multi-input multi-output QFT based approach was adopted. Based on these strategies, the steady-state, as well as the dynamic performance of the proposed topologies, was assessed. The analytical studies were verified and supported by the simulation results. In all the topologies formulated, the effectiveness of the non-diagonal controller was also seen both in steady-state as well as during dynamic conditions. It indicated the MIMO-controller's satisfactory performance on account of the plant interactions as well as the uncertainties which lead to active avoidance of the instability issues along with proper power management.

5.2. Future Scope of Work

In this thesis, the emphasis was laid on topological evolutions based on an amalgamation of buck and SEPIC converters along with switched-inductor/switched-capacitor cells. Although four different topological formulations were established, still there lies a scope of evolving topologies similar to them either from voltage gain point of view or exhibiting identical ripples. In addition, the scope for making use of the flexibility within the switched-inductor/switched-capacitor cells and exploring new topological structures is also present. Rearrangement of the alternate along with the new ones. The above suggestions were concerning the topological structure point of view; however, much work can still be carried out about the control viewpoint. Here, emphasis can be laid not only on the full-order controller structures, but possibilities also lie on evolving suitable lower or upper triangular control structures.

ANNEXURE

Various equations of chapters-2,3 were unburdened and are represented here.

A.1. Switched Inductor Hybrid Buck SEPIC TIC

The KVL equations for inductors in each mode as listed below.

Mode -1:

$$V_{g1} - 2v_{L1} + v_{C1} = 0; \quad (\text{A.1})$$

$$v_{L2} - V_{g2} = 0 \quad (\text{A.2})$$

Mode - 2:

$$V_{g1} - 2v_{L1} - V_o = 0; \quad (\text{A.3})$$

$$V_{g2} - v_{L2} - v_{C1} - V_o = 0 \quad (\text{A.4})$$

Mode -3:

$$v_{L1} = -V_o; \quad (\text{A.5})$$

$$V_{g2} - v_{L2} - v_{C1} - V_o = 0 \quad (\text{A.6})$$

On solving the above equations, the resultant capacitor voltage equation is

$$v_{C1} = \frac{V_{g2}}{1-d_2} - V_o \quad (\text{A.7})$$

Substituting the v_{C1} expression obtained from eq. (A.4), and in the eq. (A.2b) results in

$$V_{g1}d_1 - V_o(2-d_1-d_2) + \left(V_{g2} \frac{d_2}{1-d_2} - V_o d_2 \right) = 0 \quad (\text{A.8})$$

Solving and substituting eq. (A.4) in eq. (A.3b), and simplifications results in the following.

$$V_o(2-d_1) = V_{g1}d_1 - V_{g2} \frac{d_2}{(1-d_2)} \quad (\text{A.9})$$

Assuming the parasitic resistances of the inductors to be negligible, the voltage conversion ratio of this converter is obtained and is given below.

$$V_o = V_{g1} \left(\frac{d_1}{2-d_1} \right) + V_{g2} \left(\frac{d_2}{(2-d_1)(1-d_2)} \right) \quad (\text{A.10})$$

A.1.1 Design of SIHBSTIC parameters

The ripple-based design approach is used to design the elements of SIHBSTIC. The peak-to-peak current ripple is assumed to be less than 20%, while the voltage ripple is assumed to be less than 10%. The design parameters for validation are listed in Table 2.10.

The load power for dual input integrated converter is:

$P_o = V_o I_o$ where V_o , I_o is the load voltage and current, respectively.

The load current can be calculated as. $I_o = \frac{V_o}{R}$ (A.11)

For a lossless system: $P_{out} = P_{in}$ (A.12)

which may be also written as $V_o I_o = (V_{g1} I_{g1} + V_{g2} I_{g2})$ (A.13)

Substituting 'V_o' from eq. (A.7) in (A.10)

$$\left(V_{g1} \left(\frac{d_1}{2-d_1} \right) + V_{g2} \left(\frac{d_2}{2-d_1-2d_2} \right) \right) I_o = V_{g1} I_{g1} + V_{g2} I_{g2} \quad (\text{A.14})$$

$$V_{g1} I_o \left(\frac{d_1}{2-d_1} \right) + V_{g2} I_o \left(\frac{d_2}{2-d_1-2d_2} \right) = V_{g1} I_{g1} + V_{g2} I_{g2} \quad (\text{A.15})$$

Comparing the RHS and LHS of eq. (A.11), the expressions for the two source currents I_{g1} and I_{g2} can be written as

$$I_{g1} = I_o \left(\frac{d_1}{2-d_1} \right) \quad (\text{A.16})$$

$$I_{g2} = I_o \left(\frac{d_2}{(2-d_1)(1-d_2)} \right)$$

Design of Capacitors:

For obtaining capacitance of the output capacitor C_2 , the ripple current flowing through capacitor C_2 during interval d_2T_s gives rise to the ripple voltage across the capacitor C_2 and is given by

$$\Delta V_{c2} = \frac{1}{C_2} \int_0^{d_2 T_s} I_o dt$$

$$C_2 = \left(\frac{I_o d_2}{\Delta V_{c2} f_s} \right) = \left(\frac{V_o d_2}{R \Delta V_{c2} f_s} \right) \quad (\text{A.17})$$

Similarly, the capacitor ‘ C_1 ’ is obtained when main switch S_2 is in OFF-state, the capacitor current is equal to the inductor current, which same as the source-2 current for the duration $(1-d_2) T_s$ and the corresponding capacitor ripple voltage is given by:

$$\Delta V_{c1} = \frac{1}{C_1} \int_{d_2 T_s}^{T_s} I_{g2} dt$$

$$C_1 = \left[\frac{I_{g2} (1-d_2)}{\Delta V_{c1} f_s} \right] \quad (\text{A.18})$$

By applying, amp-sec balance on the capacitors C_1 and C_2 (Figs. 2.10 to 2.12), the steady-state expressions of i_{L1} are found out.

The average current of the capacitor C_1 over one switching cycle is zero. Accordingly,

$$\langle i_{C1} \rangle = -i_{L1} d_2 + i_{L2} (d_1 - d_2) + i_{L2} (1 - d_1) = 0 \quad (\text{A.19})$$

$$i_{L2} = I_o \left[\frac{d_2}{(2-d_1)(1-d_2)} \right] \quad (\text{A.20})$$

Similarly, applying amp-second balance to the other capacitors

$$i_{L1} = I_o \left[\frac{1}{2-d_1} \right] \quad (\text{A.21})$$

A.1.2 Formulation of SIHBSTIC state-space model

In order to analyze the dynamic behavior and also to realize a controller, the converter operating modes are transformed into a set of first-order differential equations using the KVL and KCL approach, which ensures the conservation of energy. In each mode of operation, the power stage dynamics can easily be described by a set of state-space equations given by the first-order differential equations formulated for various inductor currents and capacitor voltages in the following lines. After that, these equations are transformed into a state-space model given below.

$$A_1 = \begin{bmatrix} \frac{K}{2L_1} & 0 & 0 & \frac{1}{2L_1} & 0 \\ 0 & -\frac{K}{2L_{12}} & 0 & \frac{1}{2L_{11}} & 0 \\ 0 & 0 & \frac{R_{L_2}}{L_2} & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_2(R + R_{c2})} \end{bmatrix}$$

$$A_2 = \begin{bmatrix} -\frac{K_3}{2L_1} & 0 & -\frac{K_1}{2L_1} & 0 & -\frac{K_2}{2L_1} \\ 0 & -\frac{K_3}{2L_{11}} & -\frac{K_1}{2L_{11}} & 0 & -\frac{K_2}{2L_{11}} \\ -\frac{K_1}{L_2} & 0 & \frac{K_4}{L_2} & -\frac{1}{L_2} & -\frac{K_2}{2L_2} \\ 0 & 0 & \frac{1}{C_1} & 0 & 0 \\ -\frac{(1-K_1)}{C_2} & 0 & 0 & 0 & -\frac{K_2}{RC_2} \end{bmatrix}$$

$$A_1 = \begin{bmatrix} -\frac{(K_1+K_5)}{L_1} & 0 & -\frac{K_1}{L_1} & 0 & -\frac{K_2}{L_1} \\ 0 & -\frac{(K_1+K_5)}{2L_{11}} & -\frac{K_1}{2L_{11}} & 0 & -\frac{K_2}{2L_{11}} \\ -\frac{K_1}{L_2} & 0 & -\frac{K_4}{L_2} & -\frac{1}{L_2} & -\frac{K_2}{2L_2} \\ 0 & 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{(1-K_1/R)}{C_2} & 0 & \frac{(1-K_1/R)}{C_2} & 0 & -\frac{K_2}{RC_2} \end{bmatrix}$$

$$\text{Where } K_1 = \left[\frac{1}{R+R_{C_2}} \right]; K_2 = \left[\frac{RR_{C_2}}{R+R_{C_2}} \right]; K_3 = \left[\frac{R_{C_2}}{R+R_{C_2}} \right]$$

$$B_1 = B_2 = \begin{bmatrix} 1/L_1 & 1/L_{11} & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & 0 & 0 \end{bmatrix}^T;$$

$$B_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & 0 & 0 \end{bmatrix}^T$$

$$E_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{R}{R+R_{C_2}} \end{bmatrix}; \quad E_2 = \begin{bmatrix} K_2 & 0 & K_2 & 0 & \frac{R}{R+R_{C_2}} \end{bmatrix}; \quad E_3 = \begin{bmatrix} K_2 & K_2 & K_2 & 0 & \frac{R}{R+R_{C_2}} \end{bmatrix}$$

$$F_1 = F_2 = F_3 = [0];$$

$$M_1 = M_2 = M_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-R}{R+R_{C_2}} \end{bmatrix}$$

$$J = \left[\frac{RR_{C_2}}{R+R_{C_2}} \right]$$

The above matrices are obtained for each mode and are used in the latter part of the thesis to obtain the state-space averaging model of the respective TIC which, is necessary for controller design.

A.2 Switched Capacitor Hybrid Buck SEPIC Two-input DC-DC Converter-1

Volt-second balance of inductor L_1 , L_2 , L_3 was solved using the equations mentioned in Table 2.8 in mode-1, mode-2, and mode-3.

$$\begin{aligned} \langle v_{L1} \rangle &= (V_{g1} - v_{C3} - V_o)d_2T_s + (V_{g1} - v_{C1})(1-d_1)T_s + (V_{g1} - v_{C1} - v_{C2})(1-d_1)T_s \\ &= V_{g1} - v_{C1}(1-d_2) - v_{C2}(1-d_1) - v_{C3}d_2 - V_o d_2 = 0 \end{aligned} \quad (\text{A. 22})$$

$$\begin{aligned} \langle v_{L2} \rangle &= V_{g2}d_2 + (V_{g2} - v_{C3} + v_{C1} - V_o)(d_1 - d_2) + (V_{g2} - v_{C3} - V_o)(1-d_1) \\ &= V_{g2} - v_{C3}(1-d_2) + v_{C1}(d_1 - d_2) - v_{C3}d_2 = 0 \end{aligned} \quad (\text{A. 23})$$

$$\begin{aligned} \langle v_{L3} \rangle &= -v_{C3}d_2 + (V_o - v_{C1})(d_1 - d_2) + V_o(1-d_1) \\ &= V_o(1-d_2) - v_{C1}(d_1 - d_2) - v_{C3}d_2 = 0 \end{aligned} \quad (\text{A.24})$$

On solving and rearranging the terms of the above equation, the following expressions are obtained.

$$v_{C1}(d_1 - d_2) = V_o(1-d_2) - v_{C3}d_2 \quad (\text{A.25})$$

Substituting eq. (A. 21) in eq. (A. 19)

$$V_{g2} - v_{C3}(1-d_2) + V_o(1-d_2) - v_{C3}d_2 - V_o(1-d_2) = 0$$

$$V_{g2} = v_{C3}$$

$$v_{C1}(d_1 - d_2) = V_o(1-d_2) - V_{g2}d_2$$

$$v_{C1} = V_o \frac{(1-d_2)}{(d_1 - d_2)} - V_{g2} \left(\frac{d_2}{(d_1 - d_2)} \right) \quad (\text{A.26})$$

Substituting eq. (A.22) in eq. (A.19)

$$V_{g1} - v_{C1}(1-d_2) - v_{C2}(1-d_1) - V_{g2}d_2 - V_o d_2 = 0$$

$$V_o = V_{g1} - V_{g2} - v_{C1} \frac{(1-d_2)}{d_2} - v_{C2} \frac{(1-d_1)}{d_2} \quad (\text{A.27})$$

Assuming $v_{C1} = v_{C2} = v_C$, and also neglecting the products and higher powers of duty ratio terms, substituting eq. (A.23) in eq. (A.24), results in

$$V_{g1} - \left(V_o \left(\frac{1-d_2}{d_1-d_2} \right) - V_{g2} \left(\frac{d_2}{d_1-d_2} \right) \right) * (2-d_1-3d_2+2d_1d_2) = 0$$

On solving the above equations, the voltage conversion ratio of this converter is obtained as:

$$V_o = V_{g1} \frac{d_1-d_2}{(2-d_1-3d_2+2d_1d_2)} + V_{g2} \frac{2d_2(1-d_1)}{(2-d_1-3d_2+2d_1d_2)} \quad (\text{A.28})$$

Expressions for source currents I_{g1} and I_{g2}

The load power for double input integrated converter is:

$P_o = (V_o I_o)$ where V_o , I_o are the load voltage and current, respectively. For a lossless system:

$$P_{out} = P_{in}$$

which may be also written as

$$V_o I_o = (V_{g1} I_{g1} + V_{g2} I_{g2})$$

Substituting 'V_o' from eq. (A.25)

$$V_{g1} I_o \left(\frac{d_1-d_2}{(2-d_1-3d_2+2d_1d_2)} \right) + V_{g2} I_o \left(\frac{2d_2(1-d_1)}{(2-d_1-3d_2+2d_1d_2)} \right) = V_{g1} I_{g1} + V_{g2} I_{g2} \quad (\text{A.29})$$

Equating both sides of eq. (A.26)

$$I_{g1} = I_o \left(\frac{d_1-d_2}{(2-d_1-3d_2+2d_1d_2)} \right)$$

$$I_{g2} = I_o \left(\frac{2d_2(1-d_1)}{(2-d_1-3d_2+2d_1d_2)} \right) \quad (\text{2.30})$$

A.2.1 Design of SCHBSTIC Topology-1 parameters

The ripple-based design approach is used to design the elements of SCHBSTIC Topology-1. The peak-to-peak current ripple is assumed to be less than 20%, while the voltage ripple is assumed to be less than 10%. The design parameters for validation are listed in Table 2.10. For obtaining capacitance of the output capacitor C₄, the ripple current flowing through capacitor

‘C₄’ during interval d₂T_s gives rise to the ripple voltage across the capacitor C₄ which is given by

$$\Delta V_{c4} = \frac{1}{C_4} \int_0^{d_2 T_s} (I_{g1} - I_o) dt$$

$$C_4 = \frac{2V_o d_2}{R f_s \Delta v_{c4}} \left(\frac{1 - d_1 - d_2}{(2 - d_1 - 3d_2 + 2d_1 d_2)} \right) \quad (\text{A.31})$$

Similarly, the capacitor C₁ is obtained when main switch (S₂) is in the OFF-state. Here, the capacitor current is equal to the inductor current, which same as the source-1 current for the duration (1-d₂) T_s and the corresponding capacitor ripple voltage is given by

$$\Delta V_{c1} = \frac{1}{C_1} \int_{(1-d_1)T_s}^{T_s} I_{g1} dt$$

$$C_1 = C_2 = \frac{V_o(1-d_1)}{R \Delta v_{c1} f_s} \left(\frac{d_1 - d_2}{(2 - d_1 - 3d_2 + 2d_1 d_2)} \right) \quad (\text{A.32})$$

$$\Delta V_{c3} = \frac{1}{C_3} \int_{(1-d_1)T_s}^{T_s} I_{g2} dt$$

$$C_3 = \frac{V_o(1-d_1)}{R \Delta v_{c1} f_s} \left(\frac{2d_2(1-d_1)}{(2 - d_1 - 3d_2 + 2d_1 d_2)} \right) \quad (\text{A.33})$$

A.2.2 Formulation of SCHBSTIC Topology-1 state-space model

In order to analyze the dynamic behavior and also to design a controller, the converter operating modes are transformed into a set of first-order differential equations using the KVL and KCL approach. In each mode of operation, the power stage dynamics can easily be described by a set of state equations given by the following first order differential equations which are formulated for various inductor currents and capacitor voltages. These equations are then

transformed into state-space model and the state-space matrices are obtained and are given below.

$$A_1 = \begin{bmatrix} \frac{(R_{L1} + R_{C3} + (RR_{C4}/P))}{-L_1} & 0 & \frac{-R_{C3}}{L_1} & 0 & 0 & \frac{-1}{L_1} & \frac{R}{L_1 P} \\ 0 & \frac{R_{L2}}{L_2} & 0 & 0 & 0 & 0 & 0 \\ \frac{R_{C3}}{L_3} & 0 & \frac{(R_{C3} + R_{L3})}{-L_3} & 0 & 0 & \frac{1}{L_3} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1/C_3 & 0 & 1/C_3 & 0 & 0 & 0 & 0 \\ \frac{R_{C4}}{PC_4} & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_4 P} \end{bmatrix}$$

$$A_2 = \begin{bmatrix} \frac{QR_{L1} + R_{C1}R_{C2}}{-QL_1} & \frac{R_{C1}R_{C2}}{L_1Q} & \left[\frac{-R_{C1}R_{C2}}{L_1Q} \right] & \frac{-R_{C2}}{L_1Q} & \frac{-R_{C1}}{L_1Q} & 0 & 0 \\ \frac{R_{C1}R_{C2}}{L_2Q} & \frac{-1}{L_2} \left[R_{L2} + R_{C3} + \frac{RR_{C4}}{P} + \frac{R_{C1}R_{C2}}{Q} \right] & \frac{1}{L_2} \left[\frac{RR_{C4}}{P} + \frac{R_{C1}R_{C2}}{Q} \right] & \frac{-R_{C2}}{L_2Q} & \frac{R_{C2}}{L_2Q} & \frac{-1}{L_2} & \frac{R}{L_2 P} \\ \frac{R_{C1} + R_{C2}}{-L_3Q} & \frac{1}{L_3} \left[\frac{RR_{C4}}{P} + \frac{R_{C1}R_{C2}}{Q} \right] & \frac{-1}{L_3} \left[R_{L3} + \frac{RR_{C4}}{P} + \frac{R_{C1}R_{C2}}{Q} \right] & \frac{-R_{C2}}{L_3Q} & \frac{-R_{C2}}{L_3Q} & 0 & \frac{-R_{C4}}{L_3 P} \\ \frac{R_{C2}}{C_1Q} & \frac{-R_{C2}}{C_1Q} & \frac{R_{C2}}{C_1Q} & \frac{-1}{C_1Q} & \frac{1}{C_1Q} & 0 & 0 \\ \frac{R_{C1}}{C_2Q} & \frac{-R_{C1}}{C_2Q} & \frac{R_{C1}}{C_2Q} & \frac{1}{C_2Q} & \frac{1}{C_2Q} & 0 & 0 \\ 0 & 1/C_3 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{R}{C_4P} & \frac{-R}{C_4P} & 0 & 0 & 0 & \frac{-1}{C_4 P} \end{bmatrix}$$

$$A_3 = \begin{bmatrix} \frac{R_{L1} + R_{C3} + R_{C2}}{-L_1} & 0 & 0 & \frac{-1}{L_1} & \frac{-1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_2} \left[R_{L2} + R_{C3} + \frac{RR_{C4}}{P} \right] & \frac{R_{C4}}{L_2 P} & 0 & 0 & \frac{-1}{L_2} & \frac{-R_{C4}}{L_2 P} \\ 0 & \frac{RR_{C4}}{L_3(R + R_{C4})} & \frac{-1}{L_3} \left(R_{L3} + \frac{RR_{C4}}{P} \right) & 0 & 0 & 0 & \frac{R_{C4}}{L_3 P} \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{R}{C_4 P} & \frac{-R}{C_4 P} & 0 & 0 & 0 & \frac{-1}{C_4 P} \end{bmatrix}$$

$$P = \left[\frac{1}{R + R_{C4}} \right]$$

$$B_1 = B_2 = B_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & 0 & 0 \end{bmatrix}^T$$

$$E_1 = \left[\frac{RR_{C4}}{R + R_{C4}} \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad \frac{R}{R + R_{C4}} \right]; \quad E_2 = E_3 = \left[0 \quad \frac{RR_{C4}}{R + R_{C4}} \quad -\frac{RR_{C4}}{R + R_{C4}} \quad 0 \quad 0 \quad 0 \quad \frac{R}{R + R_{C4}} \right]$$

$$F_1 = F_2 = F_3 = [0];$$

$$M_1 = M_2 = M_3 = \left[0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad \frac{-R}{R + R_{C4}} \right]$$

$$J = \left[\frac{RR_{C4}}{R + R_{C4}} \right]$$

A.3. Quadratic Buck-SEPIC DC-DC Converter

$$\langle v_{L1} \rangle = (V_{g1} - v_{C1o})d_2 T_s + (V_{g1} - v_{C1})(d_1 - d_2)T_s + (-v_{C1})(1 - d_1)T_s = 0$$

$$V_{g1} = v_{C1}(d_1) \tag{A.34}$$

Volt-second balance of inductor L_2 was solved using the equations mentioned Table 2.7 for

mode-2

$$\langle v_{L2} \rangle = V_{g2}d_2 + (V_{g2} - v_{C2} - V_o)(d_1 - d_2) + (V_{g2} - v_{C2} - V_o)(1 - d_1) = 0$$

$$v_{C2} = V_{g2} \frac{1}{(1 - d_2)} - V_o \tag{A.35}$$

Volt-second balance of inductor L_2 was solved using the equations mentioned in Table 2.7 for mode-3

$$\langle v_{L3} \rangle = (v_{c1} + v_{c2})d_2 + (v_{c1} - V_o)(d_1 - d_2) - V_o(1 - d_1) = 0$$

$$v_{c1}d_1 + v_{c2} - d_2 - V_o(1 - d_2) = 0 \quad (\text{A.36})$$

Substituting eq. (A.31) and (A.32) in eq. (A.33)

$$V_{g1}d_1^2 + V_{g2} \frac{d_2}{1 - d_2} - V_o = 0 \quad (\text{A.37})$$

On rearranging the terms, the voltage conversion ratio of this converter is obtained as

$$V_o = V_{g1}d_1^2 + V_{g2} \frac{d_2}{(1 - d_2)} \quad (\text{A.38})$$

Applying the amp-second balance, the relation between different currents are obtained and given in eq. (A.36).

$$i_{L1} = i_{L3}d_1 ; i_{L3} = I_o \quad (\text{A.39})$$

$$i_{L2} = i_{L3} \left[\frac{d_2}{1 - d_2} \right] \quad (\text{A.36a})$$

$$i_{L2} = i_{L1} \left[\frac{d_2}{d_1(1 - d_2)} \right] \quad (\text{A.36b})$$

A.3.1 Design of QBSTIC parameters

For obtaining capacitance of the output capacitor C_3 , the ripple current flowing through capacitor 'C₃' during interval d_2T_s gives rise to the ripple voltage across the capacitor C_3 and is given by

$$\Delta V_{c3} = \frac{1}{C_3} \int_0^{d_2T_s} (I_o) dt$$

$$C_3 = \frac{V_o d_2}{R f_s \Delta V_{c3}} \quad (\text{A.40})$$

Similarly, the capacitor C_1 is obtained when the main switch (S_2) is in OFF-state then the capacitor current is equal to the inductor current, which is also same as the source-1 current for the duration $(1-d_2) T_s$ and the corresponding capacitor ripple voltage is given by

$$\Delta V_{c1} = \frac{1}{C_1} \int_0^{(1-d_1)T_s} (i_{L1} - i_{L3}) dt$$

$$C_1 = \frac{V_o d_1 (1-d_1)}{R \Delta v_{c1} f_s} \quad (\text{A.41})$$

$$\text{And } \Delta V_{c2} = \frac{1}{C_2} \int_{(d_1-d_2)T_s}^{(1-d_1)T_s} (i_{L2}) dt$$

$$C_2 = \frac{V_o d_2}{R \Delta v_{c2} f_s} \quad (\text{A.42})$$

A.3.2 Formulation of QBSTIC state-space model

In order to analyze the dynamic behavior and also to design a controller, the converter operating modes are transformed into a set of first-order differential equations using the KVL and KCL approach. In each mode of operation, the power stage dynamics can easily be described by a set of state equations given by the following first order differential equations which are formulated for various inductor currents and capacitor voltages. These equations are then transformed into state-space model and the state-space matrices are obtained and are given below.

$$A_1 = \begin{bmatrix} \frac{-(R_{L1} + R_{C1})}{L_1} & 0 & \frac{R_{C1}}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-R_{L2}}{L_2} & 0 & 0 & 0 & 0 \\ \frac{-R_{C1}}{L_3} & 0 & \frac{-(R_{L3} - R_{C1})}{L_3} & \frac{1}{L_3} & \frac{1}{L_3} & 0 \\ \frac{1}{C_1} & \frac{-1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_3(R)} \end{bmatrix}$$

$$A_2 = \begin{bmatrix} \frac{-(R_{L1} + R_{C1})}{L_1} & 0 & \frac{R_{C1}}{L_1} & \frac{-1}{L_1} & 0 & 0 \\ 0 & \frac{-(R_{L2} + K_1)}{L_2} & \frac{-K_1}{L_2} & 0 & \frac{-1}{L_2} & \frac{-K_2}{L_2} \\ 0 & \frac{-K_1}{L_3} & \frac{-(K_1)}{L_3} & 0 & 0 & \frac{-K_2}{L_3} \\ \frac{1}{C_1} & \frac{-1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{K_1}{C_3 R_{C3}} & \frac{K_1}{C_3 R_{C3}} & 0 & 0 & \frac{-K_2}{R} \end{bmatrix}$$

$$A_3 = \begin{bmatrix} \frac{-(R_{L1} + R_{C1})}{L_1} & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & \frac{-(R_{L2} + K_1)}{L_2} & \frac{-K_1}{L_2} & 0 & \frac{-1}{L_2} & \frac{-K_2}{L_2} \\ 0 & \frac{-K_1}{L_3} & \frac{-(K_1 + R_{L3})}{L_3} & 0 & 0 & \frac{-K_2}{L_3} \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{K_1}{C_3} & \frac{K_1}{C_3} & 0 & 0 & \frac{-K_2}{R} \end{bmatrix}$$

$$B_1 = B_2 = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & 0 & 0 & 0 \end{bmatrix}^T; \quad B_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & 0 & 0 & 0 \end{bmatrix}^T$$

$$E_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & \frac{R}{R + R_{C3}} \end{bmatrix}; \quad E_2 = E_3 = [0 \quad K_1 \quad K_1 \quad 0 \quad 0 \quad K_2]$$

$$K_1 = \frac{RR_{C3}}{R + R_{C3}}; \quad K_2 = \frac{R}{R + R_{C3}}; \quad K_3 = \frac{1}{R + R_{C3}}$$

$$F_1 = F_2 = F_3 = [0];$$

$$M_1 = M_2 = M_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & \frac{-R}{R + R_{C3}} \end{bmatrix}$$

$$J = \begin{bmatrix} \frac{RR_{C3}}{R + R_{C3}} \end{bmatrix}$$

A.4. Switched Capacitor Hybrid Buck SEPIC Two-input DC-DC Converter-2

By applying 'volt-sec' balance for L₁:

$$(V_{g1} - V_0)d_2T_s + (V_{g1} - V_0)(d_1 - d_2)T_s + (V_{g1} - 2v_{c1} - V_0)(1 - d_1)T_s = 0 \quad (\text{A.43})$$

$$v_{c1} = \frac{(V_{g1} - V_0)}{2(1 - d_1)} \quad (\text{A.44})$$

By applying 'volt-sec' balance for L₂:

$$(V_{g2})d_2T_s + (V_{g2} + v_{c1} - v_{c3} - V_0)(d_1 - d_2)T_s + (V_{g2} - v_{c3} - V_0)(1 - d_1)T_s = 0 \quad (\text{A.45})$$

By applying 'volt-sec' balance for L₃:

$$(-v_{c3})d_2T_s + (V_0 - v_{c1})(d_1 - d_2)T_s + (V_0)(1 - d_1)T_s = 0 \quad (\text{A.46})$$

By using eq. (A.42) and (A.43):

$$v_{c3} = V_{g2} \quad (\text{A.47})$$

Solving the above equations, the voltage gain expression is obtained as:

$$V_0 = V_{g1} \left[\frac{(d_1 - d_2)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right] + V_{g2} \left[\frac{2d_2(1 - d_1)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right] \quad (\text{A.48})$$

Expressions for source currents I_{g1} and I_{g2}

The load power for double input integrated converter is:

$P_o = (V_o I_o)$ where V_o, I_o are the load voltage and current, respectively. For a lossless system:

$$P_{out} = P_{in} \quad (\text{A.49})$$

which may be also written as

$$V_o I_o = (V_{g1} I_{g1} + V_{g2} I_{g2}) \quad \text{Substituting 'V}_o\text{' from eq. (A.45)}$$

$$V_{g1}I_o \left(\frac{d_1 - d_2}{(2 - d_1 - 3d_2 + 2d_1d_2)} \right) + V_{g2}I_o \left(\frac{2d_2(1 - d_1)}{(2 - d_1 - 3d_2 + 2d_1d_2)} \right) = V_{g1}I_{g1} + V_{g2}I_{g2} \quad (\text{A.50})$$

Equating both sides of eq. (A.47)

$$I_{g1} = I_o \left(\frac{d_1 - d_2}{(2 - d_1 - 3d_2 + 2d_1d_2)} \right)$$

$$I_{g2} = I_o \left(\frac{2d_2(1 - d_1)}{(2 - d_1 - 3d_2 + 2d_1d_2)} \right) \quad (\text{A.51})$$

A.4.1 Design of SCHBSTIC Topology-2 parameters

The ripple-based design approach is used to design the elements of SCHBSTIC Topology-2. The peak-to-peak current ripple is assumed to be less than 20%, while the voltage ripple is assumed to be less than 10%. The design parameters for validation are listed in Table 2.21. For obtaining capacitance of the output capacitor C_4 , the ripple current flowing through capacitor ‘ C_4 ’ during interval d_2T_s gives rise to the ripple voltage across the capacitor C_4 which is given by

$$\Delta V_{c4} = \frac{1}{C_4} \int_0^{d_2T_s} (I_{g1} - I_o) dt$$

$$C_4 = \frac{(I_{g1} - I_o)d_2}{R f_s \Delta v_{c4}} \quad (\text{A.52})$$

$$\text{Where } I_{g1} = \left[\frac{I_o(d_1 - d_2)}{2(1 - d_1)(1 - d_2) + (d_1 - d_2)} \right]; I_o = \frac{V_o}{R}$$

Similarly, the capacitor C_1 is obtained.

Similarly, the capacitor C_1 is obtained when the main switch (S_2) is in OFF-state then the capacitor current is equal to the inductor current, which is also same as the source-1 current for the duration $(1 - d_2)T_s$ and the corresponding capacitor ripple voltage is given by

$$\Delta V_{c1} = \Delta V_{c2} = \frac{1}{C_1} \int_{(d_1 - d_2)T_s}^{(1 - d_1)T_s} (I_{g1}) dt$$

$$C_1 = C_2 = \frac{I_{g1}(1-d_2)}{\Delta v_{c2} f_s} \quad (\text{A.53})$$

$$\text{Where } I_{g1} = \left[\frac{I_o(d_1 - d_2)}{2(1-d_1)(1-d_2) + (d_1 - d_2)} \right]; I_o = \frac{V_o}{R}$$

A.4.2 Formulation of QBSTIC state-space model

In order to analyze the dynamic behavior and also to design a controller, the converter operating modes are transformed into a set of first-order differential equations using the KVL and KCL approach. In each mode of operation, the power stage dynamics can easily be described by a set of state equations given by the following first order differential equations which are formulated for various inductor currents and capacitor voltages. These equations are then transformed into state-space model and the state-space matrices are obtained and are given below.

$$[A_1] = \begin{bmatrix} \frac{-(r_1 + a)}{L_1} & 0 & 0 & 0 & 0 & 0 & \frac{-b}{L_1} \\ 0 & \frac{-r_2}{L_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-(r_{c3} + r_3)}{L_3} & 0 & 0 & \frac{-1}{L_3} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 \\ \frac{b}{C_4} & 0 & 0 & 0 & 0 & 0 & \frac{-b}{RC_4} \end{bmatrix},$$

$$[B_1] = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, E_1 = [a \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad b],$$

$$[A_2] = \begin{bmatrix} \frac{-(r_1+a)}{L_1} & \frac{-a}{L_1} & \frac{a}{L_1} & 0 & 0 & 0 & \frac{-b}{L_1} \\ \frac{-a}{L_2} & \frac{-k_2}{L_2} & \frac{(a+p_1)}{L_2} & \frac{r_{c2}}{R_c L_2} & \frac{r_{c1}}{R_c L_2} & \frac{-1}{L_2} & \frac{-b}{L_2} \\ \frac{a}{L_3} & \frac{(a+p_1)}{L_3} & \frac{-(a+p_1+r_3)}{L_3} & \frac{-r_{c2}}{R_c L_3} & \frac{-r_{c1}}{R_c L_3} & 0 & \frac{b}{L_3} \\ 0 & \frac{-r_{c2}}{R_c C_1} & \frac{r_{c2}}{R_c C_1} & \frac{-1}{R_c C_1} & \frac{1}{R_c C_1} & 0 & 0 \\ 0 & \frac{-r_{c1}}{R_c C_2} & 0 & \frac{1}{R_c C_2} & \frac{-1}{R_c C_2} & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 \\ \frac{b}{C_4} & \frac{b}{C_4} & \frac{-b}{C_4} & 0 & 0 & 0 & \frac{-b}{RC_4} \end{bmatrix},$$

$$[B_2] = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, E_2 = [a \quad a \quad -a \quad 0 \quad 0 \quad 0 \quad b],$$

$$[A_3] = \begin{bmatrix} \frac{-k_1}{L_1} & \frac{-a}{L_1} & \frac{a}{L_1} & \frac{-1}{L_1} & \frac{-1}{L_1} & 0 & \frac{-b}{L_1} \\ \frac{-a}{L_2} & \frac{-(a+r_{c3})}{L_2} & \frac{a}{L_2} & 0 & 0 & \frac{-1}{L_2} & \frac{-b}{L_2} \\ \frac{a}{L_3} & \frac{a}{L_3} & \frac{-(a+r_3)}{L_3} & 0 & 0 & 0 & \frac{b}{L_3} \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 \\ \frac{b}{C_4} & \frac{b}{C_4} & \frac{-b}{C_4} & 0 & 0 & 0 & \frac{-b}{RC_4} \end{bmatrix},$$

$$[B_3] = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, E_3 = [a \quad a \quad -a \quad 0 \quad 0 \quad 0 \quad b].$$

$$\text{Where } a = \frac{Rr_{c4}}{(R+r_{c4})}; b = \frac{R}{(R+r_{c4})};$$

$$R_C = r_{c1} + r_{c2}; p_1 = \frac{(r_{c1}r_{c2})}{R_c};$$

$$k_1 = (r_1 + r_{c1} + r_{c2} + a);$$

$$k_2 = (r_2 + r_{c3} + a + p_1).$$

The important terms used for deriving various expressions of chapter 2,3 of TICs:

SIHBSTIC	QBSTIC
$a_{si} = \frac{d_1}{(2-d_1)}; \quad g_{si} = \frac{1}{(2-d_1)}$ $H_{si} = [g_{si} + b_{si} - 1]; \quad e_{sq} = (1+b_{sq})$ $M_{si} = \frac{V_{g2}}{(1-d_2)} - V_o; \quad b_{sq} = \frac{d_2}{(1-d_2)};$ $d_{sq} = \frac{d_2}{d_1^2(1-d_2)}; \quad K_q = \frac{V_{g2}}{(1-d_2)} - V_o;$ $N_{si} = \frac{d_2}{(1-d_2)}; \quad S_{gi} = \frac{V_o(2-d_1) - V_{g1}d_1}{V_{g2}}$ $K_{si1} = (1-d_1)(2-d_2); \quad K_{si2} = (2-d_1)(1-d_2)$ $Q_x = \frac{2}{(2-d_1)} + \frac{d_2}{(2-d_1)(1-d_2)} - 1;$ $Q_{gi} = \frac{d_1 + d_2 - d_1d_2}{(2-d_1)(1-d_2)}$	$a_{sq} = d_1^2$ $b_{sq} = \frac{d_2}{(1-d_2)}$ $d_{sq} = \frac{d_2}{d_1^2(1-d_2)}$ $K_q = \frac{V_{g2}}{(1-d_2)} - V_o$ $e_{sq} = (1+b_{sq})$
SCHBSTIC-1	SCHBSTIC-2
$a_{sc1} = \frac{d_1 - d_2}{(2-d_1 - 3d_2 + 2d_1d_2)} = H_{1sc1}$ $b_{sc1} = \frac{2d_2(1-d_1)}{(2-d_1 - 3d_2 + 2d_1d_2)} = H_{2sc1}$ $H_{3sc1} = H_{1sc1} - \frac{(H_{2sc1} - 1)}{2}$ $K_{sc1} = \frac{V_{g1} - V_o}{2(1-d_1)}$ $M_{sc1} = H_{1sc1}^2 d_2 + H_{3sc1}^2 (d_1 - d_2)$	$a_{sc2} = \frac{d_1 - d_2}{(2-d_1 - 3d_2 + 2d_1d_2)};$ $b_{sc2} = \frac{2d_2(1-d_1)}{(2-d_1 - 3d_2 + 2d_1d_2)}$ $d_{sc2} = 2 - d_1 - 3d_2 + 2d_1d_2$

The following table gives the representation of duty ratio of TICs in terms of V_{g1} , V_{g2} , V_0

TICs	Duty ratio ' d_1 '	Duty ratio ' d_2 '
SIHBSTIC	$\frac{2V_0 - V_{g2} \left(\frac{d_2}{1-d_2} \right)}{V_0 + V_{g1}}$	$\frac{V_0(2-d_1) - V_{g1}d_1}{V_0(2-d_1) - V_{g1}d_1 + V_{g2}}$
SCHBSTIC1	$\frac{d_2(2V_{g2} + 3V_0 - V_{g1}) - 2V_0}{2V_{g2}d_2 - V_{g1} - V_0 + 2V_0d_2}$	$\frac{2V_0 - V_0d_1 - V_{g1}d_1}{2V_{g2} + 3V_0 - V_{g1} - 2V_{g1}d_1 - 2V_0d_1}$
SCHBSTIC2	$\frac{d_2(2V_{g2} + 3V_0 - V_{g1}) - 2V_0}{2V_{g2}d_2 - V_{g1} - V_0 + 2V_0d_2}$	$\frac{2V_0 - V_0d_1 - V_{g1}d_1}{2V_{g2} + 3V_0 - V_{g1} - 2V_{g1}d_1 - 2V_0d_1}$
QBSTIC	$\sqrt{\frac{V_0 - V_{g2} \left[\frac{d_2}{1-d_2} \right]}{V_{g1}}}$	$\frac{V_0 - V_{g1}d_1^2}{V_0 + V_{g2}}$

The following table gives the expression of Source Voltages in terms of each other and the duty ratio.

TIC	V_{g1}	V_{g2}
SIHBSTIC	$\frac{V_0 - V_{g2}b_{s_i}}{a_{s_i}}$	$\frac{V_0 - V_{g1}a_{s_i}}{b_{s_i}}$
SCHBSTIC1	$\frac{V_0 - V_{g2}H_2}{H_1}$	$\frac{V_0 - V_{g1}H_1}{H_2}$
SCHBSTIC2	$\frac{V_0 - V_{g2}b_{s_{c2}}}{a_{s_{c2}}}$	$\frac{V_0 - V_{g1}a_{s_{c2}}}{b_{s_{c2}}}$
QBSTIC	$\frac{V_0 - V_{g2}b_{s_q}}{a_{s_q}}$	$\frac{V_0 - V_{g1}a_{s_q}}{b_{s_q}}$

The expression for the output power sharing among source-1 and source-2 is deduced using the expressions given below:

$$P_{g1} = P_o \left[\frac{V_{gx} d_{gx}}{1 + V_{gx} d_{gx}} \right];$$

$$P_{g2} = P_o \left[\frac{1}{1 + V_{gx} d_{gx}} \right]$$

where $V_{gx} = \left[\frac{V_{g1}}{V_{g2}} \right]$

The suffix ‘x’ may be replaced by ‘i’ for SIHBSTIC, ‘sc1’ for SCHBSTIC1, ‘sc2’ for SCHBSTIC2, and ‘sq’ for QBSTIC”.

TIC	Duty Ratio
SIHBSTIC	$d_{gi} = \frac{d_1(1-d_2)}{d_2}$
SCHBSTIC1	$d_{gsc1} = \frac{(d_1-d_2)}{2d_2(1-d_1)}$
SCHBSTIC2	$d_{gsc2} = \frac{(d_1-d_2)}{2d_2(1-d_1)}$
QBSTIC	$d_{gsq} = \frac{d_1^2(d_1-d_2)}{2d_2(1-d_1)}$

A.5. Techniques used for TIC Controller Synthesis.

Methodology 1: Power Management Control Strategy

The discussion in paper [11] deals with three distinct power status combination situations that can be suggested to double-input dc/dc converter which has two input voltage sources and one output load to obtain a regulated voltage, where the power for each one of them can be either controlled or undetermined.

Case I: In instance I, the load will use the required power by drawing a constant current, the high-voltage source will only offer a portion of the required constant power, and the low-voltage source will supply the remaining portion. The high-voltage source is the primary power source for the load in the converter used in scenario I, while the low-voltage source is an auxiliary power source. If the input current of the high-voltage source is not under control for the continuous load current demand, the low-voltage source will supply the remaining current required by the load current.

Case II: Case II is similar to Case I in that the low-voltage source will only offer a small amount of consistent power, and the high-voltage source will not be able to supply the full amount of power that the load requires. The previously described voltage and current equations can also be used to illustrate the control strategy for case II, which is the same as that for case I. The duty ratio d_{LO} is calculated in order to manage the low-voltage input current I_{LO} with a constant load current I_O . The duty ratio d_{HI} for a high-voltage source can be computed with constant input and output voltages and the established d_{LO} . The high-voltage source input current I_{HI} can be calculated after d_{HI} and d_{LO} are known.

Case III: In this scenario, the load must be capable of absorbing the energy produced by both the high- and low-voltage sources. A typical load of the power system for case III, where the two voltage sources can always provide the maximum power to the load, is a rechargeable battery.

The electrical properties of the load will dictate the output which can be used to determine the duty ratios d_{HI} and d_{LO} .

Methodology 2: Integrated digital controller design

The control scheme mentioned in [76] has three controlled duty ratios to regulate the power flow from three power ports, and a fourth port is used to keep the balance of power. Only three of the ports have their working points carefully controlled, while the fourth port was left "flexible" and allowed to run at any position that complies with the power balancing limitations. The feedback control structure, which is based on several control objectives, is dictated by the selection of the flexible power port. If the battery is left "flexible," the maximum power from the wind and solar sources can be tracked by their port currents or voltages independently, and the load voltage can be managed by a voltage feedback as well.

Methodology 3: Power Budgeting control method

A closed loop regulating control [77] was sought in order to more effectively illustrate power budgeting. To demonstrate the converter using non-ideal sources, a solar panel and a rectified line supply were utilized. Two separate proportional-integral (PI) controllers were combined into a straightforward control. The first PI loop modifies the line source's duty cycle so that it tracks a reference output voltage. The second PI loop, which has a significantly slower time constant, modifies the solar input's duty cycle to follow a reference input voltage. The greatest power point is quickly. In order to leave advanced control design to future work, the control gains were chosen to provide a delayed reaction.

Methodology 4: Independent loop control method

This methodology demonstrates in [78] shows how two control inputs, d_1 and d_2 , can be separately regulated with different control objectives for each loop. The inner current control loop $T_i(s)$ maintains the average switch current I_{s2} by average switch current control. Once the

inner current control loop $T_i(s)$ is closed, the perturbations in d_1 are treated as disturbance signals for the inner loop in an effort to lessen this dependence, which results in control of d_2 with comparable perturbations depicts the dependence of $V_o(s)$ on the two control inputs.

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