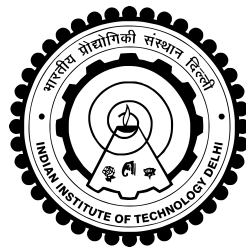


**HIGH DYNAMIC RANGE
CMOS IMAGE SENSORS
FOR LOW LIGHT APPLICATIONS**

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**DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY DELHI
AUGUST, 2023**

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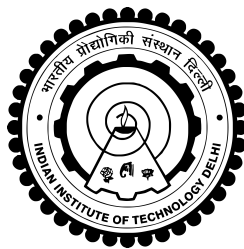
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Submitted

in fulfillment of the requirements of the degree of Doctor of Philosophy
to the



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AUGUST, 2023

In loving memory of Dr. Major Amit Handa

Certificate

This is to certify that the thesis entitled “**High Dynamic Range CMOS Image sensors for Low Light Applications**”, being submitted by **Mrs. Neha Priyadarshini** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by her under my supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

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Neha Priyadarshini

Abstract

This thesis presents dynamic range extension techniques for CMOS image sensors tailored for low light applications. The standard dynamic range of a CMOS imager is 50-60 dB. A high dynamic range (HDR) CMOS image sensor has the ability to capture a greater light range. Thus, it can successfully reproduce the high contrast information in a scene. The dynamic range of a CMOS image sensor in low light is limited by the noise floor of the sensor. Enhancement of dynamic range in low light requires suppression of the electronic noise or modification of signal readout such that it can overcome the electronic noise.

Several techniques allow sensors to perform low light detection. However, there are many trade-offs to enhancing the low light detection capability. Many signal multiplication techniques require higher power budgets, a larger pixel area and a reduction in the high light dynamic range. Whereas, noise suppression techniques require complicated and costly fabrication process modifications or a larger area and power consumption.

This thesis is motivated by the need to have low light sensing imagers without compromising on the power and area budget especially pixel area. The techniques presented here involve minimal additional hardware that does not introduce noise of its own and does not require process modification. They are compatible with existing standard fabrication processes and require minor or no changes in the standard 3T and 4T pixel architectures. Thus, they are simple to implement and cost effective. Moreover, the dynamic range is user programmable which assists the user to optimally decide the required range and simultaneously have control on other performance parameters like sensitivity and frame rate. The

flexibility provided by the proposed techniques should make their inclusion in low light sensing applications straightforward and effortless.

The underlying approach for the first prototype is a two way approach for optimum performance. First method is to increase the signal gain in the early stage of the signal chain. This makes the noise sources appearing afterwards less noticeable at the output. Second method is to decrease the noise floor itself. For signal gain enhancement, the proposed pixel architecture achieves user-programmable conversion gain modulation by periodically varying the gate-bulk capacitance of the in-pixel source follower. To implement this technique, the source follower is re-configured as a MOS capacitor for part of the pixel operation. A prototype sensor containing a 64×64 array of the proposed pixels has been fabricated in AMS $0.35 \mu\text{m}$, 3.3 V CMOS technology to verify the operation. The $10 \mu\text{m}$ pitch pixel has a 20.25% fill factor. The pixel is capable of providing standard integrated photo-signal in high illumination and amplified signal in low illumination which results in an 18 dB dynamic range enhancement after combining the outputs. Only one additional NMOS transistor is used in the pixel as compared to a standard 4T pixel to achieve the enhancement. The power consumed by the imager is 3.55 mW.

For noise reduction, the low frequency noise of the in-pixel source follower is identified as a major bottleneck. The previously outlined architecture is re-used with a modified timing to obtain $1/f$ noise reduction and high conversion gain. $1/f$ noise is reduced by periodically switching the in-pixel source follower between depletion and inversion. The depletion state is achieved by re-configuring the source follower into a MOS capacitor and

depleting the channel by controlling the source-drain terminal. As mentioned above, the state change of the in-pixel source follower also enhances the conversion gain. Experimental verification shows the measured integrated noise at the output of a pixel in the frequency band 128 Hz to 50 KHz to be $728 \mu V_{rms}$ without switching. At a switching frequency of 4 MHz, the output integrated noise reduces to $306 \mu V_{rms}$ after switching resulting in a 7.5 dB reduction. The input referred noise in electrons calculated with the help of photon transfer curve method shows a reduction from $26e_{rms}^-$ to $7.3e_{rms}^-$ after applying switching. When both, switching and conversion gain enhancement are applied, the input referred noise is further reduced to $2.3e_{rms}^-$ with an enhanced conversion gain of $398 \mu V/e^-$.

Most HDR techniques in CMOS technology require on-chip or off-chip reconstruction of images taken at multiple gain settings or multiple integration times. Alternatively, a one-shot HDR sensor which directly captures the HDR scene requires no reconstruction and is highly preferred. The next technique proposed in this thesis enhances low light dynamic range and has a one shot HDR response. The technique employs pulse width modulation and a modified counting scheme to provide a convenient, user-programmable method for controlling the dynamic range and sensitivity depending upon the ambient light. The PWM technique offers uniform SNR which is independent of photo-diode current. This aspect is utilized to improve imaging particularly in the low light region. A prototype sensor composed of a 128×128 array of standard 3T-pixels, an area-efficient column circuitry with double sampling operation, a 10-bit memory, and a modified chip level counter has been fabricated to test the algorithm. The test chip has been fabricated in 350 nm AMS

process. The maximum dynamic range obtained is 95 dB and the power consumption measured at 36 fps is 8.4 mW with a 3.3 V power supply.

सार

यह थीसिस CMOS सेंसर के लिए गतिशील रेंज विस्तार तकनीकों को प्रस्तुत करती है कम रोशनी वाले अनुप्रयोगों के लिए. CMOS इमेजर की मानक गतिशील रेंज 50-60 डीबी है. एक उच्च गतिशील रेंज (एचडीआर) CMOS छवि सेंसर में अधिक से अधिक कैप्चर करने की क्षमता होती है प्रकाश सीमा. इस प्रकार, यह किसी दृश्य में उच्च कंट्रास्ट जानकारी को सफलतापूर्वक पुनः पेश कर सकता है।

कम रोशनी में CMOS इमेज सेंसर की गतिशील रेंज शोर तल द्वारा सीमित होती है. कम रोशनी में गतिशील रेंज को बढ़ाने के लिए इलेक्ट्रॉनिक के दमन की आवश्यकता होती है सिग्नल रीडआउट का शोर या संशोधन इस तरह से कि यह इलेक्ट्रॉनिक शोर पर काबू पा सके। कई तकनीकें सेंसर को कम रोशनी का पता लगाने की अनुमति देती हैं। हालाँकि, वहाँ हैं कम रोशनी का पता लगाने की क्षमता को बढ़ाने के लिए कई बदलाव किए गए। अनेक संकेत गुणन तकनीकों के लिए उच्च बिजली बजट, बड़े पिक्सेल क्षेत्र और उच्च रोशनी में कमी की आवश्यकता होती है। जबकि, शोर दमन तकनीकों के लिए जटिल और महंगी आवश्यकता होती है निर्माण प्रक्रिया में संशोधन या बड़े क्षेत्र और बिजली की खपत।

यह थीसिस बिना किसी समझौता के कम प्रकाश संवेदन इमेजर्स की आवश्यकता से प्रेरित है बिजली और क्षेत्र बजट, विशेषकर पिक्सेल क्षेत्र पर। तकनीकें प्रस्तुत की गईं यहां न्यूनतम अतिरिक्त हार्डवेयर शामिल है जो स्वयं का शोर उत्पन्न नहीं करता है और करता है प्रक्रिया संशोधन की आवश्यकता नहीं है. वे मौजूदा मानक निर्माण के साथ संगत हैं प्रक्रियाओं और मानक 3T और 4T पिक्सेल आर्किटेक्चर में मामूली या कोई बदलाव की आवश्यकता नहीं है।

इस प्रकार, इन्हें लागू करना आसान और लागत प्रभावी है। इसके अलावा, डायनामिक रेंज उपयोगकर्ता है प्रोग्राम करने योग्य जो उपयोगकर्ता को आवश्यक सीमा को इष्टतम रूप से और एक साथ तय करने में सहायता करता है संवेदनशीलता और फ्रेम दर जैसे अन्य प्रदर्शन मापदंडों पर नियंत्रण रखें। प्रस्तावित तकनीकों द्वारा प्रदान की गई लचीलेपन को कम रोशनी में भी शामिल करना चाहिए सेंसिंग एप्लिकेशन सीधे और सहज हैं।

पहले प्रोटोटाइप के लिए अंतर्निहित दृष्टिकोण इष्टतम के लिए दो-तरफ़ा दृष्टिकोण है प्रदर्शन। पहला तरीका सिग्नल के शुरुआती चरण में सिग्नल गेन को बढ़ाना है ज़ंजीर। इससे बाद में दिखाई देने वाले शोर स्रोत आउटपुट पर कम ध्यान देने योग्य हो जाते हैं।

दूसरी विधि शोर तल को ही कम करना है। सिग्नल लाभ वृद्धि के लिए, प्रस्तावित पिक्सेल आर्किटेक्चर समय-समय पर उपयोगकर्ता-प्रोग्राम योग्य रूपांतरण लाभ मॉड्यूलेशन प्राप्त करता है इन-पिक्सेल स्रोत अनुयायी के गेट-ब्लक कैपेसिटेंस को अलग-अलग करना। अमल करना

इस तकनीक में, स्रोत अनुयायी को पिक्सेल के भाग के लिए एमओएस कैपेसिटर के रूप में पुनः कॉन्फ़िगर किया जाता है कार्यवाही। प्रस्तावित पिक्सेल की 64×64 सरणी वाला एक प्रोटोटाइप सेंसर रहा है ऑपरेशन को सत्यापित करने के लिए AMS $0.35 \mu\text{m}$, 3.3 V CMOS तकनीक में निर्मित। 10 माइक्रोन पिच पिक्सेल में 20.25% भरण कारक है। पिक्सेल मानक एकीकृत प्रदान करने में सक्षम है उच्च रोशनी में फोटो-सिग्नल और कम रोशनी में प्रवर्धित सिग्नल जिसके परिणामस्वरूप होता है आउटपुट के संयोजन के बाद 18 डीबी गतिशील रेंज वृद्धि। केवल एक अतिरिक्त इसे प्राप्त करने के लिए मानक 4T पिक्सेल की तुलना में NMOS ट्रांजिस्टर का उपयोग पिक्सेल में किया जाता है वृद्धि। इमेजर द्वारा खपत की गई बिजली 3.55 mW है। शोर में कमी के लिए, इन-पिक्सेल स्रोत अनुयायी के कम आवृत्ति शोर की पहचान की जाती है एक बड़ी बाधा के रूप में। पहले उल्लिखित वास्तुकला को संशोधित करके पुनः उपयोग किया जाता है $1/f$ शोर में कमी और उच्च रूपांतरण लाभ प्राप्त करने का समय। $1/f$ शोर कम हो जाता है समय-समय पर कमी और व्युत्क्रम के बीच इन-पिक्सेल स्रोत अनुयायी को स्विच करना।

स्रोत अनुयायी को एमओएस संधारित्र में पुनः कॉन्फ़िगर करके कमी की स्थिति प्राप्त की जाती है सोर्स-ड्रेन टर्मिनल को नियंत्रित करके चैनल को खराब करना। जैसा कि ऊपर बताया गया है, इन-पिक्सेल स्रोत फ़ॉलोअर का राज्य परिवर्तन भी रूपांतरण लाभ को बढ़ाता है। प्रयोगात्मक सत्यापन आवृत्ति में एक पिक्सेल के आउटपुट पर मापा गया एकीकृत शोर दिखाता है 128 हर्ट्ज से 50 किलोहर्ट्ज बैंड को बिना स्विच किए $728 \mu\text{Vrms}$ होना चाहिए। 4 की स्विचिंग आवृत्ति पर मेगाहर्ट्ज, आउटपुट एकीकृत शोर स्विचिंग के बाद $306 \mu\text{Vrms}$ तक कम हो जाता है जिसके परिणामस्वरूप 7.5 डीबी होता है कमी। फोटॉन स्थानांतरण की सहायता से गणना किए गए इलेक्ट्रॉनों में इनपुट संदर्भित शोर वक्र विधि स्विचिंग लागू करने के बाद $26e\text{-rms}$ से $7.3e\text{-rms}$ तक की कमी दिखाती है। कब दोनों, स्विचिंग और रूपांतरण लाभ वृद्धि को लागू किया जाता है, इनपुट संदर्भित शोर है $398 \mu\text{V/e-}$ के उन्नत रूपांतरण लाभ के साथ इसे घटाकर $2.3e\text{-rms}$ कर दिया गया।

CMOS प्रौद्योगिकी में अधिकांश एचडीआर तकनीकों को ऑन-चिप या ऑफ-चिप पुनर्निर्माण की आवश्यकता होती है एकाधिक लाभ सेटिंग्स या एकाधिक एकीकरण समय पर ली गई छवियों की। वैकल्पिक रूप से, एक वनशॉट एचडीआर सेंसर जो सीधे एचडीआर दृश्य को कैप्चर करता है, उसे किसी पुनर्निर्माण की आवश्यकता नहीं है और है अत्यधिक पसंदीदा। इस थीसिस में प्रस्तावित अगली तकनीक कम रोशनी की गतिशीलता को बढ़ाती है रेंज है और इसमें वन शॉट एचडीआर रिसर्पॉन्स है।

तकनीक पल्स चौड़ाई मॉड्यूलेशन को नियोजित करती है और एक सुविधाजनक, उपयोगकर्ता-प्रोग्राम योग्य विधि प्रदान करने के लिए एक संशोधित गिनती योजना परिवेशीय प्रकाश के आधार पर गतिशील रेंज और संवेदनशीलता को नियंत्रित करना। पीडब्लूएम तकनीक एक समान एसएनआर प्रदान करती है जो फोटो-डायोड करंट से स्वतंत्र है। यह पहलू इसका उपयोग विशेष रूप से कम रोशनी वाले क्षेत्र में इमेजिंग को बेहतर बनाने के लिए किया जाता है। एक प्रोटोटाइप सेंसर मानक 3T-पिक्सेल की 128×128 सरणी से बना, एक क्षेत्र-कुशल कॉलम सर्किटरी डबल सैंपलिंग ऑपरेशन के साथ, एक 10-बिट मेमोरी और एक संशोधित चिप लेवल काउंटर है एल्गोरिदम का परीक्षण करने के लिए निर्मित किया गया है। परीक्षण चिप का निर्माण 350 एनएम एएमएस में किया गया है प्रक्रिया। प्राप्त अधिकतम गतिशील रेंज 95 डीबी और बिजली की खपत है 36 एफपीएस पर मापा गया 3.3 वी बिजली आपूर्ति के साथ 8.4 मेगावाट है।

Table of Contents

	Page
List of Figures	xi
List of Tables	xvii
Chapter 1 Introduction	1
1.1 Dynamic Range	3
1.2 Solid-state imaging devices	5
1.3 Thesis motivation	11
1.4 Thesis organization	14
Chapter 2 High dynamic range CMOS image Sensors	16
2.1 Introduction	16
2.2 Dynamic range enhancement in high light	17
2.3 Dynamic range enhancement in low light	21
2.3.1 Temporal noise sources	21

2.3.2	Signal multiplication and gain enhancement	27
2.4	Low light DR: Challenges with other KPIs	30
2.5	Conclusions	34
Chapter 3 An HDR CIS using In-pixel Gain Enhancement and Noise Reduction		36
3.1	Introduction	36
3.2	Gain enhancement employing in-pixel capacitive variation using a re-configurable source follower	38
3.2.1	Basic operating principle	39
3.2.2	Measurement Results: Part I	43
3.3	Combining gain enhancement with in-pixel noise reduction using switched biasing	49
3.3.1	Theory and operation	50
3.3.1.1	Noise reduction using switched biasing	50
3.3.1.2	Pixel operation for switched biasing mode	54
3.3.1.3	Noise Analysis: Conversion Gain Enhancement	60
3.3.2	Measurement Results: Part II	65
3.3.3	Comparison and Discussion	80
3.4	Conclusions	81
Chapter 4 PWM based CMOS image sensor with programmable low light DR enhancement		84

4.1	Introduction	84
4.2	Theory	86
4.2.1	PWM operating principle in CIS	86
4.2.2	Chip architecture and detailed operation	89
4.2.3	Dynamic range enhancement: quantitative analysis	95
4.2.4	Design and Simulation	97
4.3	Measurement	101
4.3.1	Test Setup	101
4.3.2	Experimental Results	102
4.3.3	Performance comparison and discussion	111
4.4	Conclusions	114
Chapter 5 Conclusions and Future Scope		116
5.1	Prototype 1: High CG Low Noise CMOS Image Sensor	116
5.1.1	Conclusion	116
5.1.2	Future directions	118
5.2	Prototype 2: PWM based programmable DR CMOS image sensor	120
5.2.1	Conclusion	120
5.2.2	Future directions	121
Bibliography		123

List of Figures

1.1	A visual comparison between the dynamic range of the human eye and that of image sensors	2
1.2	Photo-transfer characteristics of a CMOS imager showing the dynamic range and its limits	4
1.3	Block diagram of an interline transfer CCD image sensor	6
1.4	Block diagram of a CMOS image sensor with a pixel array of 3T APS . . .	8
1.5	(a) Transient voltage at the photodiode node of the pixel in reset and integration modes, and (b) Images captured by a 3T pixel sensor at different exposure times in the characterization lab.	10
2.1	A representation of the sensor output of various HDR techniques in comparison to the standard sensor output of Fig. 1.2. The plots are not drawn to scale and are for general representation.	18
2.2	Noise sources contributed by the CIS signal chain which limit imaging in low light environment	22

2.3	Dangling bond in the $Si - SiO_2$ interface which create traps resulting in capture and emission of channel charge carriers	25
2.4	Pulse width modulation in CMOS image sensors. The width of the pulse at the comparator output, V_{OUT} represents the amount of light on the photodetector	29
2.5	Photo transfer characteristics of CIS showing important parameters and noise vs input illumination plot	31
3.1	Proposed 5-transistor pixel and column circuit	40
3.2	Timing Diagram	41
3.3	A pictorial representation showing variation in the depletion capacitance of transistor MS when the control terminal is switched from V_{DD} (Phase I) to V_{PA} (Phase II)	41
3.4	Chip micrograph and customized test boards	44
3.5	Single pixel layout for the proposed 5T architecture	44
3.6	CRO results of a test pixel. The sampled output is shown for $V_{PA} = 2.5$ V, 2.3 V, 2.1 V, 1.8 V and 1.6 V at a fixed illumination level of 3 lux	45
3.7	Measured pixel conversion gain for different modes of operation	46
3.8	Photo-electric conversion characteristics	47
3.9	Measured pixel conversion gain for different modes of operation	48

3.10	Sample Images at a fixed illumination of 3 lux and integration time of 300 μ s (a) Without amplification (b) $V_{PA} = 2.4$ V (c) $V_{PA} = 2.0$ V (d) $V_{PA} = 1.6$ V (e) Reconstructed Image	49
3.11	Comparison of drain current fluctuations between a continuously biased and switched biased MOSFET [1]	52
3.12	CIS and 5T pixel architecture. The circuit enclosed in the dashed line is the pixel. Arrows display the paths that are switched alternately to create depletion and inversion using switched biasing	55
3.13	Timing diagram. Switched biasing phase includes four switching cycles . . .	55
3.14	The in-pixel circuit schematics for the switched biasing implementation during signal readout. The pixel is switched between depletion and inversion at a frequency f_{SW}	56
3.15	Energy band diagram of SF in depletion and inversion.	57
3.16	Small signal model of in-pixel source follower. The gate, drain and source of SF are marked.	62
3.17	Measurement Setup for low frequency noise measurement and image acquisition	66
3.18	Detailed schematic of 1/f noise measurement using spectrum analyser . . .	68
3.19	Measured PSD at the output of the pixel for the case of conventional readout and varying value of V_{PA}	69

3.20 Comparison of PSD at the output of the pixel with and without switched biasing	69
3.21 Photon transfer curve of the sensor for (a) Conventional Readout (V_{PA} cut off from pixel) (b) Switched biasing ($V_{PA} = 3.3$) V (c) Combination of switched biasing and capacitance modulation ($V_{PA} = 1.6$ V). (d) The change in input referred noise due to the three operation schemes.	70
3.22 Input referred noise electron density shown in the frequency domain	73
3.23 Sample dark images captured from the prototype sensor at a fixed integration time of $7\mu s$. The frame rate is 196 fps. The top row displays images with increasing conversion gain enhancement without switched biasing: (a) conventional readout, (b) $V_{PA} = 2.6$ V, (c) $V_{PA} = 2$, (d) $V_{PA} = 1.6$ V. The bottom row shows the same images after noise reduction due to switched biasing: (e) With no capacitance modulation (f) $V_{PA} = 2.6$ V, (g) $V_{PA} = 2$, (h) $V_{PA} = 1.6$ V.	73
3.24 A comparison of output noise using histogram plot: (a) Conventional Readout vs switched biasing applied. With and without switched biasing for (b) $V_{PA} = 2.6$ V, (c) $V_{PA} = 2$ V, (d) $V_{PA} = 1.6$ V. X-axis is not constant for clarity of the figure.	75
3.25 Increase in σ with capacitive modulation and the suppression in σ due to switched biasing	76

3.26	Sample images from the prototype sensor to display the technique on an object. Images were taken at a fixed integration time of $200\ \mu\text{s}$ and a frame rate of 55 fps with a lens of f-number 1.4. (a) Raw image with conventional readout. (b) dark frame with conventional readout. (c) Average of 250 frames of conventional readout to suppress thermal noise. (d) Average of 250 dark frames. (e) Average of 250 frames taken with switched biasing (no capacitance modulation) to suppress low frequency noise. (f) Average of 250 dark frames with switched biasing. (g) Dark frame shown in (f) subtracted from image shown in (e) to eliminate FPN due to column, pixel offset variations. (h) Above procedure repeated with switching and CG enhancement for $V_{PA} = 1.6\ \text{V}$	77
4.1	A representative structure of the 3T pixel and column used to implement the low light capture algorithm	87
4.2	Conventional and desired DR enhancement in a PWM sensor by varying the counter frequency.	87
4.3	Block diagram of the prototype sensor	90
4.4	Architecture of the sensor for programmable low light DR enhancement using PWM in CIS	92
4.5	Timing diagram	94
4.6	Schematic of the comparator	98

4.7	Simulation results (worst case) of the comparator to show the delay time at the output.	99
4.8	Simulated transfer characteristics of one pixel and column readout of the sensor for different HDR modes: Output DN vs input photocurrent	100
4.9	Chip micrograph and layout	102
4.10	Image acquisition setup	103
4.11	Schematic diagram of measurement setup	104
4.12	Photo-transfer characteristics showing the 10-bit output of the prototype sensor with varying input illumination. The digital output has been shown for multiple modes of the algorithm in low, moderate and high light regime	104
4.13	Relationship of DR and sensitivity with respect to user input 'n'	105
4.14	Measured SNR plot for different values of 'n'	107
4.15	SNR dependence on comparator bias current	107
4.16	Effect of comparator bias current on total power consumption of sensor. The SNR and power are measure under complete dark and in the setting s='512' and n='8' with a frame rate of 36 fps	108
4.17	CRO results probed at the node CLK_COUNTER (input clock to the counter) shown in the left. The frequency division according to selected mode defined by 'n' is displayed. Sample images corresponding to each mode and in different light regimes shown in the right.	110

List of Tables

2.1	Qualitative overview of low light HDR techniques in CMOS imagers and their effect on area, power and cost	33
3.1	Performance Summary for the CG enhancement sensor	50
3.2	Parameter Calculation for PTC in Fig. 3.21(c)	71
3.3	Sensor characteristics	74
3.4	Comparison with other state-of-art 1/f noise reduction and pixel/column gain enhancement techniques	79
4.1	Selection logic output and clock division	93
4.2	Performance comparison Table	112