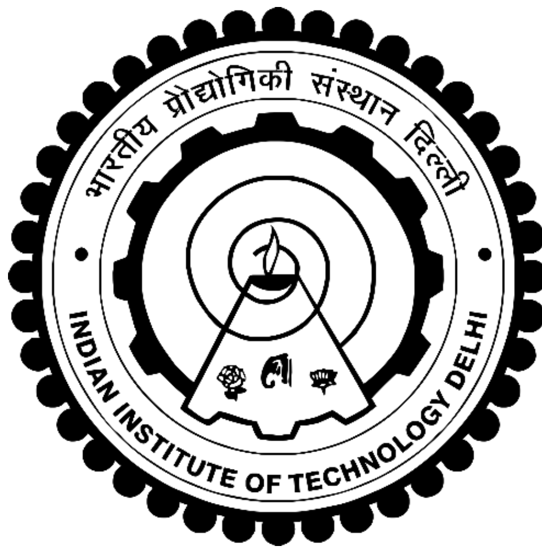
BISTABLE MEMS/NEMS BASED SWITCHES FOR RUGGED EMBEDDED APPLICATIONS: NON-VOLATILE MEMORY

Dhairya Singh Arya



CENTRE FOR APPLIED RESEARCH IN ELECTRONICS (CARE)

INDIAN INSTITUTE OF TECHNOLOGY, NEW DELHI

OCTOBER-2022

© Indian Institute of Technology Delhi (IITD), New Delhi 2022

BISTABLE MEMS/NEMS BASED SWITCHES FOR RUGGED EMBEDDED APPLICATIONS: NON-VOLATILE MEMORY

By

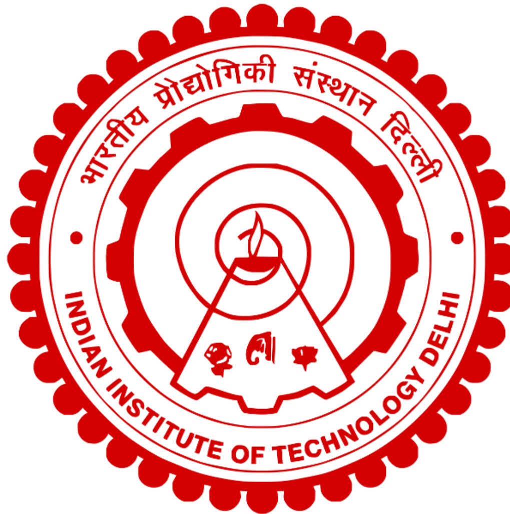
Dhairya Singh Arya

Centre for Applied Research in Electronics (CARE)

Submitted

in fulfillment of the requirements of the degree of Doctor of Philosophy

to the



INDIAN INSTITUTE OF TECHNOLOGY, NEW DELHI

OCTOBER-2022

Dedicated to Supreme Lord Shiva …

Certificate

This is to certify that the thesis entitled "***Bistable MEMS/NEMS based Switches for Rugged Embedded Applications: Non-Volatile Memory***" being submitted by ***Dhairya Singh Arya*** to the Centre for Applied Research in Electronics(CARE), Indian Institute of Technology Delhi for the award of degree of '***Doctor of Philosophy***' is a record of bonafide work carried out by him. He has worked under my supervision and guidance, and has fulfilled the requirement for the submission of this thesis, which in my opinion has reached the requisite standard. The results contained in this work has not been submitted, in part or full, to any other University or Institution for the award of any degree or diploma.

Prof. Pushpapraj Singh
Centre for Applied Research in Electronics (CARE)
Indian Institute of Technology Delhi
Hauz Khas, New Delhi-110016

Acknowledgements

Ph.D. has been a truly life-changing experience for me, and it would not have been possible to do without the support and guidance that I received from many people. This thesis represents not only my work at the keyboard and lab experiments, but also presents the lessons learned and experience gained during my Ph.D. journey. I have encountered with remarkable individuals in this journey, whom I also wish to acknowledge. First and foremost, I wholeheartedly thank my supervisors, ***Prof Pushpapraj Singh*** for his continuous support, guidance, encouragement, and suggestions in executing this research work. I express my sincere gratitude to ***Prof Arun Kumar***, Head of the Centre for Applied Research in Electronics (CARE) at IIT Delhi, for providing the constructive environment to carry out my research at the centre. Thanks to my SRC members ***Prof Bhaskar Mitra***, and ***Prof Ankur Gupta***, for their valuable comments and remarks.

Further, I extend my sincere thanks to all the faculty members of the Centre for Applied Research in Electronics (CARE), IIT Delhi. I also owe a debt of gratitude to ***Prof Sameresh Das***, for being constant source of support and encouragement. A special thanks to the faculties managing the facilities in Nanoscale Research Facility and Central Research Facility at IIT Delhi for providing exposure to world-class lab facilities during my research. No research is complete without intellectual debates, and here I take this opportunity to thank all my lab members, colleagues, and friends for their support and their company that I was fortunate to be a part of; I thank all my extended family, ***Sushil Kumar***, ***Mujeeb Yousuf***, ***Manu Garg***, ***Alka Jakhar***, ***Veerendra Dhyani***, ***Sumit Sharma***, ***John Wellington J***, ***Akhil Ramesh***, ***Khanjan Joshi***, ***Suprovat Ghosh***, ***Priyanka Dwivedi***, ***Udit Jain, Nikhil Chourasiya, Akshay Moudgil***, ***Wasi Uddin***, ***Shubham Bhatt***, ***Biswajit Khan***, ***Pranjal Mandhaniya***, ***Niharika Narang, Ankesh Wasnik, Pranav Shrivastava, Nitish Kumar*** for the fun, fights, laughter, and the inspiration they provide me during my tough times. Lastly,

I am deeply thankful to my family, and they are the reason that I am getting my Ph.D. They inspire me, push me and love me unconditionally. I am grateful to my sister ***Dr Aditi*** for her moral support, and to my brother ***Pratham*** for his affection towards me and the emotional support that rejoiced me with his smiling faces.

Dhairya Singh Arya

Thesis Abstract

The thesis focuses on the design and fabrication of bistable MEMS-based metallic switches in context to Non-Volatile Memory (NVM) and power gating applications. The bistable MEMS switches are analogous to conventional push-to-on electrical switches, which does not require biasing or voltage to hold its state. The bistable switches provide energy-efficient solutions to the embedded systems as they do not require any voltage for holding the On-state.

The objective of the thesis is to demonstrate the feasibility of non-volatile data storage based on micro-electro-mechanical systems (MEMS) for rugged embedded applications. This work introduces a MEMS cantilever and a beam structure having two stable mechanical states.

Current mainstream NVM data storage technologies suffer from poor data retention when exposed to harsh environments (high temperature). Along with current mainstream FLASH technology, other emerging NVMs typically include resistive Random Access Memory (RAM) i.e. R-RAM, magnetic RAM (M RAM), phase-change RAM (PCRAM) and ferroelectric RAM (FeRAM). However, all these NVMs use different types of storage media (charge, resistive, ferroelectric and magnetic based) to preserve the information and exposure to harsh environment severely degrades the retention in storage media.

To address the aforementioned issues in emerging NVMs', micro/nano-mechanical systems based NVM were reported. These mechanical memories precisely manoeuvre the van der Walls force to switch between the logic states. However, they lack a reliable de-actuation mechanism. Thereafter the single side SET and RESET method based on vibration was tried in MEMS-NVM, but this method lacks proper experimental validation and underlying physics. Above all, the thesis introduces a new class of bistable memory, i.e. MEM-Z NVM. The MEM-Z NVM employs a more reliable piezoelectric deactuation.

The thesis describes more than Moore's next-generation nanoelectromechanical system-based flash memory (NEMS-Flash). The proposed structure is more than Moore's in the sense of higher bit density per transistor. The approach for multibit storage is realized by altering the threshold voltage of a transistor to different levels by using switch controlled floating gate.

Further the thesis demonstrates a 1 kB high-speed prototype and scalable Nanoelectromechanical Read-Only-Memory (NEMS-ROM). The fabrication of the NEMS-ROM involves the process of solid diffusion for the formation of sub-nanometer coarse gap. The proposed NEMS-ROM is insensitive to thermal fluctuations (-100 ºC to +350 ºC). NEMS-ROM core is suitable for storing the micro-operations for high-speed rugged embedded applications.

The last chapter demonstrates the application aspects of the bistable MEMS systems, i.e. NVMs'. The bistable switches offer energy efficient solutions to the embedded systems as these bistable switches do not require any voltage for holding the ON-state.

थीसिस सार

थीसिस गैर-वाष्पशील मेमोरी (एनवीएम) और पावर गेटिंग अनुप्रयोगों के संदर्भ में बाईस्टेबल एमईएमएस-आधारित धातु स्विच के डिजाइन और निर्माण पर केंद्रित है। बाईस्टेबल एमईएमएस स्विच पारंपरिक पुश-टू-ऑन इलेक्ट्रिकल स्विच के अनुरूप होते हैं, जिन्हें अपनी स्थिति को बनाए रखने के लिए बायसिंग या वोल्टेज की आवश्यकता नहीं होती है। बाईस्टेबल स्विच एम्बेडेड सिस्टम को ऊर्जा-कुशल समाधान प्रदान करते हैं क्योंकि उन्हें ऑन-स्टेट रखने के लिए किसी वोल्टेज की आवश्यकता नहीं होती है।

थीसिस का उद्देश्य उच्च तापमान सम्बंधित एम्बेडेड अनुप्रयोगों के लिए माइक्रो-इलेक्ट्रो-मैकेनिकल सिस्टम (एमईएमएस) पर आधारित गैर-वाष्पशील डेटा भंडारण की व्यवहार्यता का प्रदर्शन करना है। यह काम एक एमईएमएस कैंटिलीवर और दो स्थिर स्थिति वाले बीम संरचना का परिचय देता है। कठोर वातावरण (उच्च तापमान) के संपर्क में आने पर वर्तमान मुख्यधारा की एनवीएम डेटा स्टोरेज प्रौद्योगिकियां खराब डेटा प्रतिधारण से ग्रस्त हैं। वर्तमान मुख्यधारा की फ्लैश तकनीक के साथ, अन्य उभरते हुए एनवीएम में आमतौर पर रेसिस्टिव रैंडम एक्सेस मेमोरी (रैम) यानी आर-रैम, मैग्नेटिक रैम (एम रैम), फेज-चेंज रैम (पीसीआरएएम) और फेरोइलेक्ट्रिक रैम (एफईआरएएम) शामिल हैं। हालाँकि, ये सभी एनवीएम सूचना को संरक्षित करने के लिए विभिन्न प्रकार के स्टोरेज मीडिया (चार्ज, रेसिस्टिव, फेरोइलेक्ट्रिक और मैग्नेटिक आधारित) का उपयोग करते हैं और कठोर वातावरण के संपर्क में आने से स्टोरेज मीडिया में रिटेंशन गंभीर रूप से कम हो जाता है।

उभरते हुए एनवीएम में उपरोक्त मुद्दों को हल करने के लिए, माइक्रो/नैनो-मैकेनिकल सिस्टम आधारित एनवीएम की सूचना दी गई थी। ये यांत्रिक वैन–डेर–वॉल्स बल को तर्क अवस्थाओं के बीच स्विच करने के लिए सटीक रूप से निर्धारण करती हैं। हालांकि, इनमें एक विश्वसनीय डी-एक्ट्यूएशन प्राकरिया का अभाव है। इसके बाद एमईएमएस-एनवीएम में कंपन पर आधारित एक तरफ सेट और रीसेट पद्धति का प्रयास किया गया, लेकिन इस पद्धति में उचित प्रयोगात्मक सत्यापन और अंतर्निहित भौतिकी का अभाव है।

इन सबसे ऊपर, थीसिस ने बाईस्टेबल मेमोरी, यानी एमईएम-जेड एनवीएम का एक नया वर्ग पेश किया। एमईएम-जेड एनवीएम एक अधिक विश्वसनीय पीजोइलेक्ट्रिक क्रिया का उपयोग करता है। थीसिस मूर की अगली पीढ़ी से आगे, नैनोइलेक्ट्रोमैकेनिकल सिस्टम-आधारित फ्लैश मेमोरी (एनईएमएस-फ्लैश) का वर्णन करती है। एनईएमएस-फ्लैश फ्लैश–रैम की तुलना में प्रति ट्रांजिस्टर ज्यदा बिट घनत्व प्रदान करती है। मल्टीबिट स्टोरेज के दृष्टिकोण से देखा जाए तो, स्विच नियंत्रित फ्लोटिंग गेट का उपयोग करके ट्रांजिस्टर के थ्रेसहोल्ड वोल्टेज को विभिन्न स्तरों में बदलकर ज्यादा डाटा स्टोर किआ जा सकता है।

इसके अलावा थीसिस एक 1 केबी हाई-स्पीड प्रोटोटाइप और स्केलेबल नैनोइलेक्ट्रोमैकेनिकल रीड-ओनली-मेमोरी (एनईएमएस-रोम) को प्रदर्शित करता है। एनईएमएस-रोम के लिये नैनोमीटर अंतराल के निर्माण के लिए ठोस–प्रसार की प्रक्रिया शामिल है। प्रस्तावित एनईएमएस-रोम थर्मल उतार-चढ़ाव (-100 ℃ से +350 ℃) के प्रति असंवेदनशील है। एनईएमएस-रोम कोर हाई-स्पीड रग्ड एम्बेडेड अनुप्रयोगों के लिए माइक्रो-ऑपरेशंस को स्टोर करने के लिए उपयुक्त है।

अंतिम अध्याय बाईस्टेबल एमईएमएस सिस्टम, यानी एनवीएम के अनुप्रयोग पहलुओं को प्रदर्शित करता है। बाईस्टेबल स्विच एम्बेडेड सिस्टम को ऊर्जा कुशल समाधान प्रदान करते हैं क्योंकि इन बिस्टेबल स्विच को ऑन-स्टेट रखने के लिए किसी वोल्टेज की आवश्यकता नहीं होती है।

Table of Contents

Certificate i

Acknowledgement ii

Thesis Abstract iv

List of Figures x

List of Tables xiii

1. **Introduction** 1

1.1 Types of Memories 1

1.1.1 Flash Memory 1

1.1.2 FRAM (Ferroelectric Random-Access Memory) 4

1.1.3 MRAM (Magnetoresistive Random-Access Memory) 7

1.1.4 PCM (Phase change memory) 9

1.1.5 RRAM (Resistive Random-access memory) 12

1.2 Mechanical Memories 14

1.2.1 MEMS based Non-Volatile Memory 15

1.2.2 Standard Cantilever beam NVM 17

1.2.3 Teeter-Totter NVM 20

1.2.4 Anchor Free MEMS NVM 22

1.2.5 Vibrational RESET Based MEMS NVM 25

1.3 Thesis Motivation and Objective 28

Bibliography 31

2. **Precision Mechanical Memories** 35

2.1 NEMS-Flash NVM Device for High-Temperature Multibit Data Storage 35

2.1.1 Background 35

2.1.2 Charge Estimation on Floating Gate 39

2.1.3 Conclusion 45

2.2 NEMS-ROM for High-Speed and Rugged Embedded Applications 46

2.2.1 Overview 46

2.2.2 Fabrication of NEMS-ROM 48

2.2.3 Memory Design and Programming 49

2.2.4 Results and Discussion 52

2.2.5 Conclusion 54

Bibliography 55

3. **Piezoelectric Deactuation Based Bistable MEMS Switch: MEM-Z NVM** 60

3.1 Introduction 60

3.2 MEM-Z NVM ... 63
3.3 Bistable MEM-Z NVM Design and Fabrication ... 65
3.4 Results and Discussion ... 68
3.5 Conclusion ... 72
Bibliography ... 73
4. **Bistable MEMS-NVM: Reducing Energy and Dynamism in DRAM** ... 76
4.1 Hold-Bias free MEM Power Gate ... 76
4.1.1 Overview ... 76
4.1.2 Bistable MEM Power Gate Design ... 77
4.1.3 Fabrication ... 79
4.1.4 Results and Discussion ... 81
4.1.5 Conclusion ... 85
4.2 Reducing Dynamism in DRAM ... 85
4.2.1 Background ... 86
4.2.2 Designing of MEMS Sleep Transistor ... 87
4.2.3 Fabrication of MEMS Sleep Transistor ... 92
4.2.4 Measurements and Discussion ... 93
4.2.5 Conclusion ... 99
Bibliography ... 101
5. **Conclusion and Future Outlook** ... 103
5.1 Summary ... 103
5.2 Future Outlook ... 104
List of Publications ... 106
Journals ... 106
Conferences ... 107
Patent ... 109
Authors Biography ... 110

List of Figures

Fig 1.1 (a) Cross section view (b) Symbol representation of the floating-gate transistor 2

Fig 1.2 Circuit schematic of the Flash NVM cell, (b) I-V characteristics for the programmed and erased cell state 2

Fig 1.3 Atomic structure of the PZT, or lead zirconate titanate (Pb[Zr(x)Ti(1-x)]O3) (a) Atom at the centre position (i.e. when no external electric field applied) (b) Atom at the up polarisation (i.e. when the field is such that the atom shifts to top)........ 5

Fig 1.4 FRAM memory cell integrated with active element FET and two states on hysteresis loop of the ferroelectric material. 6

Fig 1.5 Basic architecture for the MRAM cell with two different storage states........ 7

Fig 1.6 (a) Low resistive path (i.e. both having same moment direction, bit '1') (b) Highly resistive path, (i.e. both having opposite moment, bit '0') 8

Fig 1.7 Energy band diagram for '1' or '0' storage bit. 8

Fig 1.8 Basic phase change memory cell........ 10

Fig 1.9 Amorphous and Crystalline state of the Ge2Sb2Te5 (GST). 10

Fig 1.10 SET/RESET operation of the PCM 11

Fig 1.11 Basic RRAM cell architecture........ 13

Fig 1.12 SET/ RESET operation of the RRAM cell........ 13

Fig 1.13 Components of MEMS technology. 15

Fig 1.14 MEMS NVM cell, where B is Bistable bridge, L is lateral electrode and S is substrate....... 16

Fig 1.15 Standard cantilever NVM architecture........ 18

Fig 1.16 Basic architecture of the Teeter-totter based Non-Volatile Memory........ 21

Fig 1.17 Bit generation operation of the NVM cell, (a) Storing '1' bit operation (b) Storing '0' bit operation. 22

Fig 1.18 Cross section view of the anchor free MEMS NVM under different operations. 23

Fig 1.19 (a) Top view of the anchor free MEMS NVM (b) Cross section view with the down state and read condition (c) Cross section view with the up-state condition........ 25

Fig 1.20 Basic vibrational RESET MEMS NVM Cell. 26

Fig 1.21 Vibrational RESET with DC voltage pulses on the contact electrode........ 27

Fig 1.22 Memory Operation for the Vibrational RESET based MEMS NVM with DC pulse applied at actuation electrode. 27

Fig 2.1 Non-volatile NEMS-Flash memory cell: Symbol and layout........ 37

Fig 2.2 Working Principle of MEM-FLASH........ 38

Fig 2.3 The theoretically calculated trend for V_{PI} variation with charge loading. 42

Fig 2.4 SEM of the dynamic part of MEM-FLASH (scale bar 1µm). 43

Fig 2.5 Pull-in variation based on charge loading at the contact electrode under vacuum. 44

Fig 2.6 NEMS-ROM cell showing metal (W) bus-line crossbar structure as a single bit element

and its respective fused and unfused states. 47

Fig 2.7 The fabrication flow of the NEMS-ROM cell and the inset at right shows the thermal cycle used in the rapid thermal process (RTP) for initiating the process of solid diffusion. The ramp and hold cycle is preferred to avoid Aluminium coagulation into dots due to surface tension........ 48

Fig 2.8 SEM image of stand-alone NEMS-ROM unit cell indicating bus lines crossbar structure. The inset shows the coarse gap of ~ 30-50 nm post-fabrication and RTP annealing (scale bar 2 µm)......... 49

Fig 2.9 Unfused-state of NEMS-ROM to fused-state using transistor as a switch. The transistor's base is configured with DAQ digital output. The out-pins derive the base of transistors. This simple procedure is used to fuse the NEMS ROM-Cell. 50

Fig 2.10 Exploratory 1 KB NEMS-ROM programmed with binary-coded ASCII of string 'IEEE', where the symbols have their usual meaning. Once the corresponding unit cells are fused, the bit-stream is parallelly retrieved by selecting the corresponding address line. The waveform indicates the retrieved bit-stream. resistance in the temperature band is ~ 67 KΩ. 51

Fig 2.11 The retention test, showing that the state of NEMS-ROM is retained even after several hours and at the broader band of temperature. The inset shows a simulated bit-line voltage versus bit-line current plot indicating wide separation in transresistive states. The resistance in the fused state is inclusive of the resistance contribution from the supply voltage source and the MOS-transistor. 52

Fig 2.12 The current versus voltage plot for the NEMS-ROM unit cell. The unit cell in the unfused state has average resistance of the order of ~ $10^{9,}$ whereas if fused, the order changes to 10^3, indicating transfer of resistance from High to low state. The inset shows the variation in the fused NEMS-ROM unit cell resistance in the temperature band ranging from -100 °C to +350 ºC. The average resistance in the temperature band is ~ 67 KΩ. 53

Fig 3.1 Direct piezoelectric effect.. 62

Fig 3.2 Inverse piezoelectric effect. 62

Fig 3.3 Sort-out image of the prototype bistable MEM-Z element, showing key-parts (image not to scale). 64

Fig 3.4 Operation of the proposed bistable MEM-Z NVM, along with biasing considerations. The state Z_0 is a default state whereas MEM-Z NVM retains the state Z_2 due to adhesive locking of µ-ball and socket. 64

Fig 3.5 The CMOS compatible fabrication flow of bistable MEM-Z NVM. All the processes are carried out at nominal temperature to preserve underlying CMOS circuitry. The controlled and selective blanket etching of AlN is carried out to shape the AlN µ-ball. The top metal is conformally deposited to form anchor points and fix-fix beam. 67

Fig 3.6 The SEM of the fabricated bistable MEM-Z NVM post characterization (scale bar 5 µm). The collar around the µ-socket is fabricated for precise control over to adhesion force. The inset shows probe punctured, vertical sectioned (A'-A) image of the µ-Ball and socket.. 67

Fig 3.7 Sort-out image of the biased AlN µ-ball indicating alteration in the top surface area. The base and the socket are acting as the biasing electrodes when MEM-Z is in state Z_2. The image is not to scale in Z-axis. 70

Fig 3.8 The cyclic capacitance versus voltage (CV) sweep of MEM-Z NVM.On cyclically tracing the gate voltage the capacitance between base and collar does not drops down, indicating the stable state of Z_2. The inset indicates RESET from state Z_2 to Z_0 on the application of RESET-pulse. 71

Fig 4.1 Bistable MEM power gate as sleep transistor in CMOS ICs... 77

Fig 4.2 Summary of the criteria for power gate to be doubly stable. The designing of doubly stable power gate should be such that it falls under yellow shaded region, where the magnitude of F_{ad} is 2 to 5 times higher than F_r. If F_{ad} is too large than F_r, the gate remains in on-state and if F_r is larger than F_{ad}, the power gate is not doubly stable... 79

Fig 4.3 CMOS compatible process flow for the fabrication of bistable MEM power gate. All the deposition process carried out at moderate temperature to preserve underlying CMOS stack. 80

Fig 4.4 Fabricated bistable MEM power gate as sleep transistor (scale bar 2 µm). The Dints on the channel far end is intentionally fabricated so as to have precise control over to adhesion force. The circular inset to figure shows power gate in both the stable states... 80

Fig 4.5 Simulated thermal budget for proposed bistable MEM power gate. The graph shows the maximum temperature reached for the corresponding current density. Inset indicates the maximum temperature at dints surface in contact with drain electrode. 82

Fig 4.6 Simulated total energy component versus time for $V_{GS} = 5$ V. The average energy consumption in bistable power gate is lesser than its conventional counterpart due to no hold bias requirement in on-state. 82

Fig 4.7 The cyclic E-Test for MEM power gate, depicting bi-stability. The current does not drop from the set limiting compliance (1 µA) to noise level, even if V_{GS} is traced back to zero. The power gate has pull-in voltage of ~5 Volts, which is in line with the supply rail convention for most of the digital circuits. 83

Fig 4.8 The toggling of MEM power gate from on-state to off-state on application of RZ-pulse to control gate for ~0.5 ms duration. The frequency of applied RZ-pulse matches with the mechanical frequency of power gate resulting in beam excitation and thus the deactuation to off-state. 84

Fig 4.9 (a) The bistable MEMS power gate as sleep-transistor integrated with digital circuit block. (b) The electrical equivalent of MEMS sleep-transistor as voltage control current source. 87

Fig 4.10 Design criteria for the MEMS sleep-transistor to be bistable. The designing is such that it falls within highlighted regime, where the magnitude of F_r is 2 to 5 times lesser than $F_{ad.}$ 91

Fig 4.11 low temperature, CMOS compatible process-flow for the bistable MEMS sleep-transistor to preserve integrated CMOS stack. 92

Fig 4.12 Bistable MEMS sleep-transistor in both the stable modes (active/sleep). The notches on the cantilever end is designed to precisely control the force of adhesion (scale bar 2 µm and colors are illustrative). 93

Fig 4.13 Finite Elemental analysis (FEM) analysis for the thermal budget in MEMS sleep-transistor which corresponds to maximum current density (0.5 mA/µm^2). The highest temperature is of ~85 ºC at the notches-end complying with the set thermal budget for the digital CMOS circuits. 94

Fig 4.14 Thermal budget for the bistable MEMS sleep-transistor. Inset shows the maximum temperature at the notch surface in active mode. 94

Fig 4.15 Total energy versus time for gate to source voltage of 5 V. The time average energy used by bistable MEMS sleep-transistor is less if compared to the conventional sleep-transistor, this is due to zero hold voltage in active mode. 95

Fig 4.16 Exploratory 1KB DRAM cell (UMC-28 nm) integrated with MEMS sleep transistor in global mode (the symbols have their usual meaning) for CAD simulation. 96

Fig 4.17 The node discharging versus time. The MEMS sleep-transistor increases the distributed resistance in sleep mode and thus the discharging time. 97

Fig 4.18 The cyclic test for MEMS sleep-transistor. Even if V_{GS} is cyclically reduced to zero, the drain current does not gets drop to noise level from the limiting compliance. The inset indicates toggling from active mode to sleep mode with the applied RZ-pulsating voltage at gate terminal. 98

Fig 4.19 The bias and timing considerations to program the control gate for cyclic test. The bistable sleep-transistor shows more than 10^5 cycles of operation in vacuum environment without failure. 99

List of Tables

Table 1.1: The different possible applications explored in the field of MEMS devices 16

Table 1.2: Operating conditions for the anchor free MEMS NVM 24

Table 3.1: Bistable MEM-Z forces in consideration 69

Table 3.2: Bistable MEM-Z biasing considerations 71

Table 4.1: Bistable MEM power gate parameters 81

Table 4.2: Bistable MEM power gate performance metrics 85

Table 4.3: Bistable MEMS sleep-transistor parameters 97

Table 4.4: Bistable MEMS sleep-transistor performance parameters 98