CAPACITOR-DIODE CELL BASED FIFTH-ORDER BOOST DC-DC CONVERTERS: TOPOLOGICAL EVOLUTION AND CONTROL ASPECTS

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MAY 2022

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by

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Department of Electrical Engineering

Submitted

in fulfilment of the requirements of the degree of Doctor of Philosophy

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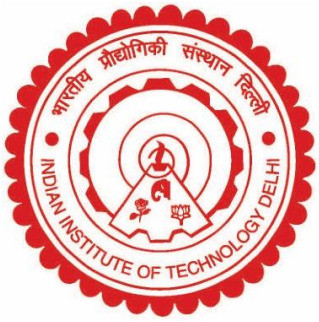

INDIAN INSTITUTE OF TECHNOLOGY DELHI

MAY 2022

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CERTIFICATE

This is to certify that the thesis entitled **"Capacitor-Diode Cell Based Fifth-order Boost DC-DC Converters: Topological Evolution and Control Aspects"** being submitted by **Mr. Priyabrata Shaw** in fulfillment of the requirements for the degree of **Doctor of Philosophy** in the Department Electrical Engineering of Indian Institute of Technology Delhi, New Delhi.

Mr. Priyabrata Shaw has worked under my supervision and fulfilled the requirement for submission of the thesis, which to my knowledge reached the requisite standards. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any Degree or Diploma.

Date:

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ACKNOWLEDGEMENTS

It is a proud privilege of mine to extend my heartfelt gratitude to my esteemed supervisor Dr. Mummadi Veerachary, Professor, Department of Electrical Engineering, Indian Institute of Technology Delhi. His determined zeal, commitment towards excellence in work, and extensive vision have been the source of inspiration for me throughout the research period. His support from the preliminary to the concluding level enabled me to develop an understanding of the subject. Despite all the important engagements, he always spared his precious time for me and gave his valuable and informative suggestions. His vast knowledge, innovative ideas, huge experience, constructive criticism, and continuous encouragement consistently enhanced the quality of this research work. It is an honor for me to have been working under his supervision.

I acknowledge my deep sense of gratitude to the members of the doctoral research committee Dr. Anandarup Das, Dr. Shaunak Sen, and Prof. S. Dharmaraja for their valuable suggestions and scrutiny of this work. I am also grateful to Dr. Amit Kumar Jain and Dr. Ramkrishan Maheshwari for their co-operation and help during my research. I would like to take this opportunity to express my sense of gratitude to all faculty members of the Electrical Engineering department especially the PEEMD group for their constant motivation throughout my study at IIT Delhi.

I would also like to extend my gratitude to Mr. Amit Kumar for his support in providing lab equipment and components at all times. I am also thankful to my seniors, friends, and juniors, especially, Mr. Amarendra Reddy, Mr. Vargil Kumar, Mr. Varun Chitrash, Mr. Prasun Mishra, Ms. Jyoti Prakash, Mr. Shrikant Misal, Mr. Nikhil Kumar, Mr. Abhilash Patel, Mr. Punit Kumar,

Mr. Ambuj Sharma, Mr. Rahul Sharma, Ms. Vasudha Khubchandani, Mr. Malay Ranjan Khuntia, Mr. Devesh Malviya, and Mr. Pushpendra Yadav, who have helped me and made my life in IIT Delhi very exciting and a good memory. My heartfelt thanks to all my colleagues in Power Electronics Lab for providing a warm research atmosphere, sharing knowledge, and personal support throughout my study at IIT Delhi.

I would also like to thank Dr. Manas Kumar Jena and Dr. Manoranjan Sahoo for their motivation, encouraging thoughts, and being with me whenever I needed them.

I would like to thank and acknowledge the MHRD, Government of India, for the financial support and continued assistance throughout the course of my studies at the IIT Delhi.

I owe my deepest gratitude to my mother Annapurna Shaw, father Laxman Shaw, and sister Sasmita Shaw, for their love, affection, care, and constant encouragement throughout the research work. Finally, I wish to mention a very special acknowledgment to my elder brother Satyabrata Shaw, for his continuous support and co-operation. I would also like to express my sense of gratitude to my parents-in-law for showing for their support, inspiration, and love in my life.

Last but not the least, I deeply acknowledge the sacrifice and the moral support of my lovely wife ‘Smruti’ throughout my research work and I am also very much thankful to her for the sacrifice she made during this research work, especially during the writing of the thesis.

Priyabrata Shaw

Date: 3rd May 2022 Priyabrata Shaw

ABSTRACT

This thesis investigates the topological evolution of three different fifth-order topologies belonging to a class of boost family exhibiting identical voltage gain. The exhaustive studies are made on the existing fourth-order boost topologies and an attempt is made to evolve fifth-order boost topologies exhibiting identical voltage gain features. With this objective, an additional capacitor-diode cell (CD-cell) is integrated into the fourth-order topologies such that the resultant topologies yield an enhanced voltage gain together with minimal current ripples on either side of the evolved topologies. An exhaustive steady-state and time-domain analysis is established to identify the proposed CD-cell based fifth-order topologies performance features. Enhanced voltage gain features and other steady-state performance aspects of the three proposed topologies are verified through experimental investigations.

To perform the controller designs, an extensive small-signal analysis is established for the three topologies evolved in this thesis. Firstly, the state-space models are formulated and then various transfer functions characterizing the dynamic performance aspects of the three topologies are established. Through this analysis it is also identified that the topologies exhibit minimum and non-minimum phase behaviors. Upon topological evolution and transfer function analysis of the proposed topologies, the controller design aspects are investigated for reliable closed-loop stabilization. A proportional-integral-lead controller (with complex conjugate zeros) belonging to the family of the PID controller is adopted for the closed-loop operation of the proposed topologies. The time and frequency domain specifications are enforced in the controller design methods. To ensure pre-specified closed-loop specifications, the degree of freedom associated with complex conjugate zeros damping adjustment is exercised. In all these controller design

methods, the closed-loop dominant pole placement approach is utilized. In the first design method, the phase margin is used as a constraint to ensure the desired closed-loop stability along with meeting the transient performance requirements. In the second controller design method, the dominance factor criterion is used along with the dominant pole placement technique.

The controllers designed based on dominant pole placement methodology are successful in the closed-loop stabilization of proposed topologies but there is no guarantee that they are sufficiently robust against fluctuations in supply voltage or even under parameter variations. This is because these design methodologies are plant-specific which depends on the operating point. In order to deal with converter parameter variations and fluctuations in the line voltage/load, the controllers are designed after accounting the robustness issues. In this thesis, a contoured robust controller Bode diagram methodology is adopted to design the robust controller. Performance and uncertainty weight functions are defined and later a step-by-step controller design procedure is established. The robustness of the controllers is demonstrated for the three proposed topologies experimentally. Finally, the performance comparison among the proposed topologies is brought out to identify the topology selection for the given specifications.

सार

यह थीसिस तीन अलग-अलग पांचवें क्रम के टोपोलॉजी के टोपोलॉजिकल विकास की जांच करती है समान वोल्टेज लाभ प्रदर्शित करने वाले बूस्ट परिवार के वर्ग से संबंधित है। संपूर्ण अध्ययन मौजूदा चौथे क्रम के बूस्ट टोपोलॉजी पर बनाया गया है और पांचवें क्रम को विकसित करने का प्रयास किया गया है समान वोल्टेज लाभ सुविधाओं को प्रदर्शित करने वाली टोपोलॉजी को बढ़ावा दें। इस उद्देश्य के साथ, एक अतिरिक्त कैपेसिटर-डायोड सेल (सीडी-सेल) को चौथे क्रम की टोपोलॉजी में एकीकृत किया जाता है जैसे कि परिणामी टोपोलॉजीज के दोनों ओर न्यूनतम करंट रिपल्स के साथ एक बढ़ा हुआ वोल्टेज लाभ प्राप्त करते हैं विकसित टोपोलॉजी। एक संपूर्ण स्थिर-अवस्था और समय-क्षेत्र विश्लेषण स्थापित किया गया है प्रस्तावित सीडी-सेल आधारित पांचवें क्रम की टोपोलॉजी प्रदर्शन सुविधाओं की पहचान करें। बढ़ी तीन प्रस्तावित टोपोलॉजी के वोल्टेज लाभ सुविधाएँ और अन्य स्थिर-अवस्था प्रदर्शन पहलू प्रयोगात्मक जांच के माध्यम से सत्यापित किया गया है।

नियंत्रक डिजाइन करने के लिए, एक व्यापक स्माल-सिग्नल विश्लेषण स्थापित किया गया है इस थीसिस में विकसित हुई तीन टोपोलॉजी के लिए। सबसे पहले, स्टेट-स्पेस मॉडल तैयार किए गए हैं और फिर तीन टोपोलॉजी के ट्रांसफर फंक्शन्स पहलुओं की विशेषता वाले विभिन्न स्थानांतरण कार्य स्थापित हैं। इस विश्लेषण के माध्यम से यह भी पता चलता है कि टोपोलॉजी न्यूनतम और गैर-न्यूनतम चरण व्यवहार प्रदर्शित करती है। टोपोलॉजिकल इवोल्यूशन और ट्रांसफर फंक्शन एनालिसिस पर प्रस्तावित टोपोलॉजी, विश्वसनीय बंद-लूप के लिए नियंत्रक डिजाइन पहलुओं की जांच की जाती है स्थिरीकरण एक आनुपातिक-अभिन्न-लीड नियंत्रक (जटिल संयुग्म शून्य के साथ) से संबंधित है PID नियंत्रक के परिवार को प्रस्तावित के बंद-लूप संचालन के लिए अपनाया गया है टोपोलॉजी। नियंत्रक डिज़ाइन में समय और आवृत्ति डोमेन विनिर्देश लागू किए जाते हैं तरीके। पूर्व-निर्दिष्ट क्लोज-लूप विनिर्देशों को सुनिश्चित करने

के लिए, संबंधित स्वतंत्रता की डिग्री जटिल संयुग्म शून्य के साथ भिगोना समायोजन का प्रयोग किया जाता है। इन सभी नियंत्रक डिजाइन विधियों में, क्लोज्ड-लूप प्रमुख पोल प्लेसमेंट दृष्टिकोण का उपयोग किया जाता है। पहले डिजाइन में विधि, चरण मार्जिन को वांछित बंद-लूप स्थिरता सुनिश्चित करने के लिए बाधा के रूप में उपयोग किया जाता है क्षणिक प्रदर्शन आवश्यकताओं को पूरा करने के साथ। दूसरी नियंत्रक डिजाइन विधि में, प्रभुत्व कारक मानदंड का उपयोग प्रमुख पोल प्लेसमेंट तकनीक के साथ किया गया है।

प्रमुख पोल प्लेसमेंट पद्धति के आधार पर डिजाइन किए गए नियंत्रक सफल हैं प्रस्तावित टोपोलॉजी का बंद-लूप स्थिरीकरण लेकिन इसकी कोई गारंटी नहीं है कि वे हैं आपूर्ति वोल्टेज में उतार-चढ़ाव के खिलाफ या यहां तक कि पैरामीटर भिन्नताओं के तहत पर्याप्त रूप से मजबूत। यह ऐसा इसलिए है क्योंकि ये डिजाइन पद्धतियां संयंत्र-विशिष्ट हैं जो ऑपरेटिंग बिंदु पर निर्भर करती हैं। कनवर्टर पैरामीटर विधताओं और लाइन वोल्टेज/लोड में उतार-चढ़ाव से निपटने के लिए, नियंत्रकों को मजबूती के मुद्दों को ध्यान में रखते हुए डिज़ाइन किया गया है। इस थीसिस में, एक समोच्च मजबूत नियंत्रक को डिजाइन करने के लिए नियंत्रक बोड आरेख पद्धति को अपनाया है। प्रदर्शन और अनिश्चितता वजन कार्यों को परिभाषित किया गया है और बाद में एक चरण-दर-चरण नियंत्रक डिजाइन प्रक्रिया स्थापित है। तीन प्रस्तावित टोपोलॉजी के लिए नियंत्रकों की मजबूती का प्रदर्शन किया गया है प्रयोगात्मक रूप से। अंत में, प्रस्तावित टोपोलॉजी के बीच प्रदर्शन तुलना लाई जाती है दिए गए विनिर्देशों के लिए टोपोलॉजी चयन की पहचान करने के लिए।

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LIST OF ABBREVIATIONS AND SYMBOLS

CBC	Conventional buck converter
CBBC	Conventional buck-boost converter
CBDC	Conventional boost dc-dc converter
CCM	Continuous conduction mode
CD-cell	Capacitor-diode cell
CDFOBC	Capacitor-diode cell based fifth-order boost converter
CE	Characteristic equation
CF	Crossover frequency
CP	Charge-pump
CRCB	Contoured robust controller Bode
D	Duty ratio
dB	Decibel
DCM	Discontinuous conduction mode
DF	Dominance factor
DP	Dominant poles
DPP	Dominant pole placement
DSO	Digital storage oscilloscope
ESR	Equivalent series resistance
FBC	Fifth-order boost converter
FOBC	Fourth-order boost converter

GM	Gain margin
HFOBC	High-gain fifth-order boost converter
HSC	Hybrid step-up converter
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
KYBC	KY boost converter
L-C	Inductor and capacitor
L-C-D-Cell	Inductor-Capacitor-Diode Cell
LED	Light emitting diode
LHP	Left half of s-plane
LMI	Linear matrix inequality
LTI	Linear time-invariant
LVDCG	Low voltage dc-grid
MOSFET	Metal-oxide semiconductor field-effect transistor
MM	Modulus margin
M_s	Maximum sensitivity
NFOBC	New fifth-order boost converter
NMP	Non-minimum phase
PI	Proportional-integral
PID	Proportional-integral-derivative
PIL	Proportional-integral-lead
PM (ϕ_M)	Phase margin
PO	Peak overshoot or percentage overshoot

PSIM	Powersim software
PWM	Pulse width modulation
QFT	Quantitative feedback theory
RHP	Right half of s-plane
RPM (Γ)	Robust performance metric
SEPIC	Single-ended primary-inductor converter
SISO	Single-input single-output
SC	Switched-capacitor
SL	Switched-inductor
SLBC	Switched-inductor-based boost converter
SMPS	Switched-mode power supplies
ST (t_S)	Settling time
UPS	Uninterruptable power supply
Re [•]	Real part of complex number (•)
Im [•]	Imaginary part of complex number (•)
T_s	Switching time period
f_s	Switching frequency
R	Load resistance
Δi_{L1}	Ripple in inductor L_1 current
Δi_{L2}	Ripple in inductor L_2 current
Δv_{c1}	Ripple in capacitor C_1 voltage
Δv_{c2}	Ripple in capacitor C_2 voltage

Δv_{c3}	Ripple in capacitor C_3 voltage
Δi_g	Peak-to-peak ripple in source current
Δi_{c3}	Peak-to-peak ripple in capacitor C_3 current
$i_{L1(\max)}$	Peak current in inductor L_1
$i_{L1(\min)}$	Minimum current in inductor L_1
$i_{L2(\max)}$	Peak current in inductor L_2
$i_{L2(\min)}$	Minimum current in inductor L_2
$[A]$	System (or state) matrix
$[B]$	Input matrix
$[E]$	Output matrix
$[F]$	Feedthrough (or feedforward) matrix
$[x]$	State vector
s	Laplace variable
$G_{vd}(s)$	Control-to-output voltage transfer function
$G_{vg}(s)$	Input-to-output voltage transfer function or audio-susceptibility
$Z_0(s)$	Load current-to-output voltage transfer function or output-impedance
$G_c(s)$	Controller transfer function
$L_g(s)$	Loop-gain transfer function
$S(s)$	Sensitivity function
$T(s)$	Complementary sensitivity function

$S_c(s)$	Control sensitivity function
$S_n(s)$	Sensitivity function for nominal condition
$T_n(s)$	Complementary sensitivity function for nominal condition
ζ	Damping ratio
ω_n	Un-damped natural frequency
$p_{d1,d2} = (-\alpha \pm j\beta)$	Closed-loop dominant pole-pair
$p_d = (-\alpha + j\beta)$	Closed-loop dominant pole
ω_{gc}	Gain crossover frequency
W_1	Performance weight function in mixed-sensitivity framework
W_2	Weight function to limit the control effort in mixed-sensitivity framework
W_3	Uncertainty weight function in mixed-sensitivity framework
W_p	Performance weight function
W_u	Uncertainty weight function
Δ	Unstructured multiplicative uncertainty