CMOS SCALING CONSIDERATIONS IN SUB 10-NM NODE MULTIPLE-GATE FETS

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Dedicated to
My loving daughter Mahira. You have made me stronger, better and more fulfilled than I could have ever imagined.

Certificate

This is to certify that the thesis entitled ***"CMOS Scaling Considerations in Sub 10-nm Node Multiple-Gate FETs"***, being submitted by **Anil Kumar Bansal** to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering and is a record of the original bonafide research work carried out by him. The results presented in the thesis have not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

I certify that he has pursued the prescribed course of research.

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Abstract

Multiple gate-FET architecture emerged as a mainstream device to take the CMOS scaling beyond 22-nm technology node. But below 10-nm node, there are inevitably various scaling issues, which pose hindrance to the use of these devices. The thesis highlights some of these scaling issues and proposed solutions to handle it. The presented simulation work in this thesis is performed in Sentaurus TCAD environment, and all the characterization work is done using Cascade microtech manual probe station and Keysight B1500 parameter analyzer. In stacked NWFET architecture, position dependent nanowire current degrades the overall drain current and it is a reliability concern. The thesis includes a solution to this issue without degrading other performance parameters of the device. Further, a comparison of position dependent drain current for three modes of NWFET architecture namely inversion mode (IM), junctionless mode (JL), and junctionless accumulation mode (JLAM) NWFET is performed. With the use of the measurement set up, characterization of different types of FinFET structures namely Si-bulk FinFET, Si-SOI FinFET, and SiGe-SOI FinFET, is performed. Gate induced drain leakage (GIDL) current, which is the dominant source of leakage current at lower technology nodes, is compared on different types of FinFET structures. Also, a new device architecture is proposed to reduce GIDL current.

Due to small nanowire dimensions, NWFETs are vulnerable to the impact of process-induced local variations, such as the line edge roughness (LER) and random dopant fluctuation (RDF). The thesis presents a variability analysis on different modes of NWFET architecture namely IM, accumulation mode (AM) and JL mode. A 3-D quasi-atomistic LER model is used for the analysis of LER-induced mismatch in JL, IM, and AM NWFETs. The impact of 3-D LER is also compared with that of 2-D LER. In addition, another emerging simulation methodology known as statistical impedance field method is utilized to analyze the impact of RDF on the three flavors of NWFETs.

सार

22-nm प्रौद्योगिकी नोड से परे CMOS स्केलिंग लेने के लिए मल्टीपल गेट-FET आर्किटेक्चर मुख्यधारा के डिवाइसेस के रूप में उभरा हैं। लेकिन 10-nm नोड से नीचे, अनिवार्य रूप से विभिन्न स्केलिंग मुद्दे हैं, जो इन डिवाइसेस के उपयोग में बाधा उत्पन्न करते हैं। थीसिस ने इनमें से कुछ स्केलिंग मुद्दों और इसे संभालने के लिए प्रस्तावित समाधानों पर प्रकाश डाला हैं। इस थीसिस में प्रस्तुत सिमुलेशन कार्य सेंटोरस TCAD पर्यावरण में किया गया है, और सभी लक्षण वर्णन कार्य कैस्केड माइक्रोटेक मैनुअल जांच स्टेशन और कीसाइट बी 1500 पैरामीटर विश्लेषक का उपयोग करके किया गया है। स्टैक्ड NWFET आर्किटेक्चर में, स्थान निर्भर nanowire विद्युत धारा संपूर्ण विद्युत धारा में गिरावट लाता है और यह एक विश्वसनीयता चिंता का विषय है। थीसिस में डिवाइस के अन्य प्रदर्शन मापदंडों को नीचा किए बिना इस मुद्दे का समाधान शामिल है। इसके अलावा, NWFET आर्किटेक्चर के तीन मोड अर्थात् इन्वर्सन मोड (IM), जंक्शनलेस मोड (JL), और जंक्शनलेस अक्युमुलेशन मोड (JLAM) NWFET के लिए स्थान निर्भर ड्रेन विद्युत धारा की तुलना की गयी है। माप सेट अप के उपयोग के साथ, विभिन्न प्रकार के FinFET संरचनाओं के लक्षण वर्णन अर्थात् Si-बल्क FinFET, Si-SOI FinFET और SiGe-SOI FinFET का प्रदर्शन किया गया है। गेट प्रेरित ड्रेन लीकेज (GIDL) विद्युत धारा, जो कि लोअर टेक्नोलॉजी नोड्स में लीकेज विद्युत धारा का प्रमुख स्रोत है, विभिन्न प्रकार के FinFET संरचनाओं पर तुलना की जाती है। साथ ही, GIDL विद्युत धारा को कम करने के लिए एक नई डिवाइस आर्किटेक्चर प्रस्तावित है।

छोटे nanowire आयामों के कारण, NWFET प्रक्रिया-प्रेरित स्थानीय विविधताओं के प्रभाव की चपेट में हैं, जैसे कि लाइन एज रफनेस (LER) और रन्डॉम डोपेंट फ्लक्चुएशन (RDF)। थीसिस NWFET आर्किटेक्चर के विभिन्न मोड पर IM, अक्युमुलेशन मोड (AM) और JL मोड पर परिवर्तनशीलता विश्लेषण प्रस्तुत करता है। JL, IM, और AM NWFETs में LER- प्रेरित बेमेल के विश्लेषण के लिए एक 3-D अर्ध-परमाणु LER मॉडल का उपयोग किया गया है। 3-D LER के प्रभाव की तुलना 2-D LER से भी की गयी है। इसके अलावा, एक और उभरती हुई सिमुलेशन पद्धति जिसे सांख्यिकीय इम्पीडेन्स फील्ड विधि के रूप में जाना जाता है, का उपयोग NWFETs के तीन स्वादों पर RDF के प्रभाव का विश्लेषण करने के लिए किया गया है।

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List of Abbreviations

Abbreviation	Description
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
NWFET	**N**ano **W**ire **F**ield **E**ffect **T**ransistor
TCAD	**T**echnology **C**omputer **A**ided **D**esign
SOI	**S**ilicon **O**n **I**nsulator
GIDL	**G**ate **I**nduced **D**rain **L**eakage
LER	**L**ine **E**dge **R**oughnes
RDF	**R**andom **D**opant **F**luctuation

List of Symbols

Symbol	Description
Lg	Gate Length
Vt	Threshold Voltage
Vds	Drain to Source Voltage
Vgs	Gate to Source Voltage
Id	Drain Current
gm	Transconductance
ION	On Drain Current