

GROWTH AND ELECTRICAL PROPERTIES OF  
CdS-SiO<sub>2</sub>-Si STRUCTURES

by

RAJENDRA KUMAR NAHAR

DEPARTMENT OF PHYSICS

SUBMITTED

IN FULFILMENT OF THE REQUIREMENTS OF THE

DEGREE OF

DOCTOR OF PHILOSOPHY

TO THE

INDIAN INSTITUTE OF TECHNOLOGY, DELHI

JANUARY, 1979

## ACKNOWLEDGEMENTS

I am indebted to my thesis supervisors Professor A.B. Bhattacharyya and Dr.D.Nag Choudhuri for their valuable guidance and sustained encouragement which have contributed so much towards the completion of this thesis.

I am also grateful to Dr.B.Mathur and Dr.J.Vasi for their helpful suggestions at various stages of the work.

Special thanks goes to Dr.B.R.Marathe for his patience and understanding during the final stages of the work.

My deepest appreciation is extended to my colleagues and friends in the microelectronics laboratory for their cooperation and help. In particular, I would like to thank Mr.S.C.Saxena and Mr.S.Jindal.

I also wish to thank Mr.H.L.Narang for typing the manuscript with interest and care.

Acknowledgement also goes to my friend Mr.R.K.Sethia, my parents and my wife for whom words are inadequate to describe. May you share in this accomplishment.

(Rajendra Kumar Nahar)

## ABSTRACT

In the present dissertation growth and electrical properties of CdS-SiO<sub>2</sub>-Si structures are investigated in detail. It is shown that the introduction of a thin interfacial layer between CdS and Si yields improved and reproducible device characteristics compared to those from conventional CdS-Si heterojunctions. The device characteristics particularly, the reverse I-V characteristics, improves significantly by annealing in an optimised cycle. The effect of film CdS resistivity, substrate Si resistivity and oxide thickness are studied on the I-V and C-V characteristics of the CdS-SiO<sub>2</sub>-Si structures.

The structure is fabricated typically on a p-type 1-10 ohm cm resistivity Si substrate. Thin 30-40 Å<sup>o</sup> oxide layer is grown by the solution growth method. Subsequently high resistivity CdS film is deposited using coevaporation technique. Ohmic contacts are formed by evaporated Al electrodes.

The I-V characteristics of the structure exhibit leakage current of about 10 uA at 15 Volts reverse bias. The breakdown voltage is typically around 35 volts. The leakage current increases as the CdS film resistivity is lowered in the structure. Forward current is affected in the low voltage region by the oxide layer, annealing and CdS film resistivity.

The C-V characteristics reveal that the structure behave essentially as an one sided abrupt junction.

Transitions at 1 volt and 5 volts reverse bias are the features of the C-V characteristics.

The observed results have been interpreted using the existing heterojunction models. Qualitatively the functional dependence of the I-V characteristics is explained. The C-V characteristics are partially explained.

The main contributions presented in the thesis are:

1. Growth of CdS film on passivated silicon substrate of controlled resistivity by co-evaporation technique.
2. The passivated  $\text{SiO}_2$  layer helps in getting strikingly reproducible heterojunction structures (CdS- $\text{SiO}_2$ -Si), with improved and sharply defined breakdown characteristics.
3. The devices give greater opportunity to put to test the existing heterojunction models.
4. The correlation between the experiment and theory suggests the future line of work in the above area.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS

ABSTRACT

LIST OF PRINCIPAL SYMBOLS

<u>CHAPTER</u>		<u>PAGE NO</u>
I	INTRODUCTION AND SCOPE OF THE WORK	1
II	GROWTH OF CdS FILMS AND FABRICATION OF CdS-SiO <sub>2</sub> -Si STRUCTURES	14
III	CURRENT-VOLTAGE CHARACTERISTICS OF CdS-SiO <sub>2</sub> -Si STRUCTURES	43
IV	CAPACITANCE-VOLTAGE CHARACTERISTICS OF CdS-SiO <sub>2</sub> -Si STRUCTURES	63
V	INTERPRETATION OF EXPERIMENTAL RESULTS	76
VI	CONCLUSIONS	118
	VITA	128

-----