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DECEM ER 1

CERTIFICATE

This is to certify that the dissertation, **"Some New Techniques for Dictionary and Verification Approaches of Analog Fault Diagnosis"**, which is being submitted by **Siva Nageswara Rao Pinjala** for the award of degree of Doctor of Philosophy to the Indian Institute of Technology, Delhi is a record of bonafide research work, carried out under my guidance and supervision.

This dissertation has reached the standard of fulfilling the requirements of the regulations relating to the degree. The results obtained in this dissertation have not been submitted to any other University or Institute for the award of any degree or diploma.

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ABSTRACT

This thesis deals with the fault dictionary and fault verification approaches used for analog fault diagnosis.The literature in this area is reviewed in ChapterI.

Adjoint network approach is used in Chapter II for determination of node voltages of the faulty network under various assumed faulty conditions. The resulting information is stored in what is called fault dictionary. For a given faulty condition, in the new metod each node voltage is computed using just one multiplication per faulty element. This gives a method which is n times faster than the best available in the literature where n is the number of nodes in the network. This formulation allows all linear elements including controlledsources. The method is shown to be fast even for the computation of the bounds in node voltages in the presence of tolerances.

In Chapter III, the adjoint network approach is used to derive the equations of non linear analog networks efficiently. Adjoint models of non linear devices are derived containing open/short circuits. These adjoint models should be chosen so that (i) all the node voltages can be determined and (ii) Computation is as low as possible. Several criteria are presented in this Chapter for this purpose.

Selection of test nodes is an important aspect of fault dictionary approach. Some authors used the concept of ambiguity sets for this purpose. The time complexity of these

methods is first analysed in Chapter IV. Then new results are presented using what is called hashing. They are f times faster than the existing methods, where f is the number of faulty conditions.

Boolean algebra techniques are used to determine all possible sets of test nodes including the smallest ones. Currently, each fault is assumed to exist in only one ambiguity set of a node. We refer to this as a non-overlapping case. In contrast to this, in this thesis we allow a fault to lie in more than one ambiguity set of a node. This is referred to as overlapping case. It is demonstrated in Chapter IV that it is advantageous to allow overlaps wherever possible. This helps to reduce the number of accessible nodes. The complexity of this case is essentially the same as that of the non overlapping case.

Fault isolation is another aspect of fault dictionary. Currently, the best known method requires $O(\log_2 f)$ time. In this Chapter, (Chapter IV) hashing is used to do this in just $O(1)$ time.

Fault dictionary approach with multiple excitations is studied in Chapter V. It is illustrated that multiple excitations in general reduce the number of accessible nodes and increase diagnosability. The adjoint network approach for single excitation developed in Chapter II is then extended to the multiple excitations case using a single adjoint

network for all excitations. The complexity is same as in Chapter II for each excitation. The problems of (i) selection of test nodes for given excitation (ii) selection of excitations for a given set of test nodes (iii)selection of test nodes as well as excitations are studied. Hashing technique is employed to do this. The complexity of this does not directly depend on the number of excitations. Further it is linear in f as in Chapter IV. Boolean algebra techniques are also used to obtain more than one answer to these problems. Fault isolation can also be done in O(1) time.

Fault verification of Jiang et al is studied in Chapter VI. Their rank condition is improved to make it error free. Multiple exictations are used so that it is useful even when the number of accessible nodes is small. It is shown that the method works even when short circuit faults exist. A fast metod is suggested to compute the node voltages once the faulty elements are identified. A new technique is presented in this Chapter to calculate the deviations of the non-faulty elements from the nominal values using the measurements on the non-faulty network. This is done by solving a set of linear equations.

Node fault diagnosis is studied in Chapter VII. This problem is formulated efficiently using 0-1 mixed integer programming method.

Finally, the results of the thesis are summarised in Chapter VIII.

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