DESIGN AND SIMULATION OF LDMOS FIELD EFFECT TRANSISTORS FOR IMPROVED PERFORMANCE

AVIKAL BANSAL

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY DELHI
AUGUST 2018

DESIGN AND SIMULATION OF LDMOS FIELD EFFECT TRANSISTORS FOR IMPROVED PERFORMANCE

by

AVIKAL BANSAL
Department of Electrical Engineering

Submitted
in fulfillment of the requirements of the degree of Doctor of Philosophy
to the

Indian Institute of Technology Delhi
AUGUST 2018

To my loving Mother

Certificate

This is to certify that the thesis entitled **"Design and Simulation of Laterally Double Diffused Metal Oxide Semiconductor Field Effect Transistors for Improved Performance"**, being submitted by **Mr. Avikal Bansal** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

August 31, 2018

New Delhi

Dr. M. Jagadesh Kumar

Professor,

Department of Electrical Engineering,

Indian Institute of Technology Delhi,

Hauz Khas, New Delhi – 110 016,

India.

Acknowledgments

Extending a heartfelt gratitude to my supervisor **Dr. M. Jagadesh Kumar**, I would like to take this opportunity to thank him for selecting and nurturing me under his supervision. I sincerely thank him for all his support, efforts and valuable guidance throughout the course of this work. I owe a great debt of gratitude to him for inculcating research attitude in me, suggesting the research problem and ever–willing provided by him help during the period of my research. The valuable discussions, I had with him, helped me to strengthen my basics and kept me in the right direction. I drew inspiration from his attitude and enthusiasm towards research and teaching. I thank him for giving me the opportunity to work as teaching assistant in his courses to hone my skills. It is indeed a great privilege and pleasure to work under his supervision. I would also like to extend my gratitude to Lakshmi Ma'am for her hospitality and lively self, which I have always admired.

I would also like to acknowledge Dr Mukul Sarkar, Dr. Anuj Dhawan and Dr Rajendra Singh, members of my research committee and Dr. G S Visweswaran for all the kind support they lent, their time and advice. I would also like to show my gratitude to my fellow research scholars Radhakrishnan, Dr. Sindhu Ramaswamy, Shubham Sahay, N Kannan,

Dr. Rajat Vishnoi, Dr. Kanika Nadda, Dr. Dawit Burusie, Vivek Asthana, Akash Jain and Avinash Lahgere. It was indeed a pleasure working with all of them and a great learning experience. A special thanks to Dr. Gajendra Choudhary, Dr. Hitesh Shrimali and Dr. Nagarjuna Nallam who were always there for their valuable inputs, help or any guidance as needed by me. I would also like to thank the batches of post graduate students which came and went through our group for helping me grow into a better person. Special thanks to my dear friends Sara Ahmady, Ankur Singhai, Arvind Mishra, Prateek Jain, Vishal Patel, Nishant Mittal, Kuldip Patel and Devendra Singh for their warmth and affection making this period more memorable for me.

I would like to extend my deepest gratitude to my parents – Dr. (Late) Asha Bansal and Dr. G L Bansal for inspiring me to pursue carrier in research and academics. I am grateful to my elder brother Major Arnav Bansal and sister in law Ms Shagun Bansal for their love and support. I always received love, support and encouragement from my family, who always encouraged me to excel in everything that I do. I am deeply indebted to them for their moral support and encouragement.

A special mention to Dr. Nabi Hasan and his wife Ms Tabassum Hasan for their guidance and hospitality throughout my stay at IIT Delhi. My special thanks to my friends Deepak Malani and Amarjeet Singh for always being there for any support I needed during this course of time. My gratitude to the Yes!$^{+}$ group of IIT Delhi for their love, affection and always keeping me stress free.

I am greatly indebted to my wife Ms Sujata Verma Bansal for the co–operation and

patience during my research work. Her contribution has been unimaginable and the most important as she has always been there to encourage and support me during my highs and lows. She has sacrificed a lot for allowing me to pursue my research even when she needed my support.

I thank Almighty and my Gurudev H H Sri Sri Ravishakar for giving me strength to reach this goal. To conclude, I acknowledge all others who have helped me and whose names could not be accommodated in this brief Acknowledgment.

August 31, 2018 **Avikal Bansal**

New Delhi

Abstract

Power electronics is an area which is continuously improving the quality of human life and enhancing the comforts of the mankind by assisting the machines to be operational. Power devices operating in these machines channelize the flow of energy from the power source to the load. These devices should be reliable, smaller in size, light weight, cost effective and energy efficient. With the advancement in the designing and the manufacturing technology, the power devices are persistently evolved by the device engineers for the overall enhancement of all of their parameters.

The bipolar junction transistors (BJT) were used initially in power applications but with the development of the power metal oxide semiconductor field effect transistors (MOSFETs), they have completely replaced BJTs because the power MOSFETs have a large input impedance, faster operation, immunity to the second breakdown and negative temperature coefficient which not only makes them less vulnerable to thermal runaway but also makes them feasible for parallel conduction. MOSFETs should have a large current carrying capability, high breakdown voltage, fast switching speed and low power losses.

There are several types of power MOSFETS such as the vertical devices e.g. the trench

gate power MOSFET and the vertically diffused MOS (VDMOS) and the planar device e.g. the laterally double diffused MOS (LDMOS). LDMOS has fabrication steps compatible with CMOS process and also it has a higher stability and larger gain at high frequencies compared to vertical devices. Planar devices can be integrated along with analog, digital or mixed signal circuitry on a single chip to form a smart power integrated circuit (SPIC). The SPICs have a good performance, increased functionality high reliability, large power density and reduced design cycle.

The main focus of this work is to increase the breakdown voltage as well as to reduce the ON–resistance of an LDMOS. Another issue examined in this work is the reduction of fabrication complexity and find alternate ways to fabricate an LDMOS. Also with silicon reaching its performance limit, InGaAs is explored for manufacturing LDMOS to improve its overall performance. The following are the work done using TCAD simulations in this thesis:

A stepped gate LDMOS using InGaAs is proposed which shows an improvement in all the performance parameters e.g. breakdown voltage, ON–resistance, transconductance, switching speed and gate charge compared to an LDMOS with a buried p^+ region under the channel. The increase in the breakdown voltage is ascribed to the electric field modulation due to the stepped gate structure and the ON–resistance reduction is because of the feasibility of high doping in the drift region due to the stepped gate architecture.

An LDMOS utilizing its parasitic BJT by biasing its body contact separately to turn ON the BJT thus, increasing the ON current resulting in the reduction of ON–resistance and an

increase in the switching speed compared to a conventional LDMOS.

The charge plasma concept is utilized in an LDMOS, which uses metals with different work functions to form the hole and electron plasma. Its performance is comparable to that of a conventional LDMOS.

A hexagonal shaped superjunction (SJ) LDMOS is proposed which has an improved breakdown voltage and a lower ON–resistance compared to a conventional SJ–LDMOS. Because of the hexagonal shape of the pillars, electric field modulation happens in the drift region improving the breakdown voltage. The lower ON–resistance is due to more efficient use of the channel for the flow of electrons because of the wider junction formed by the channel and n–pillar.

सार

पावर इलेक्ट्रॉनिक्स एक ऐसा क्षेत्र है जो मानव जीवन की गुणवत्ता में लगातार सुधार कर रहा है और मशीनों की परिचालन में सहायता करके मानव जाति के आराम को बढ़ा रहा है। इन मशीनों में चल रहे पावर डिवाइस बिजली स्रोत से लोड तक ऊर्जा के प्रवाह को चैनलकृत करते हैं। इन उपकरणों को विश्वसनीय, छोटे आकार, हल्के वजन, लागत प्रभावी और ऊर्जा कुशल होना चाहिए। डिजाइनिंग और विनिर्माण तकनीक में प्रगति के साथ, डिवाइस इंजीनियरों द्वारा अपने सभी मानकों के समग्र वृद्धि के लिए बिजली उपकरणों को लगातार विकसित किया जा रहा है।

बाइपोलर जंक्शन ट्रांजिस्टर (BJT) का उपयोग शुरू में पावर अनुप्रयोगों में किया जाता था लेकिन पावर मेटल ऑक्साइड सेमीकांडकटर फील्ड इफैक्ट ट्रांजिस्टर (MOSFET) के विकास के साथ, उन्होंने पूरी तरह से BJT को बदल दिया है क्योंकि पावर MOSFET में लॉर्ज इनपुट इम्पीडॅन्स, तेजी से आपरेशन, सेकॅन्ड ब्रेकडाउन से प्रतिरक्षा और नकारात्मक तापमान गुणांक जो न केवल उन्हें थर्मल रनवे के लिए कम आघात योग्य बनाता है बल्कि उन्हें पैरॅलल् कन्डक्शन के लिए भी व्यवहार्य बनाता है। MOSFET में बड़ा विद्युत प्रवाह ले जाने की क्षमता, उच्च ब्रेकडाउन वोल्टेज, तेज स्विचिंग गति और कम बिजली का नुकसान होना चाहिए।

कई प्रकार के पावर MOSFETS होते हैं जैसे वर्टिकल डिवाइस उदाहरण ट्रेंच गेट पावर MOSFET और वर्टिक्ली डिफ़्यूज़्ड MOS (VDMOS) और प्लेनर डिवाइस उदाहरण लेटरली डिफ़्यूज़्ड MOS (LDMOS)। LDMOS में CMOS प्रक्रिया के साथ संगत फैब्रिकेशन चरण हैं और यह वर्टिकल डिवाइस की तुलना में उच्च आवृत्तियों पर उच्च स्थिरता और बड़ा लाभ भी है। एक स्मार्ट पावर इन्टग्रेटड सर्किट (SPIC) बनाने के लिए प्लानर डिवाइस को एक चिप पर एनालॉग, डिजिटल या मिश्रित सिग्नल सर्किट्री के साथ एकीकृत किया जा सकता है। SPIC का अच्छा प्रदर्शन होता है, कार्यक्षमता में उच्च विश्वसनीयता, बड़ी शक्ति घनत्व और डिजाइन साइकॅल में कटौती होती है।

इस काम का मुख्य किरणकेन्द्र ब्रेकडाउन वोल्टेज को बढ़ाने के साथ-साथ LDMOS के ऑन-रिज़िस्टन्स को कम करने के लिए है। इस काम में जांच की गई एक अन्य समस्या फैब्रिकेशन में सरलता है और LDMOS बनाने के वैकल्पिक तरीकों को ढूंढती है। इसके अलावा सिलिकॉन अपनी प्रदर्शन सीमा तक पहुंचने के साथ, InGaAs को LDMOS के निर्माण के लिए अपने समग्र प्रदर्शन में सुधार के लिए खोजा गया है। इस शोधलेख में TCAD सिमुलेशन का उपयोग करके निम्नलिखित कार्य किए गए हैं।

InGaAs का उपयोग कर एक स्टेप्पेड गेट LDMOS प्रस्तावित है जो सभी प्रदर्शन मानकों में सुधार दिखाता है उदाहरण तहत ब्रेकडाउन वोल्टेज, ऑन-रिज़िस्टन्स, ट्रांसकंडक्टेंस, स्विचिंग स्पीड और गेट चार्ज की तुलना LDMOS के साथ एक बरिड p+ रीजन चैनल कि करि गयी है। ब्रेकडाउन वोल्टेज में वृद्धि स्टेप्पेड गेट संरचना के कारण इलेक्ट्रिक फील्ड मॉड्यूलेशन के लिए निर्धारित है और स्टेप्पेड गेट आर्किटेक्चर के कारण बहाव क्षेत्र में उच्च डोपिंग की व्यवहार्यता के कारण ऑन-रिज़िस्टन्स की कमी है।

एक LDMOS अपने परजीवी BJT के उपयोग से BJT को चालू करने के लिए अपने बॉडि के संपर्क को अलग करके, BJT को चालू करके ऑन करंट बड़ी है, जिसके परिणामस्वरूप ऑन-रिज़िस्टन्स में कमी और पारंपरिक LDMOS की तुलना में स्विचिंग गति में वृद्धि हुई है।

चार्ज प्लाज्मा अवधारणा का प्रयोग LDMOS में किया जाता है, जो होल और इलेक्ट्रॉन प्लाज्मा बनाने के लिए विभिन्न वर्क फंक्शन के साथ धातुओं का उपयोग करता है। इसका प्रदर्शन एक पारंपरिक LDMOS की तुलना में तुलनीय है।

एक हेक्सागोनल आकार वाले सुपरजंक्शन (SJ) LDMOS का प्रस्ताव है जिसमें एक पारंपरिक SJ-LDMOS की तुलना में बेहतर ब्रेकडाउन वोल्टेज और कम ऑन-रिज़िस्टन्स है। पिलर के हेक्सागोनल आकार की वजह से, ब्रेकडाउन वोल्टेज में सुधार करने वाले बहाव क्षेत्र में विद्युत क्षेत्र मॉड्यूलेशन होता है। चैनल और n-पिलर द्वारा बनाए गए व्यापक जंक्शन की वजह से कम ऑन-रिज़िस्टन्स इलेक्ट्रॉनों के प्रवाह के लिए चैनल के अधिक कुशल उपयोग के कारण होता है।

Table of Contents

List of Figures

List of Tables