

# **POWER FACTOR CORRECTION IN SWITCHED RELUCTANCE MOTOR DRIVES**

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# **POWER FACTOR CORRECTION IN SWITCHED RELUCTANCE MOTOR DRIVES**

by

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*Submitted*

*In fulfillment of the requirements of the degree of doctor of philosophy*

to the



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## **CERTIFICATE**

This is to certify that the thesis entitled “**Power Factor Correction in Switched Reluctance Motor Drives,**” being submitted by **Mr. Aniket Anand** for the award of the degree of **Doctor of Philosophy** is a record of a bonafide research work carried out by him in the Department of Electrical Engineering of Indian Institute of Technology Delhi.

Mr. Aniket Anand worked under my guidance and supervision and has fulfilled the requirements for the submission of this thesis, which to my knowledge has reached the requisite standard. The results obtained herein have not been submitted to any other University or Institute for the award of any degree.

**Dated: May 13, 2019**

**(Prof. Bhim Singh)**  
**Department of Electrical Engineering,**  
**Indian Institute of Technology, Delhi**

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Date: May 13, 2019  
Place: New Delhi

Aniket Anand

## ABSTRACT

With the increased in energy demand, the design and development of energy efficient drive for domestic and industrial appliances, have become essential. The current harmonic regulations limit the harmonics emission by the household equipment so that it does not exceed the compatibility levels. These regulations also define the minimum power factor required for the equipment connected to single phase supply. Therefore, the drives are recommended with front end PFC (Power Factor Correction) converters to increase the power conversion efficiency and to meet the international standards for power quality, such as IEC-61000-3-2. The research in power converters has developed the keen interest of researchers in special machines, which has been developed in late nineteenth century. Brushless DC motor, permanent synchronous motor, synchronous reluctance motor and switched reluctance motor (SRM) are some of the motors, which are seeking the attraction for number of applications.

This work aims at the development of the power factor correction converters for feeding SRM drive as a cost effective solution for low power household applications. The cost and efficiency are two most important aspects, which play a vital role in the design of drives focusing towards households applications such as fans, water pumps, vacuum cleaner, washing machine etc. SRM has salient pole construction such that the stator is provided with concentrated windings, which are excited through mid-point converter, sequentially. The rotor is made up of laminated magnetic materials and free from any sort of winding. SRM has many advantages such as high torque-volume ratio, fast dynamic response, low manufacturing cost and wide speed range.

The selection of suitable PFC converter for particular application depends upon various aspect including rating of SRM motor, voltage and current rating of semiconductor devices, total number of component counts, requirement of two equal output voltages, galvanic isolation, cost and efficiency of the overall system. Out of the available PFC converter configurations, the recommended PFC converters for the proposed SRM drive, are classified into five different categories of non-isolated single output PFC converters, non-isolated dual output PFC converters, isolated single output PFC converters, isolated dual output PFC converters and bridgeless PFC converters. Among them dual output PFC converters are mainly focused as per the system requirement, as two equal output voltages are required to feed the mid-point converter fed SRM drive. In this work, PFC converters are designed to operate in DCM, to obtain inherent power

factor correction at supply mains. As the voltage follower approach is considered, therefore, sensor requirement is reduced to one voltage sensor, which reduces the system cost.

The major aspect of the work, includes simplicity in control as two equal output voltages are generated to feed the mid-point converter fed SRM drive without any voltage balancing loop. The converter configurations proposed for the SRM drive, are features with neutral point N to generate, which has reduced the stress across the semiconductor switches. Moreover, the selected DCM of operation via voltage follower approach requires simple control to obtain inherent power factor correction at input side. In this technique, PFC is obtained due to discontinuous inductor current mode during each switching period. During this period, the circuit behaves as an emulated resistance, and thus inherent wave-shaping is provided to the circuit. The controlled DC link voltage over wide range, delivers excellent speed control, which is well demonstrated in the test results. The performance of proposed PFC converters fed SRM drive is validated on the models developed in MATLAB/Simulink environment. Further, to validate the simulation results, a laboratory prototype of PFC converter fed SRM drive is developed. However, the performance evaluation of proposed SRM drive is carried out during different steady state and dynamic conditions. The voltage and current waveforms of different circuit components including circuit inductor, capacitor and semiconductor switches are analysed. The proposed PFC converters fed SRM drive is also tested under different supply voltage fluctuation conditions, which is well demonstrated through test results. The accepted power quality indices of these PFC converters fed SRM drive are also evaluated at AC mains. The found indices comply with the given power quality standard IEC 61000-3-2.

## आब्स्ट्रॅक्ट

वित्त थे इनक्रीस्ड इन एनर्जी डिमँड, थे डिज़ाइन आंड डेवेलपमेंट ऑफ एनर्जी एफीशियेंट ड्राइव फॉर डोमेस्टिक आंड इंडस्ट्रियल अप्लाइयेन्सस, हॅव बिकम एसेन्शियल. थे करेंट हारमॉनिक रेग्युलेशन्स लिमिटेड थे हारमॉनिक्स एमिशन बाइ थे हाउशोल्ड एक्विपमेंट सो तट इट डज़ नोट एक्सीड थे कंपॅटिबिलिटी लेवेलज़. दीज़ रेग्युलेशन्स ऑल्सो डिफाइन थे मिनिमम पवर फॅक्टर रिक्वायर्ड फॉर थे एक्विपमेंट कनेक्टेड तो सिंगल फेज़ सप्लाई. देफॉर, थे ड्राइव्स अरे रेकमेंडेड वित्त फ्रंट एंड पपक (पवर फॅक्टर करेक्षण) कन्वर्टर्स तो इनक्रीस थे पवर कन्वर्षन एफीशियेन्सी आंड तो मीट थे इंटरनॅशनल स्टॅंडर्ड्स फॉर पवर क्वालिटी, सच आस इयीक-61000-3-2. थे रिसर्च इन पवर कन्वर्टर्स हास डेवेलपड थे कीं इंटेरेस्ट ऑफ रिसर्चर्स इन स्पेशल मशीन्स, विच हास बिन डेवेलपड इन लाते नाइंटीत सेंचुरी. ब्रूषलेषस डीसी मोटर, पर्मनेंट साइंकरनस मोटर, साइंकरनस रिलक्टेन्स मोटर आंड स्विचड रिलक्टेन्स मोटर (स्म) अरे सम ऑफ थे मोटर्स, विच अरे सीकिंग थे अट्रॅक्शन फॉर नंबर ऑफ अप्लिकेशन्स.

तीस वर्क एम्स अट थे डेवेलपमेंट ऑफ थे पवर फॅक्टर करेक्षण कन्वर्टर्स फॉर फीडिंग स्म ड्राइव आस आ कॉस्ट एफेक्टिव सल्यूशन फॉर लो पवर हाउशोल्ड अप्लिकेशन्स. थे कॉस्ट आंड एफीशियेन्सी अरे टू मोस्ट इंपॉर्टेंट आस्पेक्ट्स, विच प्ले आ वाइटल रोल इन थे डिज़ाइन ऑफ ड्राइव्स फोकसिंग टुवर्ड्स हाउशोल्ड्स अप्लिकेशन्स सच आस फॅस, वॉटर पंप्स, वॅक्यूम क्लीनर, वॉशिंग मशीन एट्सेटरा. स्म हास सेलीयेंट पोले कन्स्ट्रक्शन सच तट थे स्टॅटर इस प्रोवाइडेड वित्त कॉन्सेट्रेटेड वाइंडिंग्स, विच अरे एग्ज़ाइटेड थ्रू मिड-पॉइंट कन्वर्टर, सीक्वेन्शियली. थे रोटर इस मेड उप ऑफ लॉमिनेटेड मॅग्नेटिक मेटीरियल्स आंड फ्री फ्रॉम अन्य सॉर्ट ऑफ वाइंडिंग. स्म हास मानी अड्वांटेजस सच आस हाइ टॉर्क-वॉल्यूम रेशियो, फास्ट डाइनमिक रेस्पॉन्स, लो मॅन्यूफॅक्चरिंग कॉस्ट आंड वाइड स्पीड रेंगे.

तीस वर्क एम्स अट थे डेवेलपमेंट ऑफ थे पवर फॅक्टर करेक्षण कन्वर्टर्स फॉर फीडिंग स्म ड्राइव आस आ कॉस्ट एफेक्टिव सल्यूशन फॉर लो पवर हाउशोल्ड अप्लिकेशन्स. थे कॉस्ट आंड एफीशियेन्सी अरे टू मोस्ट इंपॉर्टेंट आस्पेक्ट्स, विच प्ले आ वाइटल रोल इन थे डिज़ाइन ऑफ ड्राइव्स फोकसिंग टुवर्ड्स हाउशोल्ड्स अप्लिकेशन्स सच आस फॅस, वॉटर पंप्स, वॅक्यूम क्लीनर, वॉशिंग मशीन एट्सेटरा. स्म हास सेलीयेंट पोले कन्स्ट्रक्शन सच तट थे स्टॅटर इस प्रोवाइडेड वित्त कॉन्सेट्रेटेड वाइंडिंग्स, विच अरे एग्ज़ाइटेड थ्रू मिड-पॉइंट कन्वर्टर, सीक्वेन्शियली. थे रोटर इस मेड उप ऑफ लॉमिनेटेड मॅग्नेटिक मेटीरियल्स आंड फ्री फ्रॉम अन्य सॉर्ट

ऑफ वाइंडिंग. स्म हास मानी अडवांटेजस सच आस हाइ टॉर्क-वॉल्यूम रेशियो, फास्ट डाइनमिक रेस्पॉन्स, लो मॅन्युफॅक्चरिंग कॉस्ट आंड वाइड स्पीड रंगे.

थे सेलेक्शन ऑफ सूटबल पफक कन्वर्टर फॉर पर्टिक्युलर अप्लिकेशन डिपेंड्स अपॉन वेरियस आस्पेक्ट इंकलूडिंग रेटिंग ऑफ स्म मोटर, वोल्तेज आंड करेंट रेटिंग ऑफ सेमिकंडक्टर डिवाइसस, टोटल नंबर ऑफ काँपोनेंट काउंट्स, रिक्वाइर्मेंट ऑफ टू ईकल आउटपुट वोल्टएजस, गॅल्वेनिक आइसोलेशन, कॉस्ट आंड एफीशियेन्सी ऑफ थे ओवरॉल सिस्टम. आउट ऑफ थे अवेलबल पफक कन्वर्टर कॉन्फिगरेशन्स, थे रेकमेंडेड पफक कन्वर्टर फॉर थे प्रपोज़्ड स्म ड्राइव, अरे क्लासिफाइड इंटो फाइव डिफरेंट केटेगरीस ऑफ नों-आइसोलेटेड सिंगल आउटपुट पफक कन्वर्टर, नों-आइसोलेटेड ड्युयल आउटपुट पफक कन्वर्टर, आइसोलेटेड सिंगल आउटपुट पफक कन्वर्टर, आइसोलेटेड ड्युयल आउटपुट पफक कन्वर्टर आंड बरिडगेलाइज्ड पफक कन्वर्टर. अमाँग देम ड्युयल आउटपुट पफक कन्वर्टर अरे मेन्ली फोकस्ड आस पेर थे सिस्टम रिक्वाइर्मेंट, आस टू ईकल आउटपुट वोल्टएजस अरे रिक्वाइर्ड तो फीड थे मिड-पॉइंट कन्वर्टर फेड स्म ड्राइव. इन तीस वर्क, पफक कन्वर्टर अरे डिज़ाईड तो ऑपरेट इन डकम, तो ओब्टेन इन्हेरेंट पवर फॅक्टर करेक्शन अट सप्लाई मैस. आस थे वोल्तेज फॉलोवर अप्रोच इस कन्सिडर्ड, देफॉर, सेन्सर रिक्वाइर्मेंट इस रेड्यूसड तो वन वोल्तेज सेन्सर, विच रेड्यूसस थे सिस्टम कॉस्ट.

थे मेजर आस्पेक्ट ऑफ थे वर्क, इंकलूड्स सिंप्लिसिटी इन कंट्रोल आस टू ईकल आउटपुट वोल्टएजस अरे जेनरेटेड तो फीड थे मिड-पॉइंट कन्वर्टर फेड स्म ड्राइव विदाउट अन्य वोल्तेज बॅलेन्सिंग लूप. थे कन्वर्टर कॉन्फिगरेशन्स प्रपोज़्ड फॉर थे स्म ड्राइव, अरे फीचर्स वित न्यूट्रल पॉइंट न तो जेनरेट, विच हास रेड्यूसड थे स्ट्रेस अक्रॉस थे सेमिकंडक्टर स्विचस. मोरोवर, थे सेलेक्टेड डकम ऑफ ऑपरेशन वाइया वोल्तेज फॉलोवर अप्रोच रिक्वाइर्स सिंपल कंट्रोल तो ओब्टेन इन्हेरेंट पवर फॅक्टर करेक्शन अट इनपुट साइड. इन तीस टेक्नीक, पफक इस ओब्टेड ड्यू तो डिसकॉन्टिन्युवस इनडक्टर करेंट मोड ड्यूरिंग ईच स्विचिंग पीरियड. ड्यूरिंग तीस पीरियड, थे सर्क्यूट बिहेव्स आस आन एम्युलेटेड रेज़िस्टेन्स, आंड दस इन्हेरेंट वेव-शापिंग इस प्रोवाइडेड तो थे सर्क्यूट. थे कंट्रोल डीसी लिंक वोल्तेज ओवर वाइड रंगे, डेलिवर्स एक्सलेंट स्पीड कंट्रोल, विच इस वेल डेमाँस्ट्रेटेड इन थे टेस्ट रिज़ल्ट्स. थे पफार्मेंन्स ऑफ प्रपोज़्ड पफक कन्वर्टर फेड स्म ड्राइव इस वॅलिडेटेड ओं थे माँडेल्स डेवेलपड इन मतलब/सिमुलिक एन्वाइरन्मेंट. फर्दर, तो वॅलिडेट थे सिम्युलेशन रिज़ल्ट्स, आ लॅबोरेटरी प्रोटटाइप ऑफ पफक कन्वर्टर फेड स्म ड्राइव इस डेवेलपड. हवेवर, थे पफार्मेंन्स एवॅल्यूएशन ऑफ प्रपोज़्ड स्म ड्राइव इस कॅरीड आउट ड्यूरिंग डिफरेंट स्टेडी स्टेट आंड डाइनमिक कंडीशन्स. थे

वोल्टेज आंड करंट वेविफॉर्म्स ऑफ डिफरेंट सर्क्यूट काँपोनेंट्स इंकलूडिंग सर्क्यूट इनडक्टर, केपॅसिटर आंड सेमिकंडक्टर स्विचस अरे अनलाइज़्ड. थे प्रपोज़्ड पफ़क कन्वर्टर्स फेड स्म ड्राइव इस ऑल्सो टेस्टेड अंडर डिफरेंट सप्लाइ वोल्टेज फ्लक्चुयेशन कंडीशन्स, विच इस वेल डेमॉन्स्ट्रेटेड थ्रू टेस्ट रिज़ल्ट्स. थे आक्सेप्टेड पवर क्वालिटी इंडिसेस ऑफ दीज़ पफ़क कन्वर्टर्स फेड स्म ड्राइव अरे ऑल्सो एवॅल्यूयेटेड अट एसी मैस. थे फाउंड इंडिसेस कंप्लाइ वित थे गिवन पवर क्वालिटी स्टँडर्ड इयीक 61000-3-2.

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- Fig. 5.2 Buck-Boost Converter fed SRM drive
- Fig. 5.3 Operation of the buck boost converter in the DCM of operation during (a, b, c) three different modes of operation (d) associated waveform during interval I, II and III.
- Fig. 5.4 Proposed CSC Converter fed SRM drive
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- Fig.5.19 (a) Input voltage and current with improved power factor at rated condition, (b) Motor phase currents at rated condition, (c) Regulated 300 V DC across DC link and maintained DC link across mid-point and (d) Voltage across the phase A during steady state operation.
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- Fig. 5.28 Performance of proposed PFC based CSC converter fed SRM drive at rated DC link voltage as 300 V.
- Fig. 5.29 Obtained test results when converters is operated at rated conditions: (a) Simultaneous excitation of two phases at a time, (b) Current through all the four phases of the motor at rated condition, (c) Obtained PFC operation of proposed drive at rated DC link voltage as 300 V, and (d) Obtained PFC operation of proposed drive at reduced DC link voltage as 100 V.
- Fig. 5.30 (a) Performance of CSC converter with voltage and current through different circuit components and (b) zoomed view to demonstrate the circuit components operating in CCM and DCM of operation.
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- Fig. 5.32 Test results showing; (a) Current and voltage waveform through inductor L and capacitor C during PFC operation, (b) diode current, inductor current and output capacitor voltage during switch on and switch off period of switching, (c) peak voltage and current stress through switch and (d) enlarge view of Fig. 5.19. (c) showing peak voltage and current stress through during switch on period and switch off period.
- Fig. 5.33 Dynamic performance of proposed PFC converter fed SRM drive during (a) starting and (b) during change in Supply voltage from 220 V AC to 170 V AC.
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- Fig. 5.35 Test results shows the dynamic performance of proposed drive during; (a) change in DC link voltage from 150 V to 230 V, (b) change in DC link voltage from 250 V to 170 V and (c) Starting.
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- Fig. 5.37 Test result of proposed SRM drive on the basis of power quality indices with (a)-(c)  $V_{ac}=220$  V,  $V_{DC}=300$  V and  $P_{out}$  (output power)=421W, (d)-(f)  $v_{ac}=170$  V,  $V_{DC}=300$  V and  $P_{out}$  (output power)=421W, (g)-(i)  $v_{ac}=270$  V,  $V_{DC}=300$  V and  $P_{out}$  (output power)=421W and (j)-(l)  $v_{ac}=220$  V,  $V_{DC}=100$  V and  $P_{out}$  (output power)=136W.
- Fig. 5.38 Showing the steady state performance of PFC based Cuk converter fed SRM drive.

- Fig.5.39 Test results: (a) Generated switching pulses on the basis of rotor position feedback for simultaneous excitation of phase A and phase B and (b) Motor current through all the four phases during steady state.
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- Fig. 5.47 Test results of drive under dynamic conditions as: (a) Dynamics during starting at 70 V, (b) Step change in DC link voltage from 150 V to 230 V to obtain speed control correspondingly and (c) Step change in DC link voltage from 250 V to 170 V to obtain speed control correspondingly.
- Fig.5.48 Harmonic spectra of the supply current PFC converter fed SRM drive at (a) rated DC link voltage as 300 V and (b) minimum DC link voltage as 100 V.
- Fig. 5.49 Test result of proposed SRM drive on the basis of power quality indices with (a)-(b)  $v_{ac}=220$  V,  $V_{DC}=300$  V and  $P_{out}$  (output power)=381W and (c)-(d)  $v_{ac}=220$  V,  $V_{DC}=100$  V and  $P_{out}$  (output power)=105W.
- Fig. 5.50 Test result of proposed SRM drive on the basis of power quality indices with (a)-(b)  $v_{ac}=170$  V,  $V_{DC}=300$  V and  $P_{out}$  (output power)=372W and (c)-(d)  $v_{ac}=270$  V,  $V_{DC}=300$  V and  $P_{out}$  (output power)=369W.
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- Fig.5.53 Switching stress with peak switch current and voltage as 25 A and 640 V.
- Fig. 5.54 (a) Motor starting dynamics with reduced phase current and (b) Motor dynamic during change in supply voltage from 220 V AC to 170 V AC.
- Fig. 5.55 Dynamics during DC link variation from (a) 280 V DC to 200 V DC and (b) 200 V DC to 280 V DC.
- Fig. 5.56 Harmonic spectra of supply current at DC link as (a) 300 V and (b) 100 V.
- Fig. 5.57 Steady state performance at motor side at rated speed.
- Fig. 5.58 (a) Performance of SC converter with voltage and current through different circuit components and (b) zoomed view to demonstrate the circuit components operating in CCM and DCM of operation.

- Fig. 5.59 (a) Peak voltage and current stress across the PFC converter switch and (b) zoomed view of figure (a) demonstrating current and voltage across the switch during each switch on and switch off period.
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- Fig. 5.61 Performance of PFC based SC converter fed SRM drive during change in DC link voltage from (a) 300 V to 240 V and (b) 240 V to 300 V.
- Fig. 5.62 Dynamics during Supply voltage variation 170 V to 270 V AC.
- Fig. 5.63 Harmonics spectrum of supply current at supply voltage as 220 V AC and DC link voltage as (a) 300 V and (b) 100 V.
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- Fig. 5.65 Voltage and current across different circuit components during rated speed operation and (b) zoomed view of figure (a) demonstrating circuit waveform during each switching period including switch on period, switch off period and DCM period.
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- Fig. 5.67 Dynamic performance of proposed drive during (a) starting and (b) change in supply voltage from 220 V AC to 170 V AC.
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- Fig. 6.2 Double switch dual output buck boost converter fed SRM drive.
- Fig. 6.3 Operation of the proposed converter in DCM during (a, b, c) three different modes of operation (d) associated waveform during three modes of operation.
- Fig. 6.4 Proposed Zeta-SEPIC based converter fed SRM drive.
- Fig. 6.5 Proposed Zeta-SEPIC based converter during: (a) device turn on period (b) turn off period and (c) during DCM.
- Fig. 6.6 Theoretical waveform during different modes of operation.
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- Fig. 6.8 Operation of the proposed Cuk converter in DCM during (a, b, c) three different modes of operation (d) associated waveform during three modes of operation.
- Fig. 6.9 Proposed modified Cuk converter fed SRM drive
- Fig. 6.10 Converter operating modes during positive half : (a) Mode I ( $t_2-t_1$ ), (b) Mode II ( $t_3-t_2$ ), (c) Mode III ( $t_4-t_3$ ) and during negative half (d) Mode I ( $t_2-t_1$ ), (e) Mode II ( $t_3-t_2$ ), (f) Mode III ( $t_4-t_3$ ).
- Fig. 6.11 Theoretical waveforms during different operating modes.
- Fig. 6.12 Proposed Cuk-SEPIC based dual output converter fed SRM drive.
- Fig. 6.13 Proposed circuit derived from combination of two basic circuit configuration: (a) SEPIC, (b) Cuk converter.
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- Fig. 6.15 Associated voltage and current waveform in three different modes of operation.
- Fig. 6.16 Proposed dual output Luo converter fed SRM drive.

- Fig. 6.17 Operation of proposed dual output Luo converter during different operating modes; (a) & (b) switch on period, (c) & (d) switch off period and (e) & (f) DCM of operation.
- Fig. 6.18 Voltage and current waveform of the circuit components during different operating modes.
- Fig. 6.19 Modified SEPIC converter fed SRM drive.
- Fig. 6.20 DCM operation during (a, b, c) for positive half cycle, during (d, e, f) for negative half cycle and related waveforms (g) and (h) for each switching period during Modes I, II, III, IV, V and VI.
- Fig. 6.21 MATLAB/Simulink model of non-isolated dual output PFC converter fed SRM drive.
- Fig. 6.22 Motor performance at rated speed of 1500 rpm with DC link at 320 V and supply voltage at 220 V.
- Fig. 6.23 (a) Current through diode  $D_1$  and  $D_2$  and discontinuous current through inductor  $L_{o1}$  and  $L_{o2}$  and (b) Zoomed view of figure (a) demonstrating current during each switching period.
- Fig. 6.24 Switching stress with peak switch current and voltage as 20 A and 350 V.
- Fig. 6.25 Motor starting dynamics with reduced phase current at DC link voltage as 50 V and (b) Motor and converter side dynamics during supply voltage variation (220 V to 170 V).
- Fig. 6.26 Dynamics during DC link variation from (a) 320 V DC to 240 V DC and (b) 320 V DC to 240 V DC.
- Fig. 6.27 Simulated harmonics spectrum for an dual output buck-boost converter fed SRM drive with DC link voltage as (a) 300 V and (b) 100 V.
- Fig. 6.28 Steady state performance of proposed Zeta-SEPIC converter fed SRM.
- Fig. 6.29 Rated speed operation of proposed Zeta-SEPIC based converter fed SRM drive: (a) motor current, (b) Voltages across two output capacitors of Zeta and SEPIC converter (c) PFC operation at  $V_{dc}$  as 300 V, and (d) PFC operation  $V_{dc}$  as 100 V.
- Fig. 6.30 Voltage and current waveform through different circuit components of proposed dual output Zeta-SEPIC converter.
- Fig. 6.31 (a) Switching stress across PFC converter switch and (b) zoomed view of peak voltage and current stress across the switch.
- Fig. 6.32 Experimental results demonstrating: (a) Zeta converter in operation, (b) enlarge view of Zeta converter in operation, (c) SEPIC converter in operation, (d) enlarge view of SEPIC converter in operation and (e) stress through converter switch.
- Fig. 6.33 Proposed PFC converter fed SRM drive under dynamic conditions: (a) during starting and (b) during change in supply voltage from 220 V AC to 170 V AC.
- Fig. 6.34 Performance of proposed converter when DC link voltage is subjected to sudden change from: (a) 300 V to 240 V and (b) 240 V to 300 V.
- Fig. 6.35 Drive during different dynamic conditions with change in  $V_{dc}$  from; (a) from 150 V to 230 V, (b) 250 V to 170 V and (c) 0 to 50 V.
- Fig. 6.36 Simulated harmonics spectrum for an dual output Zeta-SEPIC converter fed SRM drive with DC link voltage as (a) 300 V and (b) 100 V.
- Fig. 6.37 Power quality indices during different input and output voltage conditions: (a)-(c)  $v_{ac}=220$  V,  $V_{dc}=300$  V, (d)-(f)  $v_{ac}=270$  V,  $V_{dc}=300$  V, (g)-(i)  $v_{ac}=90$  V,  $V_{dc}=300$  V and (j)-(l)  $v_{ac}=220$  V,  $V_{dc}=100$  V.
- Fig. 6.38 Motor performance at rated speed of 1500 rpm with DC link at 300 V and supply voltage at 220 V.

- Fig. 6.39 (a) Performance of proposed dual output Cuk converter demonstrating voltage and current across each circuit components and (b) zoomed view presenting mode of operation of different circuit components during each switching period.
- Fig. 6.40 (a) Peak voltage and current stress across PFC converter switch and (b) zoomed view demonstrating switch stress during each switch on and switch off period.
- Fig. 6.41 Drive performance during (a) starting dynamics with reduced phase current at DC link voltage as 50 V and (b) supply voltage change from 220V AC to 170 V AC.
- Fig. 6.42 Dynamics during DC link variation from (a) 240 V DC to 300 V DC and (b) 300 V to 240 V.
- Fig. 6.43 Simulated harmonics spectrum for an dual output Cuk converter fed SRM drive with DC link voltage as (a) 300 V and (b) 100 V.
- Fig. 6.44 Steady speed operation of proposed drive at rated DC link voltage as 300 V.
- Fig. 6.45 Obtained results demonstrating: (a) improve power quality operation with  $V_{dc}$  as 300 V, (b) PFC operation at  $V_{dc}=100$  V, (c) voltage across two output capacitors as  $V_{dc1}=V_{dc2}=150$  V, (c) two motor phases excitation at any instant and (d) motor current at rated speed.
- Fig. 6.46 Performance of proposed converter during rated conditions.
- Fig. 6.47 Zoomed view of Fig. 6.46 demonstrating voltage and current through circuit component during (a) positive half cycle and (b) during negative half cycle.
- Fig. 6.48 (a) Peak voltage and current stress through converter switch and (b) zoomed view of Fig. (a) demonstrating peak value of voltage and current during each switching period.
- Fig. 6.49 Obtained results showing; (a) continuous capacitor voltages and discontinuous inductor currents through two Cuk converters, (b), (c) enlarge view showing DCM of operation, (d) current through input inductor and two output inductors and (e) peak current and voltage stress across the switch.
- Fig. 6.50 Dynamic during (a) starting with DC link voltage as 50 V and (b) dip in supply voltage from 220 V AC to 170 V AC.
- Fig. 6.51 Fig. 6.51 Dynamic during step change in DC link voltage as (a) 300 V to 240 V and (b) 240 V to 300 V.
- Fig. 6.52 Experimental results during change in  $V_{dc}$  as: (a) 170 V to 250 V, (b) 230 V to 150 V, (c) input voltage, input current and motor phase current during starting, (d) current in all the four motor phases during starting and (e) motor phase current with  $V_{dc}$  as 50 V.
- Fig. 6.53 Simulated harmonics spectrum for an dual output modified Cuk converter fed SRM drive with DC link voltage as (a) 300 V and (b) 100 V.
- Fig. 6.54 Power quality results at different input voltages as: (a)-(c)  $V_{ac}=220$  V, (d)-(f)  $V_{ac}=170$  V, (g)-(i)  $V_{ac}=270$  V and (j)-(l) at reduced DC link voltage as 100V and input voltage as  $V_{ac}=220$  V.
- Fig. 6.55 Steady state operation of dual output Cuk-SEPIC converter.
- Fig. 6.56 Obtained test results when converters is operated at rated conditions: (a) Obtained PFC operation of proposed drive at rated DC link voltage as 300 V, (b) Two equal output voltages as 150V and rated DC link voltage as a summation of two voltages as 300 V, (c), (d) Motor speed control with PFC at two different DC link voltages as 300 V and 100 V, (e) Simultaneous excitation of two motor phases and (f) Current through all the four phases of the motor at rated condition.

- Fig. 6.57 (a) Performance of proposed converter at rated DC link and (b) zoomed view of figure (a) demonstrating circuit components under CCM of DCM operating mode as per the selected design.
- Fig. 6.58 (a) Peak voltage and current stress at rated DC link voltage as 300 V and rated supply voltage as 220V AC and (b) zoomed view of figure (a) demonstrating peak voltage and current during each switching period.
- Fig. 6.59. Test results showing; (a) Current and voltage waveform through circuit components in SEPIC converter with high resolution view (top right corner), (b) Current and voltage waveform through circuit components in Cuk converter with high resolution view (top right corner), (c) Discontinuous current through output inductors  $L_{o1}$  and  $L_{o2}$  with continuous capacitor voltages ( $V_{c1}$  and  $V_{c2}$ ) and (d) PFC operation of proposed converter with enlarge view of waveform showing large freewheeling period which ensures DCM of operation.
- Fig. 6.60 Test results with enlarge view showing peak voltage and current stress across switching device during rated condition.
- Fig. 6.61 Demonstrating dynamic during (a) starting with DC link voltage as 60 V and (b) change in input voltage from 220 V AC to 170 V AC.
- Fig. 6.62 Drive dynamic performance during change in DC link voltage from (a) 300 V to 240 V and (b) 240 V to 300 V.
- Fig. 6.63 Test results shows the dynamic performance of proposed drive during; (a) Starting, (b) change in DC link voltage from 170 V to 250 V and (c) change in DC link voltage from 250 V to 170 V.
- Fig. 6.64 Simulated harmonics spectrum for an dual output modified Cuk converter fed SRM drive with DC link voltage as (a) 300 V and (b) 100 V.
- Fig. 6.65 Test result of proposed SRM drive on the basis of power quality indices with (a)-(c)  $v_s=220$  V,  $V_{dc}=300$  V, and  $P_{out}$  (output power)=388W, (d)-(f)  $v_s =170$  V,  $V_{dc}=300$  V and  $P_{out}$  (output power)=387W, (g)-(i)  $v_s=270$  V,  $V_{DC}=300$  V and  $P_{out}$  (output power)=389W and (j)-(l)  $v_s=220$  V,  $V_{DC}=100$  V and  $P_{out}$  (output power)=121W.
- Fig. 6.66 Steady state performance of dual output Luo converter fed SRM drive.
- Fig. 6.67 Test results showing: (a) PFC operation at rated DC link voltage as 300 V and (b) PFC operation at reduced DC link voltage as 100 V Obtained test results when converters is operated at rated conditions (a) converter producing two equal output voltages and (b) current through motor phases.
- Fig. 6.68 (a) Performance of proposed converter at rated DC link voltage and (b) zoomed view of Fig. (a) demonstrating voltage and current across various circuit component operating in CCM and DCM during each switching period.
- Fig. 6.69 Peak voltage and current stress across PFC converter switch with its zoomed view.
- Fig. 6.70 Experiment results showing: (a) and (b) DCM current through two input inductors  $L_{i1}$  and  $L_{i2}$ , CCM current through two output inductors  $L_{o1}$  and  $L_{o2}$  and voltage across two capacitor  $C_1$  and  $C_2$  in CCM, (c) current through all the four inductors  $L_{i1}$ ,  $L_{i2}$ ,  $L_{o1}$  and  $L_{o2}$ , (d) zoomed views showing discontinuous inductor current and (e) peak voltage and current stress across converter switch.
- Fig. 6.71 Drive performance during (a) starting and (a) supply voltage fluctuation when input voltage changes from 220 V AC to 170 V AC.
- Fig. 6.72 Dynamic during change in DC link voltage from (a) 300 V DC to 240 V DC and (b) 240 V DC to 300 V DC.

- Fig. 6.73 Test results shows the dynamic performance of proposed drive during; (a) Starting, (b) change in DC link voltage from 250 V to 170 V and (c) change in DC link voltage from 170 V to 250 V.
- Fig. 6.74 Simulated harmonics spectrum for an dual output modified Cuk converter fed SRM drive with DC link voltage as (a) 300 V and (b) 100 V.
- Fig. 6.75 Test result of proposed SRM drive on the basis of power quality indices with (a)-(c)  $v_s=220$  V,  $V_{dc}=300$  V, and  $P_{out}$  (output power)=405W, (d)-(f)  $v_s =90$  V,  $V_{dc}=300$  V and  $P_{out}$  (output power)=396W, (g)-(i)  $v_s=270$  V,  $V_{DC}=300$  V and  $P_{out}$  (output power)=408W and (j)-(l)  $v_s=220$  V,  $V_{DC}=100$  V and  $P_{out}$  (output power)=155W.
- Fig. 6.76 Motor performance at rated speed of 1500 rpm with DC link at 320 V and supply voltage at 220 V.
- Fig. 6.77 Test results demonstrating: (a) equal voltage across two output capacitors as  $V_{dc1}=V_{dc2}=150$  V, (b) improve power quality operation with  $V_{dc}$  as 300 V, (c) PFC operation at  $V_{dc}=100$  V and (d) motor current.
- Fig. 6.78 Performance of proposed converter during positive and negative half of the supply voltage.
- Fig. 6.79 Voltage and current waveform though different circuit components during (a) positive half of the supply voltage and (b) during negative half of the supply voltage.
- Fig. 6.80 Peak voltage and current stress through converter switch.
- Fig. 6.81 Test results demonstrating: (a) continuous current through  $L_i$ , discontinuous current through  $L_o$  and continuous voltage across  $V_{c1}$  and  $V_{c2}$ , (b) converter operation during each switching period, (c) intermediate capacitors operating in CCM mode and (d) switching stress across the device.
- Fig. 6.82 Motor and converter side dynamics during supply voltage variation
- Fig. 6.83 Dynamics during DC link variation from (a) 240 V DC to 300 V DC and (b) 300 V to 240 V DC.
- Fig. 6.84 Test results during change in  $V_{dc}$  as: (a) 250 V to 170 V, (b) 150 V to 230 V, and (c) input voltage, input current and motor phase current during starting.
- Fig. 6.85 Simulated harmonics spectrum for an dual output modified SEPIC converter fed SRM drive with DC link voltage as (a) 300 V and (b) 100 V
- Fig. 6.86 Power quality results at different input voltages as: (a)-(c)  $V_{ac}=220$  V, (d)-(f)  $V_{ac}=170$  V, (g)-(i)  $V_{ac}=270$  V and (j)-(l) at reduced  $V_{dc}$  as 100V and input voltage as  $V_{ac}=220$  V.
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## LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
BL	Bridgeless
CCM	Continuous Conduction Mode
CF	Crest Factor
CRM	Critical Conduction Mode/Critical Current Mode
CSC	Canonical Switching Cell
DAC	Digital to Analog Converter
DBR	Diode Bridge Rectifier
DC	Direct Current
DCM	Discontinuous Conduction Mode
DF	Distortion Factor
DPF	Displacement Power Factor
DSP	Digital Signal Processor
EMF	Electro Magnetic Force
EMI	Electro Magnetic Interference
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
I/O	Input/Output
HFT	High Frequency Transformer
LC	Inductor Capacitor
PCB	Printed Circuit Board
PF	Power Factor
PI	Proportional Integral
PMBLDC	Permanent Magnet Brushless DC
PWM	Pulse Width Modulation
PFC	Power Factor Correction
RMS	Root Mean Square
RTI	Real Time Interface
SC	Switched Capacitor
SEPIC	Single Ended Primary Inductance Converter

SRM	Switched Reluctance Motor
THD	Total Harmonic Distortion
UPF	Unity Power Factor
ZVS	Zero Voltage Switching

## LIST OF SYMBOLS

$C_1, C_{i1}, C_{i2}$	Capacitance of Input Side Intermediate Capacitors (F)
$C_2, C_{21}, C_{22}$	Capacitance of Output Side Intermediate Capacitors (F)
$C_{dc1}, C_{dc2}$	Capacitance of DC Link Capacitors (F)
$C_f$	Capacitance of Filter Capacitor (F)
$C_{fmax}$	Maximum Capacitance of Filter Capacitor (F)
$D_{max}$	Maximum Duty Ratio
$D_{min}$	Minimum Duty Ratio
$f_c$	Filter Cut-off Frequency (Hz)
$f_L$	Line Frequency (Hz)
$f_{sw}$	Switching Frequency (Hz)
$I_{dc}$	DC Link Current (A)
$i_A, i_B, i_C, i_D$	Phase Currents of SRM
$i_{Li}, i_{Li1}, i_{Li2}$	Input Side Inductor Current (A)
$i_{Lo}, i_{Lo1}, i_{Lo2}$	Output Side Inductor Current (A)
$i_{sw}, i_{sw1}, i_{sw2}$	PFC Converters Switch Current (A)
$i_s$	Drive Input Current (A)
$I_m$	Input Peak Current (A)
$K_{pv}, p_{pv}$	Proportional Gain for Voltage Controller
$K_{iv}, p_{iv}$	Integral Gain for Voltage Controller
$L_f$	Filter Inductor (H)
$L_i, L_{i1}, L_{i2}$	Inductance of Input Side Inductor (H)
$L_m, L_{m1}, L_{m2}$	Magnetizing Inductance of High Frequency Transformer (H)
$L_s$	Source Inductance
$N$	Speed of SRM (rpm)
$N_1$	Number of Primary Turns of High Frequency Transformer
$N_2, N_3$	Number of Secondary Turns of Two Windings of High Frequency Transformer
$N_2/N_1$	Transformation Ration of High Frequency Transformer
$P_i$	Instantaneous Power
$P_{max}$	Maximum Power ( $P_{max}$ )
$P_{min}$	Minimum Power ( $P_{min}$ )

$P_{rated}$	Rated Power of SRM Motor (W)
$R_L$	Emulated Load resistance ( $\Omega$ )
$T_e$	Electromagnetic Torque of SRM Motor (Nm)
$T_s$	Sampling Time (sec)
$T_{rated}$	Rated Torque of SRM Motor (Nm)
$v^*_{ref}$	Reference Voltage (V)
$v_e$	Comparator Error Output Voltage
$v_{cdc}$	Controlled Output Voltage
$V_{dc}$	Total Sensed DC Link Voltage (V)
$V_{dc1}, V_{dc2}$	Voltage Across Two series Connected Output DC Link Capacitor (V)
$V_{dcmax}$	Maximum DC Link Voltage (V)
$V_{dcmin}$	Minimum DC Link Voltage (V)
$v_s$	Input Voltage (V)
$V_{in}$	Input Voltage After DBR (V)
$V_m$	Peak Value of Input Voltage After DBR (V)
$v_{smin}$	Minimum Supply Voltage (V)
$v_{max}$	Maximum Supply Voltage (V)
$V_{c1}, V_{c2}$	Voltage Across Intermediate Capacitors (V)
$v_{sw}, v_{sw1}, v_{sw2}$	Voltage Across Semiconductor Switches (V)
$\omega$	Speed of SRM (rad/sec)
$\omega_L$	Line Frequency (rad/sec)
$\Delta i_{Li}, \Delta i_{L1}, \Delta i_{L2}$	Ripple Current in Input Side Inductor (A)
$\Delta i_{Lo}, \Delta i_{Lo1}, \Delta i_{Lo2}$	Ripple Current in Output Side Inductor (A)
$\Delta V_c, \Delta V_{c1}, \Delta V_{c2}$	Ripple Voltage Across Input Intermediate Capacitors (V)
$\Delta V_{c21}, \Delta V_{c22}$	Ripple Voltage Across Output Intermediate Capacitors (V)
$\eta$	Percentage of Ripple Current in Input Inductor (A)
$\chi, \kappa$	Percentage of Ripple voltage Across Intermediate Capacitor (V)
$\delta$	Percentage of Voltage Ripple across Two DC Link Capacitors (V)